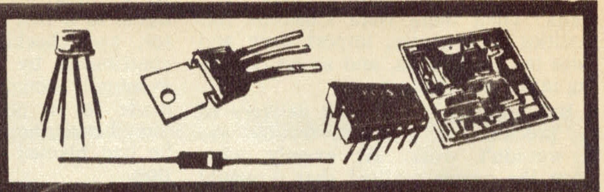
Fundamentals of SOLID STATE



Chapter 8

by Jamieson Rowe

Field-effect transistors — the junction FET — operation — cut-off and pinch-off — channel current "plateau" — static drain-source characteristics — triode and pentode operation, depletion and enhancement modes—the transfer characteristic — transconductance — other parameters and characteristics — constant current diodes — insulated gate FETs — the three basic types of MOSFET — the dual-gate MOSFET — insulation breakdown.

In the discussion of unijunction device operation given in the last chapter it was noted that one aspect of device behaviour involved a so-called "field effect" mechanism, in which the effective conductivity of one region of the device was modulated by the width of a depletion layer extending from an adjacent P-N junction. Mention was made of the fact that this type of mechanism is quite important, and that it actually forms the basis of a number of useful semiconductor devices. The best-known of these devices is the **field-effect transistor,** and it is appropriate that we now turn our attention to this device.

Like the unijunction, the field-effect transistor is a device whose complexity is only slightly greater than that of the basic semiconductor diode. However, even more so than in the case of the unijunction, the field-effect transistor is a device capable of performing many unique and highly useful functions. Because of this it has, in recent years, found use in many different applications, and it seems likely that it will be used to an even greater extent in the future.

In concept, the field-effect transistor was actually the first semiconductor amplifying device to be proposed. Far-sighted American engineer Julius E. Lilienfeld first proposed such a device as early as 1928, and patented the idea in 1930. Then in 1948 the pioneering semiconductor physicist William Shockley proposed a more practical form of the device—although his work at that time actually led to the development, with W. Brattain and J. Bardeen, of the bipolar transistor.

Despite the early theoretical predictions, it was not until 1958 that the first commercial field-effect transistor appeared. Called the "Tecnetron," it was developed by Polish scientist Stanislaus Teszner in the laboratories of the French firm, Compánie Francais Thompson-Houston.

The Tecnetron was a germanium device and had rather limited performance; as a result, interest in field-effect devices did not really awaken until 1960, when the first commercial silicon device was produced by the American firm Crystalonics, Inc. Since then the devices have been developed to a stage where they are now highly competitive with the more established bipolar devices.

A number of different varieties of field-effect transistor have been developed, and although it is true that these all operated in a broadly similar fashion, the differences are significant enough to justify at least partially individual treatment. Accordingly, this chapter will adopt the procedure of dealing initially and primarily with the device which represents the most direct development from the basic semiconductor diode, namely **the junction field-effect transistor** or **"JFET."** It will use this device to develop most of the basic concepts and will then deal briefly with the other main types of device.

Other names which have been used for the JFET are "fieldistor" and "unipolar transistor," the latter term intended mainly to distinguish the device from the bipolar transistor.

In structure, the JFET is only slightly more complex than the unijunction, which we examined in the last chapter. It consists basically of a narrow strip or **channel** of lightly doped semiconductor material, whose effective conductivity is modulated by the width of the depletion layer or layers associated with one or more P-N junctions formed between the channel and adjacent heavily doped **gate regions.**

Like the unijunction, the JFET may in theory be made from either germanium or silicon; in practice, it is made almost exclusively from silicon because of the lower saturation currents and higher performance which this material offers. And, as may be expected, it is possible to make "complementary" versions of the JFET—i.e., one can produce either a device having an N-type channel region and adjacent P-type gate regions, or alternatively a device with the opposite arrangement. Both types of JFET are in fact produced, and both are found in typical circuit applications.

Figure 8.1 shows the basic structure of a modern silicon JFET device of the "N-channel" variety. It may be seen that the lightly doped N-type channel of the device is roughly U-shaped, and that it is bounded on either side by heavily doped gate regions. The electrodes connecting to the gate regions are labelled here "gate 1" and "gate 2," but in most devices these connections are tied together internally and brought out as a single **gate electrode.**

The electrodes connecting to the ends of the channel region are conventionally known as the **source** and **drain** electrodes. However, in most JFETs the internal structure is symmetrical, so that these labels are actually interchangeable.

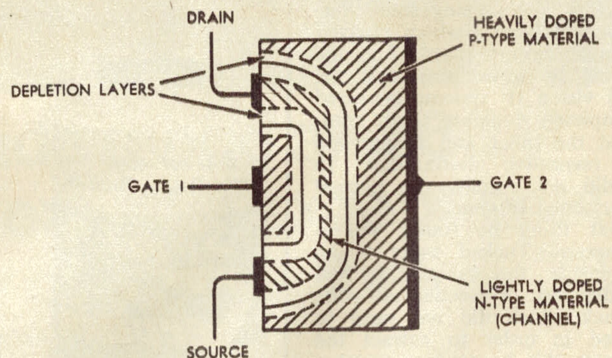


Figure 8.1

Naturally enough, even when such a device is in equilibrium with no external bias voltages applied to the electrodes, the familiar depletion layers will be set up in the vicinity of the P-N junctions along the sides of the channel. And because the channel material is intentionally doped rather lightly, compared with the gate regions, these depletion layers will extend further on the channel side of the junctions than on the gate side, as shown.

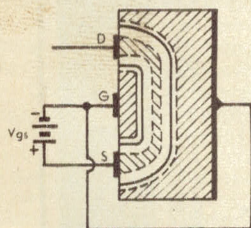
As we have seen in earlier chapters, a depletion layer is a region in a semiconductor which has been effectively "converted" into very high resistivity by the removal of all current carriers. Because of this very high resistivity, a depletion layer is actually closer to an insulator than to a conductor.

The depletion layers which extend into the channel region of a JFET thus represent areas in that region which are capable of only slight conduction relative to the remaining central strip. As a result the effective

electrical width of the channel is somewhat less than its physical width, and its resistance is accordingly higher than would be the case if the depletion layers were not present.

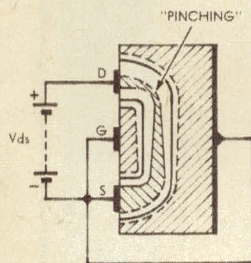
From the discussions of P-N junction operation and depletion layer behaviour given in earlier chapters, it should be fairly easy for the reader to see that if an external bias voltage is applied to the JFET between the gate and channel regions, it will change the effective width of the channel region and hence change its resistance from the equilibrium value. An external voltage which reverses biases the gate-channel junctions will cause the depletion layers to widen, encroaching further into the channel to reduce its effective width still further and increase its resistance. Conversely, if the external voltage forward biases the junctions, the depletion layers will narrow, widening the effective width of the channel and lowering its resistance.

If another external voltage is applied to the device between the drain and source electrodes, the current drawn by the channel region will naturally depend upon both the applied drain-source voltage and upon the channel resistance. But the channel resistance is itself determined by the actual bias voltage present across the gate-channel junctions which will depend in turn upon both the external gate-channel bias and the drain-source voltage.



(NO CHANNEL CURRENT) GATE-CHANNEL CHARACTERISTIC AS FOR A NORMAL P-N DIODE. FOR REVERSE BIAS AS SHOWN, ONLY A SMALL AND VIRTUALLY CONSTANT SATURATION LEAKAGE CURRENT Igss FLOWS.

(a)



Ids
Idss
PINCH-OFF "KNEE"
PINCH-OFF "PLATEAU" OR CONSTANT CURRENT REGION
AVALANCHE BREAKDOWN
Vp
Vds

Figure 8.2

(b)

Hence the channel current which flows will be determined by both the gate-channel and drain-source voltages.

Although the relationship between channel current and the applied voltages may seem rather complex from the foregoing, it can be broken down into two quite simply understood mechanisms. One of these is associated with an "external" gate-channel junction bias component provided by the external gate bias voltage, while the other is associated with an "internal" bias component derived within the device from the applied drain-source voltage. The two mechanisms may be understood by reference to the diagrams of figure 8.2.

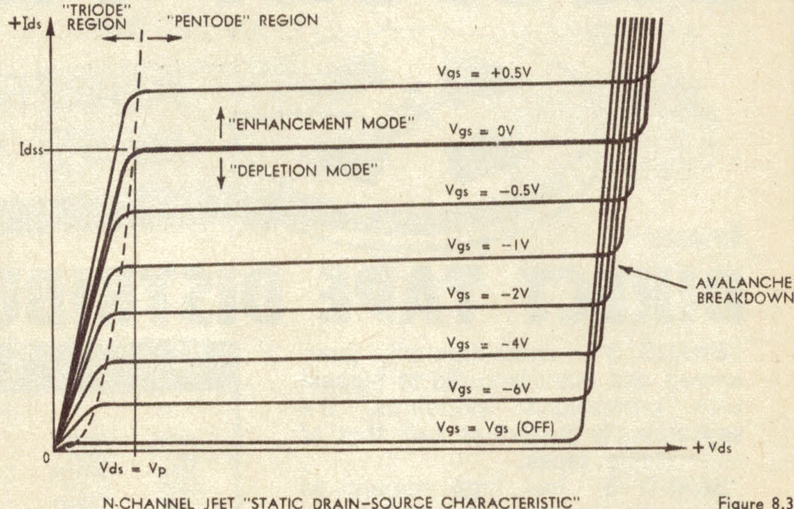
The diagram of figure 8.2 (a) shows the effect of an external gate-source bias Vgs applied to the JFET, with the drain electrode left unconnected. Here there is no longitudinal channel current, and hence no source of "internal" junction bias. The external bias simply causes the depletion layers of the junctions to adjust evenly to the altered conditions. In fact the gate-channel junctions of the device will behave in these circumstances exactly as a normal P-N diode.

If the polarity of Vgs corresponds to reverse bias of the junctions, as shown, the depletion layers will be found to extend considerably into the channel; at the same time only a small and almost constant gate-source saturation current **Igss** will flow. Conversely if Vgs were connected to bias the junctions in the forward direction, the depletion layers would be found to extend only a small distance into the channel. Of course if the forward bias were increased beyond the turn-on knee (0.6V in the case of a silicon device), significant gate-source current would flow; however, as will be seen later this significantly disturbs device operation, and is therefore not permitted to occur in the majority of JFET applications.

In the reverse-bias situation, there will naturally be a value of applied gate-source bias Vgs at which the depletion layers will have extended sufficiently to meet one another along virtually the **full length** of the narrow portion of the channel. For this and higher reverse-bias values of Vgs, therefore, the narrow portion of the channel will effectively consist of very high resistivity material— i.e., the channel will be effectively **cut off.**

The value of Vgs at which cutoff occurs is known as the **cutoff bias**, usually symbolised by **Vgs(off).** With typical JFETs it varies between about −1V and −10V, depending upon the doping levels and the device dimensions or "geometry."

When external gate-source bias alone is applied to the JFET, then, the depletion layers are uniform in width along the length of the channel, and the latter has a uniform width which is directly related to the gate-source bias. As soon as the applied voltage reaches the reverse-bias value Vgs (off) where the depletion layers meet, the channel is cut off. This illustrates the first of the two mechanisms responsible for JFET operation.



N-CHANNEL JFET "STATIC DRAIN-SOURCE CHARACTERISTIC"

Figure 8.3

The second mechanism is that which is best seen when only drain-source bias is applied to the device, as illustrated in figure 8.2(b). Here the two gate regions are tied to the source electrode, so that in this case there can be no external component of gate-channel bias. However, because the drain-source bias voltage Vds is applied between the ends of the channel, there is a current and a voltage gradient in the latter, and this produces an **internal** gate-channel bias component.

Because of the voltage gradient in the channel, the gate-channel junctions will in fact be reverse-biased to an increasing extent along the channel length. The reverse bias will reach a maximum value at the drain end, where virtually the full value of the drain-source voltage Vds will be present as reverse bias.

As a result of the progressive increase in reverse bias, the junction depletion layers will increase progressively in width along the length of the channel as shown. At the source end they will have the modest width corresponding to equilibrium conditions, while at the drain end they will have widened to correspond to a reverse bias of Vds.

Because of this progressive widening of the depletion layers, a pronounced "pinching" occurs at the drain end of the narrow portion of the channel. Naturally the result of this pinching effect is that the effective channel resistance does not remain constant at its initially low value, but rises with increasing drain-source voltage. The

change in resistance is slow at first, but becomes more rapid as Vds rises.

If Vds is increased sufficiently, a point is eventually reached where the "pinching" of the channel at the drain end becomes virtually complete. The depletion layers effectively touch one another in the pinched region, converting this portion of the channel into high resistivity "intrinsic" material. Further increase in Vds then simply causes this "pinched off" portion of the channel to extend further down the channel towards source end.

Re-stating the situation, the result of this mechanism is that the drain-source current Ids drawn by the channel rises sharply with small values of Vds, then rises more slowly and finally flattens off as pinch-off is reached at the drain end of the channel. This is shown in the graph plotted on the right of figure 8.2(b), and it may be seen that the channel current has a distinct "knee" at the onset of pinch-off.

Not surprisingly, perhaps, the value of gate-channel reverse bias at the drain end of the channel which corresponds to the onset of pinch-off is known as the **pinch-off voltage,** symbolised **Vp.** Hence for the situation of figure 8.2(b) pinch-off occurs when Vds=Vp, because virtually the whole of Vds appears as reverse bias at the drain end of the channel.

With most devices the value of the pinch-off voltage Vp is almost exactly the same as that of the cutoff bias Vgs(off). A moment's thought should reveal why this is so: Vgs (off) effectively represents the junction bias necessary for the channel depletion layers to meet fully **throughout the length of the channel,** while Vp effectively represents the bias necessary at the drain end of the channel to cause the depletion layers to meet **in that region.** Providing the channel is reasonably uniform in width, therefore, one would expect the values of Vp and Vgs (off) to be identical.

Note, however, that this equivalence in value between Vp and Vgs (off) does not imply that the two have the same significance, or that "pinch-off" and "cut-off" are simply alternative names for the same situation. Vp and Vgs (off) merely have the same value because the two phenomena concerned each begin when the gate-channel depletion layers meet.

The important difference between pinch-off and cut-off is that in the cut-off situation the depletion layers have met throughout the length of the channel, converting the whole of the channel to high resistivity material, and preventing the flow of significant channel current even when drain-source voltage is applied; whereas in the pinch-off situation the meeting of the depletion layers involves only a relatively small portion of the total channel length, with the result that current flow is merely regulated.

The cutoff situation may actually be regarded as a special and "limit" case of pinch-off, as may become clear shortly. This is because the term "pinch-off" really applies to any situation in which the drain-source voltage Vds is equal to or greater than Vp.

It may be seen from figure 8.2(b) that for values of Vds above the pinch-off voltage Vp, the drain-source current Ids remains virtually constant, forming a "plateau" region. This is a result of the fact that drain-source voltages larger than Vp simply cause the pinched off portion of the channel to extend back toward the source end. The very high resistivity of the extending pinched off region thus effectively "absorbs" the additional voltage, maintaining the current constant at substantially its value at the pinch-off knee.

The drain-source current level corresponding to the constant - current "plateau" in the zero-external-gate-bias situation of figure 8.2(b) is known as the **zero-bias saturation current,** symbolised **Idss.** Like Vgs(off) and Vp, Idss is actually quite an important JFET behaviour paramater. It, too, varies with doping levels and device geometry, as one might expect, and with typical devices it ranges between about 1mA and 30mA.

Note that while the JFET pinch-off plateau current is termed a "saturation" current, it is a saturation current of a different type from that which flows through a reverse-biased P-N junction. As we saw in earlier chapters the latter type of current is "saturated" in the sense that it is limited by the number of available current carriers generated by the "intrinsic" mechanism; the JFET plateau current is limited, not by the number of carriers available, but by the pinching action of the channel depletion layers.

The channel current of the JFET remains substantially constant in the pinched-off region, then, over a wide range in drain - source voltage Vds. Significant increase in the channel current only occurs if Vds is increased to the point where the electric field strength in the depletion layers is sufficient to initiate avalanche breakdown. The current then rises sharply, as may be seen, and also the device dissipation.

As with the devices which were discussed in earlier chapters, the JFET can enter avalanche breakdown without necessarily sustaining damage. However, avalanche is a high dissipation region of operation, and like any other device a JFET has the usual continuous and short-term power dissipation ratings based on the allowable internal temperature rise. Accordingly, many low-power JFET devices may only be operated in the avalanche region, or even in some cases on the upper portion of the pinch-off plateau, for very short periods.

Although the two mechanisms involved in JFET operation have been treated separately in the foregoing discussion, and are shown separately in figure 8.2, they are generally both involved in device operation. Most JFETs are operated with both gate-source bias Vgs and drain-source bias Vds applied, so that the gate-channel junctions are presented with both "external" and "internal" bias components, and both mechanisms contribute to device operation.

The combined effect of the two mechanisms is basically a straightforward additive one. The external gate-source bias Vgs provides a fixed component of gate-channel bias, and hence contributes to widening (or narrowing) of the channel depletion layers in a uniform fashion, while the drain-source bias Vds provides a progressive internal reverse bias component, and hence a tapering or pinching contribution to the depletion layer width. The resultant width of the depletion layers is simply the sum of the two.

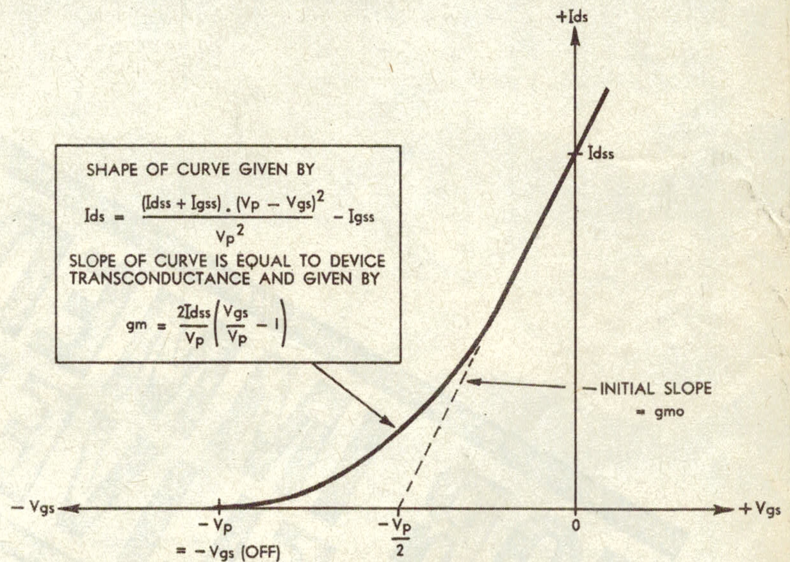


Figure 8.4 N-CHANNEL JFET "STATIC TRANSFER CHARACTERISTIC"

Pinch-off still occurs when the effective gate-channel reverse bias at the drain end of the channel is equal to Vp, the pinch-off voltage. However, this point will no longer in general correspond to the point where Vds=Vp, as in the zero-external-gate-bias case, but because Vgs also contributes to the depletion layer width it will now correspond to the situation

$$Vds - Vgs = Vp \qquad \ldots (8.1)$$

where the negative sign simply draws attention to the fact that the external gate bias is nominally of the opposite polarity to the drain bias.

In other words, the effect of a fixed negative bias component produced by Vgs is simply to lower the value of drain-source voltage Vds at which pinch-off is reached. The higher Vgs is made, the wider the uniform widening of the channel depletion layers and the lower the value of Vds at which the layers meet at the drain end.

Ultimately, of course, if Vgs is made equal to or greater than Vp, and hence

equal to or greater than Vgs(off), the device is in the pinch-off region of operation even when Vds=0 —i.e., it is cut off. Hence the reason for regarding the "cutoff" condition as a special and limiting case of pinch-off.

Naturally the converse effect occurs if the applied gate-source bias is in the forward-bias direction. Here the effect will be to increase the value to which Vds may be raised before pinch-off is reached.

It should be noted in passing that in saying that the drain-source voltage Vds and the gate-source voltage Vgs both contribute to the width of the channel depletion layers, and hence to pinch-off, all we are really saying is that it is the **effective drain-gate voltage** present across the device which determines whether or not it has entered pinch-off.

In short, an alternative general requirement for pinch-off is that the drain-gate voltage Vdg must be equal to or greater than the pinch-off voltage Vp.

With either polarity of applied gate-source bias, the altered depletion layer situation also results in a value of pinch-off plateau current different from the value Idss corresponding to the zero-bias case. When Vgs is of the reverse-bias polarity the plateau current level is naturally lower than Idss, while with Vgs values of the forward-bias polarity (but below about 0.6V) the plateau current level exceeds Idss.

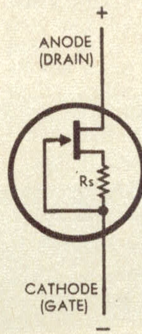
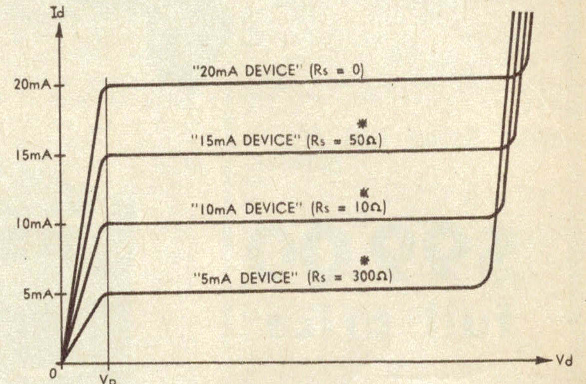
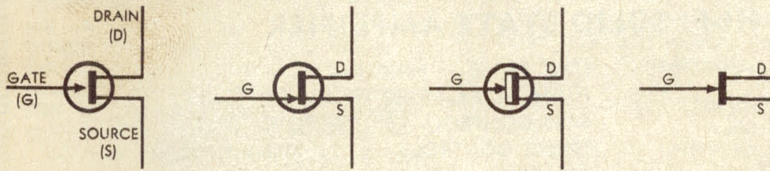


Figure 8.6





(a) N-CHANNEL JFET SYMBOLS

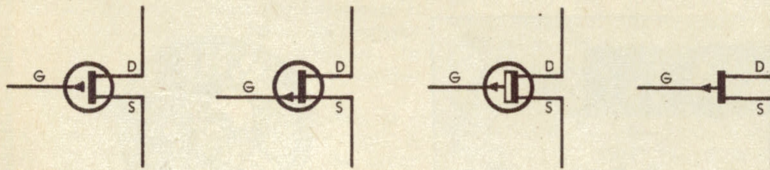


Figure 8.5 (b) P-CHANNEL JFET SYMBOLS

Because each value of Vgs thus results in both a unique value of Vds corresponding to the pinch-off knee, and also a unique value of pinch-off plateau current, it is convenient to represent JFET operation by a family of characteristic Vds/Ids curves of the type shown in figure 8.3. The polarities shown are for an N-channel device as shown in figure 8.1; for a P-channel device they would be reversed.

It may be seen that for each of the sample values of Vgs for which the curves are drawn, there is a different value of Vds appropriate to the pinch-off knee. In fact the knee points of the curves all lie on a parabolic locus (dashed curve), which is exactly what one would expect from the relationship given in expression (8.1). Similarly each curve has its current plateau at a different value of Ids.

The portions of the various curves to the **left** of the dashed knee-point locus may be seen to resemble fairly closely the familiar plate characteristics of a triode thermionic valve. For this reason this area of the JFET drain-source characteristics is often called the "triode region" of operation. Similarly because the remaining portions of the various curves resemble the plate characteristics of a pentode thermionic valve, this area of the characteristics is often called the "pentode region" of operation.

In most circuit applications JFETs are operated in the pentode region of operation—that is, at operating points to the **right** of the dashed curve in figure 8.3.

Because the narrower channel depletion layers produced by forward gate-source bias result in higher Ids (or "enhanced channel conduction") of a device in the pentode region of operation, relative to the zero-bias situation, this mode of operation is known as **enhancement mode.** This mode of JFET operation is represented in figure 8.3 by the curve marked "Vgs = +0.5V".

Fairly obviously the range of enhancement mode operation possible with JFETs is rather limited, because Vgs cannot be increased beyond the point where forward conduction current begins to flow through the gate-channel junctions. However, it will be shown later that other types of field-effect device are capable of more extended enhancement mode operation.

In contrast with forward gate-source bias, reverse bias produces wider channel depletion layers and results in lower Ids or "depleted channel conduction" in the pentode region of operation, again relative to the zero-bias situation. This mode of operation is accordingly known as the **depletion mode,** as shown.

JFET devices are almost always biased to a quiescent operating point in the depletion mode region, if only for the reason that this allows a device to be swung over a greater dynamic range before non-linearity occurs.

A further point which may be noted from figure 8.3 is that the drain-source voltage Vds at which a device enters avalanche breakdown reduces with increasing reverse gate-source bias Vgs. This is really only to be expected, because Vgs and Vds are additive in terms of the effective maximum reverse bias present across the gate-channel junctions at any time.

In effect, then, it is really the drain-gate voltage present across the device which determines whether or not it enters avalanche breakdown, just as this same voltage determines whether or not the device is operating in the pinch-off or pentode region. Hence a common way of rating a JFET in terms of its avalanche breakdown point is to quote its **drain-gate breakdown voltage,** usually symbolised **BVdgo.**

JFET "static drain-source characteristics" of the type illustrated in figure 8.3 show quite well the operation of the device, as may be seen. However, for design work they are often of less interest and lower utility than the so-called "static transfer characteristic," which is illustrated in figure 8.4. This curve shows the controlling action of gate-source bias Vgs upon the device drain-source current Ids, for the pentode region of device operation (only).

Note that whereas there is a whole family of curves comprising the static drain-source characteristics, the static transfer characteristic consists of but a single curve. This arises from the fact that the transfer characteristic by definition only applies to the pentode region of operation, where the constant-current nature of the drain-source characteristics makes the "transfer" or controlling effect of Vgs over Ids virtually independent of drain-source voltage Vds.

It may be seen that the transfer characteristic is a parabolic curve whose shape and slope are described by the expressions shown. The essential points to note are that the curve cuts the Ids axis at a value equal to Idss, the zero bias drain-source current, and that it becomes asymptotic to the Vgs axis at a value equal to both Vgs(off) and Vp.

The transfer characteristic describes the relationship between Ids and Vgs, so that its slope at any point represents the rate of change in Ids for a change in Vgs—i.e., the **transconductance** or "mutual conductance," usually symbolised **gm.**

Because of the parabolic shape of the curve, its maximum slope occurs in the region where it crosses the zero bias or Ids axis, at Idss. In other words, the transconductance of a JFET is greatest when the device is operating at zero or slight forward gate bias.

This being the case, device manufacturers usually specify the transconductance of a JFET for the zero-bias condition, where it is nominally at a maximum. This "maximum transconductance" is usually symbolised **gmo.** Because of the shape of the transfer curve gmo is closely approximated by the simple expression

$$gmo = \frac{-2.Idss}{Vp} \qquad \ldots (8.2)$$

which in graphical terms simply corresponds to the dashed line in figure 8.4 joining the Ids axis at Idss and the Vgs axis at —Vp/2.

An alternative to gm sometimes quoted on JFET data sheets is the **forward transadmittance,** symbolised **Yfs.** This is strictly a more general device parameter, including any susceptance (inverse reactance) components of the transfer behaviour in addition to conductance. However, in most cases it is specified at a low frequency (around 1KHz) where the zero-bias value of Yfs is generally almost identical with gmo.

For typical JFET devices in current production, gmo ranges from about 1000-8000 micromhos, or 1—8mA/V.

From figure 8.4 and from expression 8.2 it may be seen that the transconductance characteristics of a JFET are closely determined by the zero bias current Idss and the pinch-off voltage Vp. In fact, knowing these two parameters it is quite easy both to calculate gmo and to construct the transfer characteristic. This provides further evidence of the importance of the two parameters.

It may be worthwhile to summarise our present discussion of the JFET by drawing attention to those unique aspects of the device behaviour which are together responsible for its wide range of circuit applications, and which are accordingly of particular significance for circuit design.

Possibly the first thing which the reader may have realised from the foregoing description of JFET operation is that the device is one which, like the thermionic valve, is capable of **power amplification.** A small change in gate-source voltage Vgs is capable of producing a relatively large change in drain-source current Ids. Hence if a small AC signal is superimposed upon a suitable quiescent gate-source bias, an amplified AC signal can be obtained at the JFET drain electrode by placing a suitable load resistor in series with the Vds supply.

Because in normal operation its gate-source junctions are biased either only slightly in the forward direction, or more usually in the reverse direction, the JFET also has another important property in common with the thermionic valve: **high input resistance.** The only current which normally flows in the gate circuit is the junction saturation/leakage current Igss, mentioned earlier, which is typically in the order of but a few nanoamps. This gives typical devices an input resistance of around 1000 megohms.

As we observed from the static drain-source curves shown in figure 8.3, the Vds/Ids characteristics of the JFET in the pinch-off region are virtually "constant current" lines, having a very low current change/voltage change slope. In other words, then, the device resembles a pentode valve, possessing a **high output resistance.** Typical figures for JFET output resistance **rds** range from about 20K to 100K.

As with transconductance, some device manufacturers do not quote the output resistance rds on their JFET data sheets, but instead give values for **output admittance,** symbolised **Yos.** Usually this is quoted at a low frequency, say 1KHz, where its value is very close to the inverse of rds. Hence typical devices have Yos values in the range 10-50 micromhos.

Not surprisingly the depletion layers which separate the gate and channel regions of a JFET in normal operation behave as a dielectric, in this respect being no different from the depletion layer of a normal P-N junction diode. As a result there is a small but often significant capacitance between the gate and channel regions. The distribution of capacitance is naturally non-linear due to the tapering depletion layers, and also varies with the applied bias.

For convenience in circuit design the gate-channel capacitance is normally considered to consist of two main components: the **effective input capacitance** of the device as seen by the gate electrode, symbolised by **Cgs,** and the **reverse transfer or drain-gate "feedback" capacitance,** symbolised **Cdg.**

Typical modern JFET devices designed for low- and medium-frequency applications have Cgs figures ranging from 4—7pF, and Cdg figures ranging from 1—3pF. Devices intended for high frequency applications have figures somewhat lower than these.

The reverse transfer capacitance Cdg is often of particular significance for circuit design, because being coupled between the input and output of the device it can be effectively magnified in value by the familiar "Miller effect." Further discussion of this will be found in the next chapter.

The circuit symbols commonly used for JFETs of both configurations are shown in figure 8.5.

It is hoped that the foregoing discussion of the junction field-effect transistor has given the reader a basic understanding of the device and its operation. Let us now turn to consider briefly some of the other types of field-effect device in present use.

A device which is very closely related to the JFET is the so-called **constant current diode.** Although basically a very simple development from the JFET, this device is finding increasing use in many circuit applications in which current levels must be maintained despite voltage and impedance variations.

Basically the device consists of a JFET which is fitted with an "internal" self-bias resistor in series with the source, with the gate being tied to the remote end of the resistor. Figure 8.6 shows the basic arrangement, where it may be seen that only the drain and gate connections are brought out as device electrodes. These are labelled "anode" and "cathode" respectively.

As one might expect the operation of the device is again dependent upon the two basic JFET mechanisms discussed earlier. However, in this case the single bias voltage Vd applied to the device is connected directly between drain and gate, so that pinch-off simply corresponds to the situation where Vd=Vp. The pinch-off voltage is not dependent upon the value of Rs.

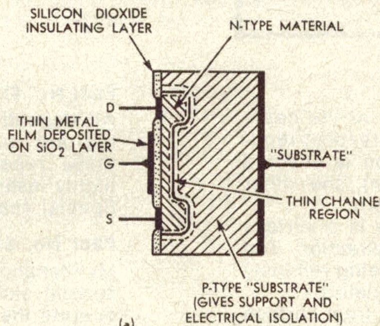


Figure 8.7 DEPLETION OR "TYPE A" MOSFET (N-CHANNEL)

The function of the resistor is to provide a "fixed" component of gate-source bias derived from the device channel current. This quite naturally has the effect of determining the value of device current at which the pinch-off plateau occurs. Thus a device fitted with no resistor might have a plateau current (in this case equal to Idss) of say 20mA, while a device fitted with a resistor of 100 ohms might have a plateau current of 10mA, as shown.

It should be fairly clear from this that the plateau current of such a device may be set to any desired value below the basic Idss for the internal structure, merely by fitting the appropriate value of resistor Rs. Hence it is possible to produce such devices with plateau currents covering quite a useful range, suitable for use in circuit applications as current regulating devices. In operation, the devices are merely arranged to operate on their pinch-off plateau, so that they tend to pass a substantially constant current despite variations in applied voltage.

No doubt the astute reader will have realised while reading the foregoing that virtually any normal JFET device could be used as a current regulating element, simply by connecting it into circuit with the source tied to the gate via a suitably chosen resistor. And in fact this forms the basis of many JFET circuit applications. However, semiconductor device manufacturers

have found it possible to provide a range of "custom-made" current regulating devices with specified current ratings, and accordingly circuit designers have been able to take advantage of the devices.

An important type of field-effect device which differs both in construction and in certain aspects of its operation from the JFET is the **insulated-gate field effect transistor, or IGFET.** Other general names for this type of device are MISFET, standing for "metal-insulator-semiconductor FET," and TFT, or "thin film transistor." The last of these names is usually reserved for devices which are in the form of elements within micro-circuits or "ICs."

In broad terms the operation of IGFET devices is very similar to that of the JFET device which we have already examined. As before, the effective conductivity of a semiconductor channel region is modulated by a control bias applied between the channel and an adjacent electrode termed the gate.

However, an important difference between the two types of device is that whereas in the JFET the gate electrode is isolated from the channel by a non-conducting P-N junction, in the IGFET this isolation is performed bv a very thin layer of insulating material such as silicon oxide or silicon nitride. Also the gate electrode is a metallic film deposited on the surface of the insulating layer, rather than a semiconductor region.

Probably the most common type of IGFET device is the **MOSFET** or **metal-oxide-semiconductor** FET, in which as the name suggests the gate-channel insulation is performed by a thin layer of silicon dioxide. Other names for this device are "MOST," "MOS transistor" and "SCOUT" — the latter standing for "surface controlled oxide unipolar transistor."

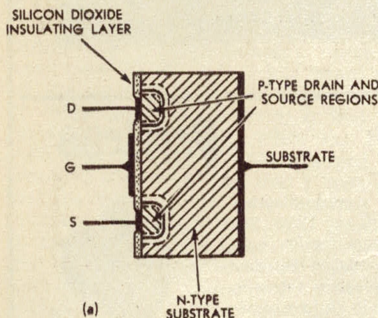
Because the MOSFET relies upon an oxide layer for gate-channel isolation rather than the depletion layers associated with non-conducting P-N junctions, it is not inherently subject to the restriction on enhancement-mode operation which applies to the JFET. There are definite restrictions to the voltage which may be applied between gate and source, as will be explained shortly, and these restrictions are of paramount importance if a MOSFET is to be protected from damage; however in general they apply equally for both polarities of applied gate-channel voltage.

Taking advantage of this, device manufacturers have been able to provide three different types of MOSFET, each of which is designed to give optimum performance under different conditions. Thus there are (a) the depletion-mode or **normally on** MOSFET, designed to operate in a very similar fashion to the JFET; (b) the depletion/enhancement MOSFET, designed for operation at around zero bias, and capable of linear signal excursions into both the depletion and enhancement modes; and (c) the enhancement-mode or **normally off** MOSFET, designed for optimum operation in the "forward-biased" condition.

The three types of MOSFET are sometimes known respectively as type "A," type "B" and type "C" devices.

The basic construction of a depletion-mode or type "A" MOSFET is shown in figure 8.7(a). It may be seen that the device channel here consists of a very thin semiconductor layer linking the drain and source regions at the surface of a supporting or "substrate" region. The device shown is of the "N-channel" variety, with an N-type channel and a P-type substrate; however the complementary configuration is also made. Like JFETs, MOSFETs can be made in both "polarities," this applying to all three types of device.

As the channel and substrate regions of the device are of opposite type, the junction between the two is surrounded by the usual depletion layer even in equilibrium. However, in this case the depletion layer plays no part in the operation of the device, serving merely as an internal isolation medium for the channel. In typical circuit applications the substrate electrode of a JFET is simply tied to the source, to earth or to some other "cold" reference point.



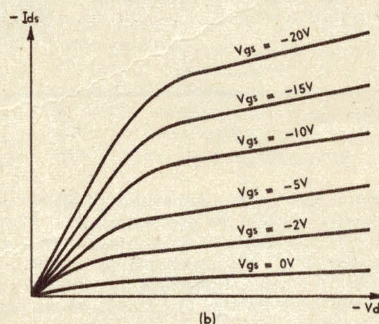


Figure 8.8 ENHANCEMENT OR "TYPE C" MOSFET (P-CHANNEL)

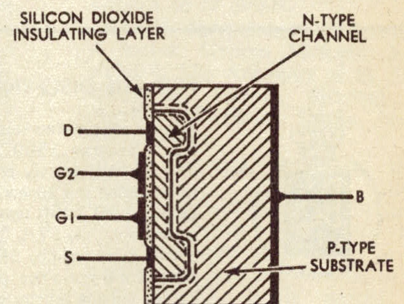
The surface of the MOSFET above the channel is covered, as may be seen, with a silicon dioxide insulating layer. The layer is very thin, typically in the order of 1,000 angstroms (.0001mM). Deposited in turn on the top of this layer, above the channel, is the gate electrode. This is simply a thin film of metal, usually aluminium.

Fairly obviously, because there is no "junction" as such between the gate and channel of the device, there can be no depletion layer at the top of the channel for zero bias, to correspond to the "equilibrium" depletion layers present in the JFET. However, the depletion mode MOSFET nevertheless operates in a very similar manner to that of the former device, as a result of the close electrical coupling between the gate and channel provided by the very thin oxide layer.

In fact although there is no depletion layer at the top of the channel for zero gate bias, such a layer begins to "grow" inwards from the top of the surface of the channel beneath the gate as soon as external reverse bias is applied to that electrode. The electric field between the gate and the semiconductor material causes carriers to be repelled from the surface, leaving a carrier-depleted region virtually identical to that associated with a P-N junction. (The repelled carriers are normally swept away by the longitudinal channel field, just as in the case of the JFET; they correspond to charging current of the gate-channel capacitance.)

As before, the encroaching depletion layer reduces the effective electrical thickness of the channel.

Not surprisingly, when gate-source bias Vgs and drain-source bias Vds are both applied, there is again a pinching action at the drain end of the channel, and channel current tends to reach a saturation or pinch-off level. Hence the depletion-type MOSFET has very similar Vds/Ids characteristics to those of a JFET, as may be seen from figure 8.7 (b). The "plateau" segments of the curves are not quite as horizontal as those of the JFET, because of the less intimate control exercised by the gate, but the behaviour of the device is very similar.



DUAL-GATE DEPLETION-TYPE MOSFET (N-CHANNEL)

Figure 8.9

In contrast with the depletion-mode MOSFET of figure 8.7 is the enhancement-mode type, whose basic construction and operation are shown in figure 8.8. The type shown is the "P-type channel" version, or more strictly the "**induced** P-type channel" configuration.

The construction of this type of device is similar to that of the depletion type, as many be seen, except that there is **no physical channel** between the two "islands" forming the drain and source regions. The substrate is continued right up to the oxide-covered surface between the two. Hence when no external gate bias is applied to the device, there can be no drain-source current except a small saturation/leakage current through the drain substrate and substrate-source junctions.

This explains why the enhancement-type MOSFET is often called a "normally off" device, in contrast with the "normally on" characteristics of the JFET and depletion-type MOSFET.

At this point the reader may well be wondering how the enhancement-type device can be persuaded to pass current. Actually the answer to this is fairly obvious — by the creation of an "effective channel" linking drain and source. And not unexpectedly, this effective channel is created at the surface of the substrate by the external bias applied to the gate electrode.

The idea is that "forward" bias applied to the gate produces an electric

field at the surface of the substrate, and this in turn has two effects. One is that majority carriers in the substrate material are repelled away from the surface; the other effect is that minority carriers are attracted towards the surface. And the net result of both these effects is that the material at the surface of the substrate is effectively **inverted in type** to become what is termed an **induced channel** linking drain and source.

Hence the example shown, forward bias (gate negative) tends to repel electrons from the surface of the N-type substrate, and at the same time attract thermally generated holes. The surface is thus inverted in type to form an induced P-type channel linking the drain and source regions, and drain-source current is able to flow if a drain-source bias Vds is applied.

Naturally the greater the forward bias applied to the gate, the deeper the induced channel and the lower the drain-source resistance. However, as before the drain-source bias Vds tends to reverse-bias the drain end of the induced channel, so that a phenomenon very similar to pinch-off occurs. Hence apart from the different gate bias sense, the Vds/Ids curves of an enhancement-type MOSFET prove rather similar to those of a depletion - type device. This may be seen by comparing the typical curves given in figure 8.8(b) with those of figure 8.7(b).

Note that in the case of the depletion-type MOSFET the gate need not extend for the full length of the channel in order to achieve proper device operation, whereas with the enhancement-type device it is essential for the gate to extend the full distance between the drain and source in order to provide a link between the two. This tends to make the enhancement-mode device harder to fabricate, and also gives it a higher gate-channel capacitance.

The depletion-enhancement or "type B" MOSFET is very similar in construction to the depletion-type device shown in figure 8.7. The only difference is that the channel section is made particularly thin, allowing the gate bias to be used either to diminish its conductivity in the manner of a depletion-type device, or to enhance its conductivity in the manner of an enhancement-type device.

A further type of MOSFET device which should be briefly mentioned here is the **dual-gate MOSFET,** which as the name suggests is a device having not one, but two control gate electrodes. The two gates are arranged to act upon the channel conductivity in cascade, as may be seen from the diagram of figure 8.9. For practical reasons associated with both the fabrication and application of such devices they are normally made in either the type A (depletion) or type B (depletion/enhancement) variety—i.e., in "normally-on" form.

The two gate electrodes of this type of device make it very well suited for use as a controlled-gain amplifier, a "cascode" RF amplifier, and an RF mixer. Thus although the device is a relatively late development on the semiconductor device scene, it is already finding many applications.

The circuit symbols commonly used for the various types of MOSFET are shown in figure 8.10.

Because of the excellent insulating properties of the silicon dioxide layer insulating the gate of a MOSFET from its channel, the input resistance of these devices is typically some 1,000 to 10,000 times greater than that of a JFET — i.e., from 1 to 10 Teraohms (1 to 10 million Megohms). This is even higher than many thermionic valves, and is, in any case, independent of the polarity of the applied gate bias — in contrast with both the JFET and the thermionic valve. At the same time the gate-channel capacitance of the MOSFET is generally somewhat lower than for the JFET, due to the isolation associated with the oxide layer, and this gives lower values for both Cgs and Cdg.

Together with these advantages come problems, however. It proves difficult to reduce the thickness of the silicon dioxide layer separating the gate electrode from the channel sufficiently to achieve as high a transconductance with MOSFETs as can be achieved fairly easily with the JFET. Very thin oxide layers are not only difficult to achieve reliably during manufacture, but they also present stability problems; their insulation becomes more subject to imperfections due to trapped impurities, and a phenomenon known as "ion drift" can occur over a period of time due to migration of impurity ions from the oxide into the semiconductor channel.

Not only this, but the silicon dioxide layer of a MOSFET does not possess the same breakdown characteristic as that of the P-N junction insulating the gate of a JFET. Whereas the latter can enter avalanche breakdown without necessarily sustaining damage, the oxide layer of a MOSFET is only capable of the "punch-through" breakdown typical of dielectrics such as paper and plastic film. Hence if a critical field strength is exceeded the gate-channel insulation is punched through at a particular point, and the device may well be ruined.

Because of the very high resistance and low capacitance between the gate and channel, even slight "static electricity" charges reaching the gate of a MOSFET can produce permanent device damage in this fashion. Hence such devices are normally supplied by the manufacturer with all electrodes temporarily shorted together to preclude static charge effects, and the electrode shorting clips are normally left connected until the devices are wired into circuit ready for operation.

Recently MOSFET devices have been released featuring "internal" protection against gate insulation failure, by means of zener diode structures incorporated into the basic device. The diodes are arranged to enter non-destructive avalanche breakdown before the oxide punch-through voltage is reached. Naturally these devices provide a form of MOSFET which is somewhat more rugged electrically than the standard type; however because the protection diode P-N junctions are effectively in parallel with the gate-channel insulation, the input resistance of these devices is lowered to the level of approximately 1000M typical of JFET devices. Luckily this figure is still very high, and quite adequate for many applications.

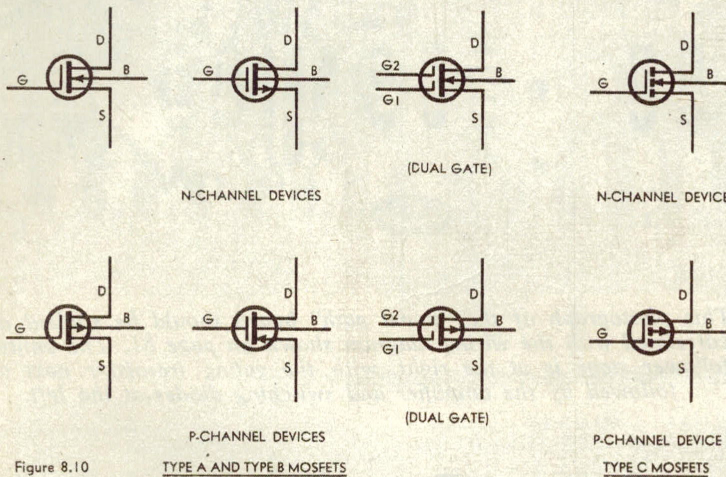


Figure 8.10

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