TATUNG

SERVICE INFORMATION

Colour Display Monitor
Type TM01

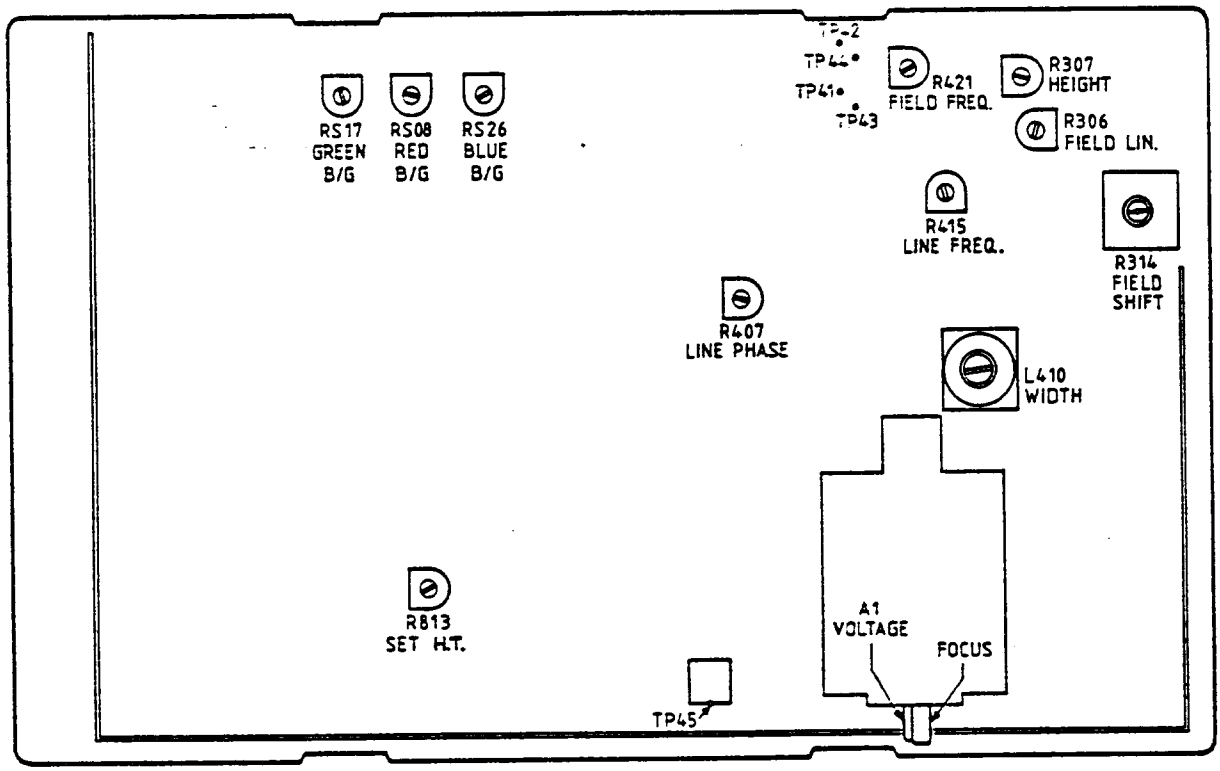


Fig. 2a - Main Chassis (component side view)

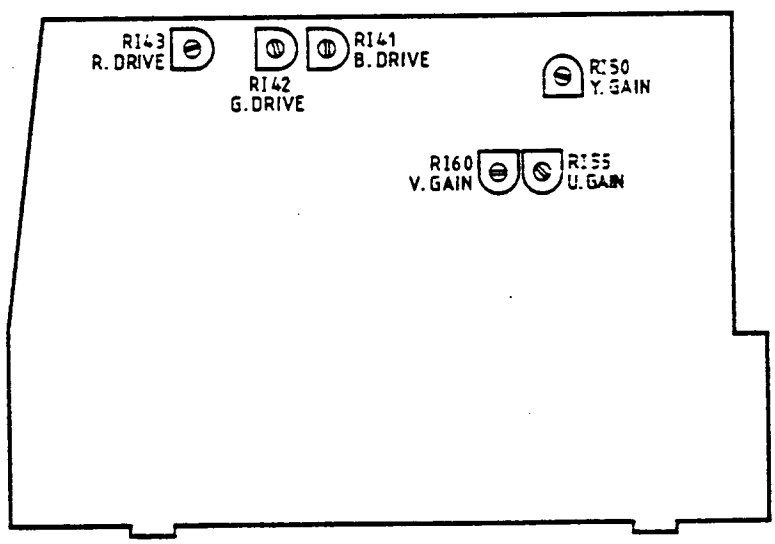


Fig. 2b - RGB/YUV Interface Panel (component side view)

3.1. CIRCUIT DESCRIPTION

The power supply is a self-oscillating switching type of converter which, under normal conditions, operates at a free-running frequency of between 20 and 30kHz. All control functions are performed within 1801 (TDA4600).

The output transistor, Q801, switches the primary winding of the transformer, T801, across the rectified mains voltage developed on the reservoir capacitor, C804. The output voltages, (121V and 18V, are generated at taps on the secondary winding and rectified and smoothed by D812, D811, C822, C826 and C821.

The base drive for Q801 is generated in I801, the current at pin 8 controlling the switch-on period and that at pin 7 controlling the turn-off conditions of Q801.

R808, R810 and C813 develop a sawtooth voltage at pin 4 which simulates the collector current of Q801. This is used to generate a sawtooth base drive at pin 8 to avoid over-saturation of Q801.

0803 and C314 rectify and smooth a voltage from the feedback winding on T801 which is proportional to the output voltages. This voltage is attenuated by R313, R312, R807 and R806 with respect to a reference voltage at pin 1 and applied to pin 3. Any changes in the output are thus transmitted via pin 3 to the control logic and the base current amplifier within the I.C. In this way the frequency and duty cycle of the output pulses are adjusted to correct for the changes.

R813 (set H.T.) adjusts the proportion of voltage fed back and hence adjusts the output vol+age. In order to complete the oscillator feedback loop R8i4 feeds an attenuated voltage from the feedback winding on T801 and pin 2. This enables the I.C. to identify the points at which the output pulse crosses the zero voltage level and so provide correctly timed base drive pulses to Q801.

The supply for the I.C. is developed by D806 and C808 from a third winding on T801. D805 and R802 provide a start-up supply for the I.C.

If an overload occurs on the 121V output voltage, the frequency and the duty cycle are reduced, thus limiting the power supplied to the load, If the overload becomes a short circuit, the frequency reduces further to 1.4kHz and the power output is limited to a low level.

3.2. VOLTAGE ADJUSTMENT

with the receiver operating with a normal picture signal, reduce the brightness control for zero beam current.

Adjust the 'Set H.T.' preset potentiometer R813 to give a meter reading of 117V at TP45, the supply voltage- to the line scan output transistor.

3.3. VOLTAGE MEASUREMENTS

Measured with a multimeter (20kOhm/V) cn low d.c. range With a normal picture displayed unless otherwise state?

Integrated Circuit I801 (TDA4600)

Rectified mains across C804 330V d.c. (iOOOV range)

IMPORTANT: All other *voltages on* I801 *and* Q801 are *measured with respect* to *the heat sink tab of I801 as a reference level for the power supply.*

Integrated Circuit 1801

Pin	V	Pin	V
1	4.4	6	0
2	0.1	7	1.8
3	*2.2*	8	1.8
4	2.2	9	16.5 (30V range)
5	6.3		

Transistor Q801 BU426A

Emitter V	Base V	Collector V
0	-0.2 (0.5V a.c.)	300 (1000V range)

4.1. CIRCUIT DESCRIPTION

4.1.1. Introduction

The generation of timebase'sync., gating, line drive pulses and field oscillator ramp are derived from 1401, (TDA2578A).

From inputs of positive going composite video, (or merely negative going sync. pulses), line flyback pulses and field output feedback, three main output signals are produced:-

(1) A line drive pulse to switch the line driver transistor Q401

(2) A field oscillator ramp voltage to drive the field output I.C., 1301

(3) A 3-level sandcastle pulse for gating, clamping, blanking and switching in the various functions required of the monitor

4.1.2. Sync. Separator

A positive going video signal, (negative going sync. pulse), is fed to Pin 5 of 1401 via a low-pass filter, R414/C411 which attenuates any colour burst and/or noise content that may be present. The sync. separator within the I.C. incorporates a noise inverter and a self-adjusting pulse slicer, to produce a constant amplitude sync. pulse train over a wide range of inputs.

4.1.3. Line Oscillator Control and Output

The pulses from the sync. separator are compared in a phase locked loop with a 15.625kHz oscillator. The free-running frequency is determined by C410, R415 and R416.

The phase locked loop has a short time constant to provide rapid locking from the out-of-sync. condition, but a coincidence detector switches the loop to a long time constant for the in-sync. state, affording excellent noise immunity. The 'flywheel' time constant is determined by the network connected to Pin 8 of the I.C.

A second control loop includes a phase detector which compares the timing of the output of the 15.625kHz oscillator, with a line flyback reference pulse coming from an auxiliary winding, (the Picture Tube heater winding), on the line scan transformer. The reference pulse is coupled to Pin 12 via C401 and R401. This loop corrects for any phase errors due to storage time variations of the line output transistor Q402. R406 provides a small amount of adjustment to the loop phase detector control stage, enabling the picture information to be centred on the raster.

The resulting output pulses are fed via an open collector output stage to Pin 11 of the I.C. from whence they are led away via the network R424/C416/R425 to switch the line driver transistor Q401.

4.1.4. Field Oscillator

Pulses from the sync. separator are fed into the vertical sync. integrator whose slice level is controlled at ?in 4 of 1401.

The output pulses are used to trigger a vertical oscillator/ sawtooth generator. The oscillator is connected to an internal comparator, the other input of which is fed with an inverted and attenuated sample of the field scan output derived from the negative feedback from 1301 and connected to 1401 at Pin 2. The error corrected output of the comparator is buffered before being led out at Pin 1.

The field oscillator ramp signal is frequency controlled at Pin 3 by R418, R419, R421, R423 and C413.

Two currents from the 121V and 25V supplies are used to charge C413 and, in this way, optimise vertical ramp linearity and minimise vertical 'breathing'.

Additional internal circuitry ensures that spurious triggering of the field oscillator, (by noise), is automatically inhibited.

1401 also embodies a circuit which detects 50/60Hz field standards and, as necessary, corrects picture height without the need for manual adjustment.

4.1.5. Sandcastle Pulse

The 15.625kHz oscillator feeds a burst gate pulse generator whose output is mixed with line flyback pulses and an internally generated field blanking pulse, (obtained by first doubling, and then dividing down from line frequency). The result is a 3-level sandcastle pulse train which is brought out at Pin 17.

4.2. SETTING-UP PROCEDURE

4.2.1. Line Frequency

If it is necessary to adjust the 15.62kHz oscillator, connect a shorting link between TP41 and Tp42, (across C411), and adjust R415 until the picture drifts slowly through horizontally, then remove the shorting link.

4.2.2. Field Frequency

If it is necessary to adjust the field oscillator, the following procedure should be adopted:

With a suitable signal applied to the monitor, turn R307, (Height), to mid. position and place shorting links between TP41 and TP42 and between TP43 and TP44, (across R419). Adjust R421, (Field Frequency), so that the unlocked picture just runs through vertically. Remcve the shorting links and reset R307 for correct height, (With the links in, the free-running. field frequency when correctly set is 46.5Hz +/-0.5Hz.

4.3. **VCLTAGE MEASUREMENTS**

Measured with a multi-meter (2OkOhms/V) with respect t0 chassis on 10V d.c. range, (unless otherwise stated), with nor-21 picture displayed.

Integrated Circuit 1401 (TDA 2578A)

Pin	Voltage (V)
1	3.5
2	Do not measure
3	4.0
4	4.5
5	3.6
6	7.1
7	4.8
a	2.6
9	0
10	12.0
11	2.6
12	1.0
13	N/C
14	2.4
15	3.7 (loss of line
16	a.2
17	1.6
18	3.0

5.1. CIRCUIT DESCRIPTION

5.1.1. Line scan

Pulses at line frequency from the sync. processor (see Sect. 4.1.3), are fed to the base of the line driver transistor, Q401. The line driver transformer secondary provides a low impedance source of pulses to switch the line output transistor, Q402.

The line scan output circuit is a conventional energy recovery type with the deflection coils and associated inductances tuned during flyback by capacitor C425. Line Linearity control is provided by saturable reactor, L408 in conjunction with the S-correction furnished by C424.

A 25V supply for the field timebase is taken from a secondary winding on the line output transformer, T402, after rectification by D404 and smoothing by C423. The fusible resistor, R434, provides protection against any short circuit faults on the 25V supply.

A further winding on T402 provides power for the picture tube heaters and a phase reference pulse to the sync. processor.

A tap on the primary winding provides a pulse voltage which is rectified by D403 and smoothed by C426 to produce a 220V supply for the video output amplifiers.

5.1.2. E.H.T.

The EHT supply to the picture tube, (24kV nominal), is produced within the line output transformer, T402, using an overwind split up into 3 main sections, each section interconnected by integral high voltage diodes.

The leakage inductance of the transformer and distributed capacitance of the overwind are tuned to harmonics of the flyback frequency in order to improve EHT regulation and minimise 'breathing' effects on the picture.

T402 also incorporates a thick film resistor network connected across the first section of the overwind. This is used to provide adjustable focus and A1 voltages for the picture tube. The focus voltage is variable from 4.3 to 7.8kV and the A1 voltage from 100 to 1000V approximately.

5.1.3. BEAM CURRENT LIMITING

The picture tube beam current flows through R433 and DS05 in opposition to the current through R427 from the 121V supply. When beam current exceeds 0.9mA, DS05 ceases conduction and the current begins to reduce the contrast control voltage at Pin 19 of II03, (the Video Control Circuit), on the Interface Panel.

At the same time, a measure of control is applied to the video preamp via DS04, DS01, DS02 and DS03.

A direct limiting action also occurs in the video amplifiers where there is a sudden large increase of beam current, (see Section .1.2).

5.2. VOLTAGE MEASUREMENTS

Measured with a multimeter (20kOhm/V) with respect to chassis on 10V d.c. range, (unless otherwise stated), with a normal picture displayed.

Transistor	Emitter V	Base V	Collector V
Q401	0	-0.25	105 (300V range)
Q402	0	-1.0 (2.1V a.c.)	Do not measure

E.H.T. MEASUREMENT

IMPORTANT NOTE:

When measuring the E.H.T. voltage, the earth return from the meter must be connected to the C.R.T. Dag or braid earthing system and NOT to the chassis rail or heat sink.

6.1. CIRCUIT DESCRIPTION

Field scan power generation is carried out by I301, (TDA3651), which includes a power amplifier and flyback generator, using a 25V supply derived from the line scan output circuit.

A field drive signal present on Pin 1 of I401 is fed to the input of I301 on Pins 1 and 3.

The scan current output is taken from Pin 5 to the field deflection coils. The current in the coils is sampled by R310 and the resulting voltage fed back via R307, (the height control), and R305 to Pin 2 of I401 in which it is compared with a signal derived from the field rate ramp on Pin 3. The resulting error correcting signal is developed on Pin 1 of I401.

The gain of the field scan amplifier is controlled by R310, R307 and R305, H.F. stability maintained by C302, C303 and C305, the D.C. operating point is established by R303 and R304 and field linearity by R306 and C304. A short flyback time is achieved by the use of a separate flyback generator within I301.

The 25V supply to the power amplifier during scan, is applied to Pin 6 via D301. During flyback the voltage is transferred through C308 to Pin 8, causing the voltage on Pin 6 to double while D301 is not conducting.

This results in a more rapid collapse of the scan coil field until the voltage across the coils falls below 25V when Pin 8 swings back to a low voltage and the whole scan cycle is repeated.

The field deflection coils are terminated via R313 and the Field Shift control, R314.

6.2. SETTING-UP PROCEDURE

Due to a degree of interaction between the field frequency and height controls, coupled with the necessity to set the field frequency accurately, the following order of adjustments are recommended:-

(1) Set R307, (Height), to mid position.

(2) Adjust R421, (Field Frequency), as detailed in Section 4.2.2.

(3) Adjust R306, (Field Linearity), for optimum linearity.

(4) Readjust R307 and recheck field freq. if necessary.

(5) Adjust R314, (Field Shift), as necessary.

6.3. VOLTAGE MEASUREMENTS

Measured with a multi-meter, (20kOhms/V), with respect to chassis on 10V D.C. range, (unless otherwise stated), and with normal picture displayed.

Integrated Circuit I301 (TDA3651)

Pin	Voltage (V)
1	1.6
2	0
3	1.6
4	0
5	13.5 (30V range)
6	28 (30V range)
7	N/C
8	5.4
9	25 (30V range)

7.1 CIRCUIT DESCRIPTION

7.1.1. Introduction

The function of the RGB/YUV Interface Panel is to interface RGB, YUV or TTL compatible data and sync. inputs to the display section of the monitor.

The heart of the interface is the Video Control Circuit II03, (TDA3505), which processes, (with internal switching), either R, G and B + sync., YUV, (actually Y, -(B-Y) and -(R-Y)), or TTL inputs, producing fully blanked, clamped and controlled outputs in the order of 2V p-p. D.C. contrast and brightness control is furnished within the I.C. for all types of input and saturation control is also provided for YUV inputs. D.C. gain control of the outputs, (R, G, and B Drive - white point adjustment), is also featured in the system.

Horizontal and vertical blanking and black-level clamping are generated within the I.C., derived from the 3-level sandcastle pulse fed to II03 from the sync. processor on the main chassis.

A block diagram of II03, (TDA3505) is shown in Fig. 7a.

7.1.2. TTL Inputs

With the 3-position selector switch, SI01, at 'TTL', (lowest position), TTL compatible R, G, B and sync. inputs are fed in at the DIN socket MI01 from whence they are fed to four Exclusive OR gates, II01 with open collector outputs. The collector load/potential divider networks RI13/RI07, RI14/RI08, RI15/RI10 and RI16/RI11 provide outputs in the order of 0.7V.

(Note: When leaving the factory II01 is connected on the assumption that the TTL inputs will conform to: R.G.B. - Active high and Sync. - Active low. However, should the users inputs be in the opposite logic, this will be inverted in II01 if links JI80 and JI81 are removed).

The R, G and B signals thus present on Pins 11, 6 and 3 of II01 are directly connected to Pins 3, 13 and 1 of the triple 2-channel transmission gate II02. Control of II02 is determined by the High or Low state of the control line connected collectively to Pins 9, 10 and 11 of the device which operates in accordance with the following table:-

Control	'On' channels (Pins)
H	3 - 4
	13 - 14
	1 - 15
L	5 - 4
	12 - 14
	2 - 15

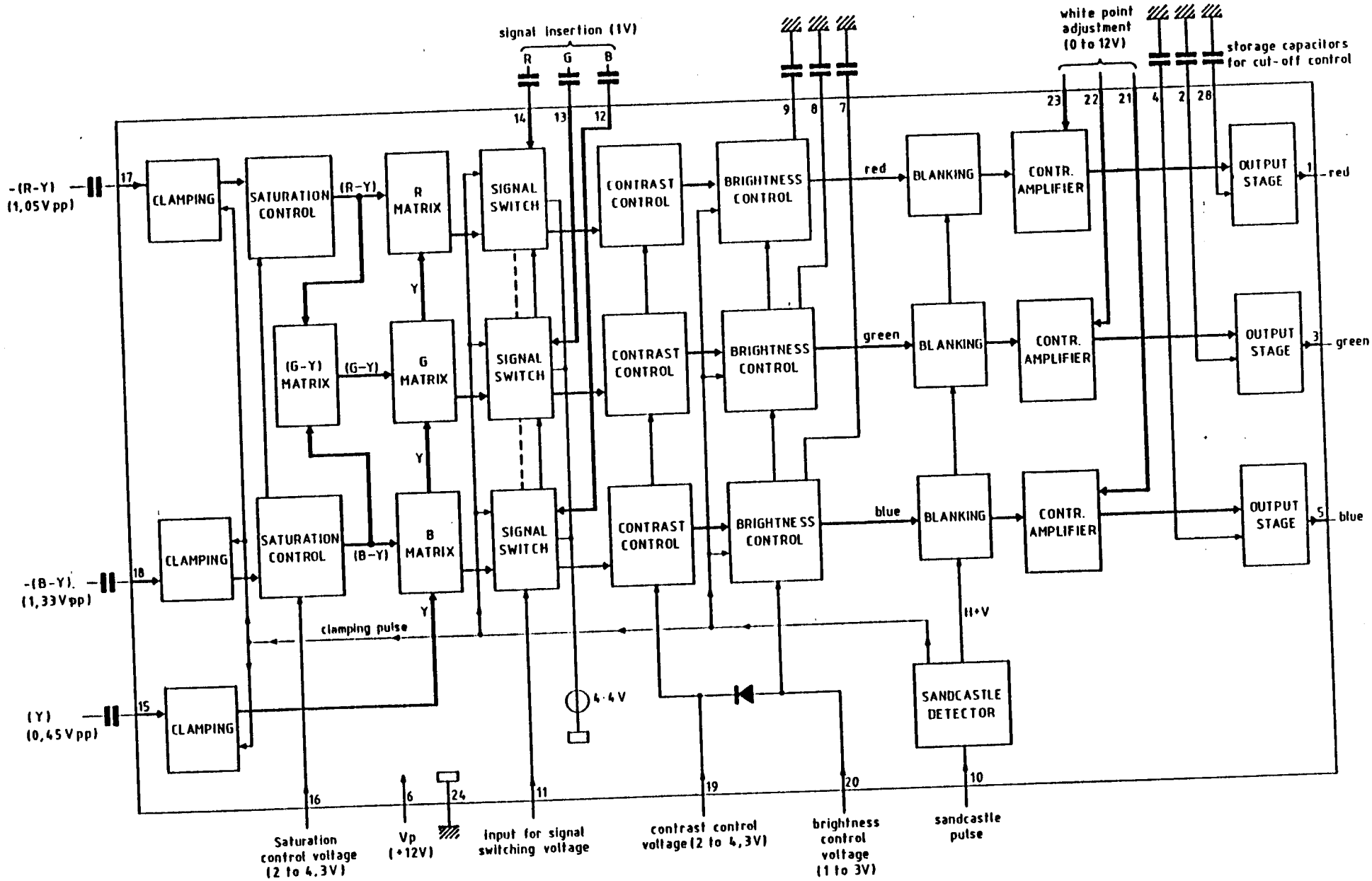


Fig. 7a - IIO3 (TDA3505) Block Diagram

Transistor QI16 activates the control line and, with SI01 in the 'TTL' position, 0V will appear on the base of QI16 causing it to conduct rendering the control line 'H'. Thus the inputs on Pins 3, 13 and 1 of II02 appear on Pins 4, 14 and 15 from whence they are fed via DC blocking capacitors CI03, CI04 and CI05 to Pins 14, 13 and 12 on II03.

After process in II03, the signals appear on Pins 1, 3 and 5 respectively and are fed via attenuating/frequency compensating networks, RI31/RI34/CI17, RI32/RI35/CI18 and RI33/RI36/CI19 to 12-way connector MI03 Pins 2, 3 and 1 and thence to the video pre-amps on the main chassis.

Meanwhile, the sync. appearing on Pin 8 of II01 is fed to Pins 5 and 4 of a 4-channel transmission gate, II05, (see Section 7.1.3 for details of operation), out at Pin 3 and via DC blocking capacitor CI41 to a non-inverting amplifier QI06/QI07. DC restoration is provided by DI12 and the sync is then routed via Pin 10 of connector MI03 to the sync. processor on the main chassis.

7.1.3. Linear (Analogue) Inputs

7.1.3.1. RGB Input

With the selector switch SI01 in the 'Linear" mode. RGB and sync. inputs are applied to DIN socket MI02. The R, G and B signals are fed via CI23, CI21 and CI22 to the bases of transistors QI03, QI01 and QI02, and the signals appearing on their emitters are connected to Pins 5, 12 and 2 of II02. With the selector switch in the 'Linear' position, QI16 is now biased off and, thus, the control line to II02 will be 'L' thereby the signals will be switched to Pins 4, 14 and 15 and thence, via the DC blocking capacitors to II03.

At the same time, the sync. input is fed via CI36 to emitter follower QI04 and from its emitter to Pin 2 of the 4-channel transmission gate II05. Inverted sync. is taken from the collector of QI04, DC blocked by CI37, detected by DI08, DC restored by DI07, reservoired by CI40 and coupled to the base of QI05. It will be seen that, whenever sync. is connected to Pin 4 of the linear signal input socket MI02, QI05 will conduct, causing the control line connected to Pin 9 of II05 to adopt an 'H' state. The second control line to II05, (Pin 10), is the same line that services II02 and is, therefore, dependent upon the position of SI01. II05 provides 'on' channels in accordance with the following table

Controls		'On' channels
Pin 9	Pin 10	(Pins)
L	L	1 - 3
L	H	5 - 3
H	L	2 - 3
H	H	4 - 3

It will be seen that in the conditions under discussion, Pin 9 will be 'H' and Pin 10 will be 'L' and that the sync. will, thus, be led from Pin 2 to Pin 3 and thence to QI06/QI07 and onwards.

(It may also be noted that in TTL operation the normal path for sync. through II05 is Pin 5 - 3, but, when TTL signals are selected and used whilst Linear RGB + Sync signals are still connected at MI02, the TTL sync. will take the alternative path, Pin 4 - 3).

7.1.3.2. YUV Input

Y, U and V signals are fed via Pins 2, 3 and 1 of DIN socket MI02 to QI01, QI02 and QI03 respectively. The Y signal, (composite video), is taken from the emitter of QI01 and fed to Pin 1 of II05. Both control lines to MI05 will be 'L', (no input on Pin 4 of MI02 and switch SI01 in 'Linear' position), thus the path through II05, Pin 1 - 3 will be established and sync. will be processed in the usual way.

The Y signal is also taken from a variable resistor, (RI50 - Y Gain) which forms the emitter load of QI01, and is fed via DC blocking capacitor CI31 to Pin 15 of II03.

Inverted U and V signals are taken from variable resistors RI55 and RI60, (U and V Gain), which form the collector loads of QI02 and QI03, and fed via DC blocking capacitors CI25 and CI26 and quad bilateral switch, II04, to II03 Pins 18 and 17 respectively.

The Quad Bilateral Switch, II04, which performs the function of burst, (or pulse) blanking, is driven by products of the sandcastle pulse generated in the sync. processor on the main chassis.

The sandcastle pulse fed from the main chassis to II03 is also fed to voltage comparators QI08/QI10 and QI13/QI14. The values of RI86/RI87 and RI97/RI98 determine the operating bias of the two comparators and, therefore, the levels at which they will slice the sandcastle pulse. QI13/QI14 is biased to select the top, (shortest) portion of the pulse whilst QI08/QI10 slices at the second (slightly longer) level. QI15 amplifies and inverts the pulse from QI13/QI14 and QI11 amplifies a non-inverted pulse from QI08/QI10.

During the line flyback period, the control lines to Pins 5 and 6 of II04 will go 'H', (pulse from QI11), connecting the transmission lines to CI28 and CI30 which will charge to reference level. Almost immediately, the control lines to Pins 12 and 13 will go 'L', (negative going pulses from QI15), temporarily disconnecting the inputs on Pins 1 and 11 from the transmission lines, thus removing any reference burst or pulse that might be present.

Transistor QI12 amplifies a non-inverted pulse from QI13/QI14 which is fed to MI03, Pin 5 and thence to the main chassis where it is used to drive the video pre-amp DC clamps QS03, QS07 and QS12.

Selector switch SI01 offers a 'Green Screen' facility on linear signal inputs by shunting the red and blue outputs with diodes DI14 and DI13 respectively.

7.2. SETTING-UP PROCEDURE

7.2.1. Equipment Required

1) An oscilloscope suitable for displaying video waveforms, bandwidth 0-15MHz sensitivity 10mV/div. with high impedance probe.

2) A suitable signal source having Linear RGB, Linear YUV and RGB TTL outputs.

3) Preset control adjusting tool.

7.2.2. Initial Conditions

Turn down the A1 voltage control Z402 to minimum, i.e. no beam current or a low beam current.

7.2.3. Setting-Up RGB Drive Pre-sets

1) Insert R.G. and B. signals having a white-black amplitude of 0.7V p-p and a Sync. signal of 0.3V p-p. (Pins 1,2,3 & 4 respectively of MI02). A white-black "staircase" signal is ideal for this purpose.

2) Adjust brightness control RI17 for mid. position and selector switch (SI01) to Linear (also mid-position).

3) Connect oscilloscope to red output, (junction RI34/CI17 and adjust RI43, (red drive) to give a white-black amplitude of 800mV.

4) Connect oscilloscope to green output, (junction RI35/CI18) and adjust RI42, (green drive) to give a white-black amplitude of 800mV.

5) Connect oscilloscope to blue output, (junction RI36/CI19), and adjust RI41, (blue drive) to give a white-black amplitude of 800mV.

NOTE: With the above procedure carried out satisfactorily, TTL inputs into MI01 and selector switch to TTL should automatically produce R. G. and B. interface outputs with a white-black amplitude of approximately 800mV.

7.2.4. Setting Up YUV Gain Pre-Sets

1) Connect a luminance signal, (positive-going video), having a white-black amplitude of 0.7V p-p and a sync. amplitude of 0.3V p-p to the Y input. (Pin 2 of MI02).

2) Connect colour difference signals having an amplitude of 0.7V p-p to the V and U inputs. (Pins 1 and 3 respectively of MI02).

3) Set user contrast control to max., brightness control to mid. position and saturation control to min.

4) Set signal source to colour bars, (or similar suitable pattern).

5) Check Pins 17 and 18 of II03 with oscilloscope to ensure that the burst pulse has been removed from the V and U signals respectively.

6) Connect the oscilloscope to the green output, (junction RI35/ CI18) and adjust RI50, (Y gain) for a white-black amplitude of 570mV.

7) Set user saturation control to mid. position.

8) Connect oscilloscope to red output and adjust RI60, (V gain), to give 100% saturation.

9) Connect oscilloscope to blue output and adjust RI55, (U gain), to give 100% saturation.

10) Set input selector switch to Green Screen and check for zero signal on red and blue outputs.

7.2.5. User Control Checks

1) Reset the A1 voltage control for correct picture grey scale (see Section 9.2.3).

2) Check that user brightness, contrast and colour controls have adequate ranges.

7.3. VOLTAGE MEASUREMENTS

Measured with a multimeter (20K ohm/V) with respect to chassis, with picture displaying colour bars at average viewing conditions.

7.3.1. Linear And TTL Mode

Transistor	Base V	Emitter V	Collector V
QI08	2.1	2.0	1.2
QI10	1.8	1.9	0
QI11	0.6	0	2.6
QI12	0.7	0	0.5
QI13	2.1	2.6	1.4
QI14	5.8	2.6	0
QI15	0		11.0

Integrated Circuit II03 (TDA3505)

Pin	V	Pin	V
1	6.6	15	2.7
2	0.3	16	2.6
3	6.6	17	2.7
4	0.3	18	2.7
5	6.6	19	1.8
6	11.6	20	1.6
7	4.1	21	6.1
8	4.1	22	6.0
9	4.2	23	5.8
10	1.6	24	0
11	1.6	25	5.1
12	3.6	26	0
13	3.6	27	2.0
14	3.8	28	0.3

7.3.2. R.G.B. (TTL) Mode

Integrated Circuit II01 (74LS136)

Pin	V	Pin	V
1	1.3	8	0.8
2	0	9	0
3	0.5	10	1.9
4	0	11	0.5
5	1.3	12	0
6	0.5	13	1.3
7	0	14	5.0

Integrated Circuit II02 (4053)

Pin	V	Pin	V
1	0.5	9	11.5
2	2.2	10	11.5
3	0.5	11	11.5
4	0.5	12	1.8
5	2.2	13	0.5
6	0	14	0.5
7	0	15	0.5
8	0	16	12.0

7.3.3. R.G.B. Linear Mode

Transistor	Base V	Emitter V	Collector V
QI04	2.2	1.7	5.8
QI05	11.0	11.5	11.5
QI16	11.5	11.5	0
QI06	2.2	1.6	9.3
QI07	9.3	10.0	2.2

Integrated Circuit II05 (4052)

Pin	V	Pin	V
1	1.8	9	11.5
2	1.7	10	0
3	1.7	11	11.5
4	0.9	12	11.5
5	0.9	13	11.5
6	0	14	11.5
7	0	15	11.5
8	0	16	11.5

7.3.4. Y.U.V. Linear Mode

Transistor	Base V	Emitter V	Collector V
QI01	2.3	1.8	11.5
QI02	2.8	2.2	6.9
QI03	2.8	2.2	7.2

Integrated Circuit II04 (4066)

Pin	V	Pin	V
1	2.7	8	2.7
2	2.7	9	2.7
3	2.7	10	2.7
4	2.7	11	2.7
5	2.7	12	11.0
6	2.7	13	11.0
7	0	14	11.5

SECTION 8 VIDEO PRE-AMPLIFIERS

8.1. CIRCUIT DESCRIPTION

Red, Green and Blue signals from the Interface Panel are fed to the pre-amplifiers via the 12-pin plug/socket MI03/MS01 at Pins 2, 3 and 1 respectively.

Taking the Red preamp as an example, the two transistors QS01 and QS02 and the surrounding components form a two-stage non-inverting amplifier with a nominal voltage gain of 6.6 determined by the values of RS03 and RS04 and with H.F. compensation provided by CS01. The amplified signal is coupled to an emitter follower by CS03 and thence to the Video Output stage via RS07.

D.C. restoration is furnished by a driven clamp QS03, (an F.E.T.), which is gated at line frequency by a pulse produced on the Interface Panel from the sandcastle pulse originating in the sync. processor. The sandcastle pulse is connected to the Interface Panel via MI03, Pin 11 and the resultant gating pulse emerges on MI03, Pin 5 whence it is coupled via the network CS02/RS05 to the gate of QS03. The source of QS03 is fed from a variable preset pot., (RS08), which is connected across the 12V supply via RS27. The drain of QS03 is coupled to the base of QS04, causing CS03 to become charged to a D.C. level consistant with the setting of RS08 which thus performs the function of background control.

Beam limiting is applied to the three preamps by DS04 and DS01 (red), DS02 (green) and DS03 (blue).

8.2. VIDEO OUTPUT ALIGNMENT PROCEDURE

8.2.1. Equipment Required

1) An oscilloscope suitable for displaying video waveforms, bandwidth 0-15MHz, sensitivity 10mV/div. with high impedance probe.
2) A good quality Linear R.G.B. colour bar signal generator.
3) Preset control adjusting tool.

8.2.2. D.C. Adjustment

1) Set user brightness control (RI17) to centre of range and select Linear on SI01.
2) Set all video drive presets RS08, RS17 and RS26 to minimum.
3) Reduce A1 control to low or zero beam current.
4) With oscilloscope connected between 'Red' video output at R906 and chassis, adjust red background (RS08) for a black level of 130V.
5) Repeat step 4 for 'Green' and 'Blue' video outputs at R907 and R908, adjusting RS17 and RS26 respectively for black levels of 130V.

8.2.3. Video Output Gains Adjustment

1) Insert R, G and B signals having a white/black amplitude of 0.7Vp-p and a sync signal of 0.3Vp-p at MI02.

2) Connect oscilloscope probe to Red video output at R906 to display waveform 202.

3) Adjust red drive RI43 located on the RGB/YUV Interface Panel to give 80V output black to white level. The blanking pulse amplitude should be approximately 35V.

4) Repeat step 3 for the 'Green' and 'Blue' video outputs (waveforms 203 and 204), adjusting RI42 and RI41 respectively to give 80V black to white.

5) Disconnect oscilloscope probe.

8.3. VOLTAGE MEASUREMENTS

Measured with a multimeter (20k Ohm/V) with respect to chassis on 10V d.c. range with picture displaying colour bars under average viewing conditions.

Transistors	Emitter V	Base V	Collector V
QS01, QS05, QS10	1.1	1.7	11.3
QS02, QS06, QS11	12.0	11.2	3.5
QS04, QS08, QS13	2.7	2.0	0

F.E.T.	Source	Drain
QS03, QS07, QS12	1.3	2.0

SECTION 9 PICTURE TUBE BASE PANEL

9.1. CIRCUIT DESCRIPTION

9.1.1. Picture Tube

The circuit panel fitted on the Picture Tube base includes the supplies to the tube electrodes with their associated components for circuit protection against possible surge effects of picture tube flashover. Integral spark gaps from all electrodes are constructed in the tube socket for connection to the external dag coating of the tube. Also included on the panel are the video amplifiers driving the red, green and blue cathodes.

The focus and A1 electrode voltages are supplied from a thick film resistance module incorporated in the diode split transformer.

9.1.2. Video Amplifiers

The three video output amplifiers, comprising Q204/Q203, Q209/208 and Q211/Q210, operate in a low dissipation mode.

Taking the red amplifier as typical, Q204 amplifies the video signal into a high value collector load, R221, which keeps the dissipation of Q204 at a comparatively low level. Since, under these conditions, the mean output impedance of the amplifier would be relatively high - rendering the signal susceptible to tube capacity loading - the signal is coupled to the C.R.T. via a low impedance buffer, (emitter follower), Q203.

During the forward-going part of the signal, Q204 conducts and drives the tube directly via the H.F. compensation inductance L201. However, as Q204 becomes turned off, its impedance is high and the collector voltage will begin to rise towards H.T. potential via D203 and R221. At the same time, the anode of D204 is held low by tube capacity under which conditions, the base of Q203 will be pulled up, providing a low impedance drive at its emitter.

For background level stability, the emitters of the video amplifier transistors Q204, Q209 and Q211 are held at a constant reference voltage determined by the conduction conditions of Q205 and Q207. These conditions are controlled by Q206 and D201 in a negative feedback loop giving a low effective D.C. and A.C. emitter impedance with temperature drift compensation.

On sudden large increases of tube beam current, a negative voltage is developed at R234. D202 conducts and takes the base voltage of Q206 negative. This turns off both Q206 and Q205 allowing the common emitter rail of the video amplifiers to 'float', causing a rapid reduction of video output and, therefore, of beam current.

9.2. GREYSCALE TRACKING

9.2.1. Equipment Required

1) R, G and B signal source giving a black/white staircase of 0.7Vp-p and a sync signal of 0.3Vp-p.

2) Preset control adjusting tool.

9.2.2. D.C. Level Adjustment

If output stage d.c. voltages are completely out of adjustment re-align as in section 8.2.

9.2.3. Background Adjustment

1) Insert R, G and B signals having a white/black amplitude of 0.7Vp-p and a sync signal of 0.3Vp-p at MI02. A monochrome staircase signal is ideal for this purpose.

2) Set user brightness (RI17) and contrast (RI20) controls to mid-position and colour control (RI22) to minimum.

3) Turn up the A1 voltage control until the black bar becomes just visible on the picture tube on one (or more) colours.

4) Adjust one or two only of the background presets RS08, RS17, RS26 corresponding to the colour(s) not illuminated to make them equally visible on the black bar.

9.2.4. Drive Adjustment

1) Adjust user contrast control (RI20) to give a normally contrasted picture.

2) If the white bars show any colouration adjust one or two only of the drive presets RI43, RI42, RI41 as appropriate to reduce the drive on the colour(s) which predominate.

3) If after a number of adjustments the results are unsatisfactory, reset the initial conditions as in paragraphs 8.2.2. and 8.2.3.

9.3. VOLTAGE MEASUREMENTS

Measured with a multi-meter (20kOhm/V) with respect to chassis with picture displaying colour bars at average viewing conditions.

9.3.1. Picture Tube Socket

Pin	Function	V.D.C.	Meter Range
5	Grids	10	30V
6	Cathode, Green	115	300V
7	A.1	450	1000V
8	Cathode, Red	115	300V
11	Cathode, Blue	115	300V

Heater voltage measured across Pins 9 and 10 is, typically, 6.1V when measured on a meter which reads true R.M.S. up to 100kHz. On a multi-meter, (10V A.C. range), the reading will be approximately 3.8V.

9.3.2. Video Amplifiers

Measured on 10V D.C. range for voltages below 10V and 300V D.C. range for voltages above 10V.

Transistors	Emitter	Base V	Collector V
Q203, Q209, Q210	115	116	205
Q201, Q209, Q212	4.2	4.8	114
Q205	4.2	3.5	0.5
Q206	0	0.6	3.5
Q207	4.2	4.8	7.5

10.1. This section illustrates the printed circuit panels with full component identification, viewed from the component side.

A simplified view of the positions of adjustable components only, will be found on Figs. 2a and 2b in Section 2.

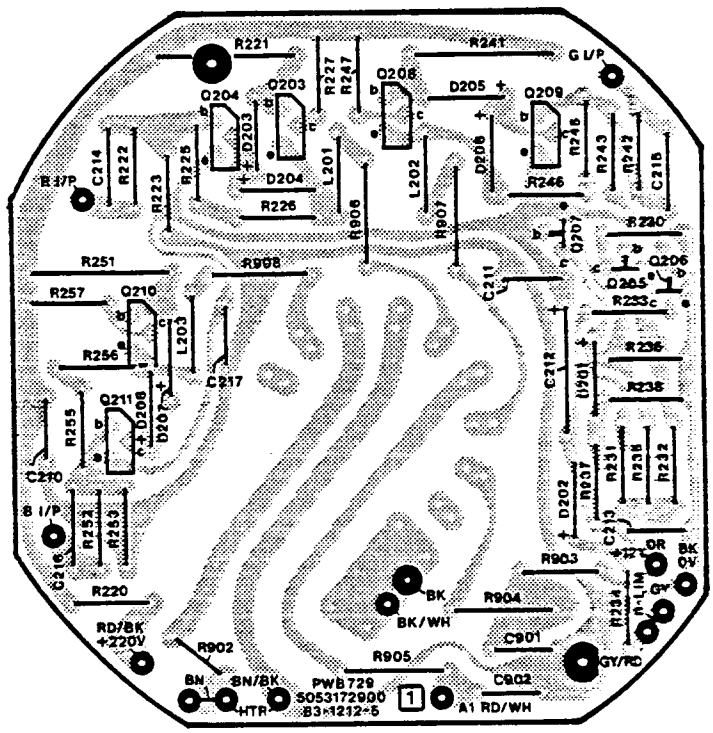


Fig. 10a - Picture Tube Base Panel

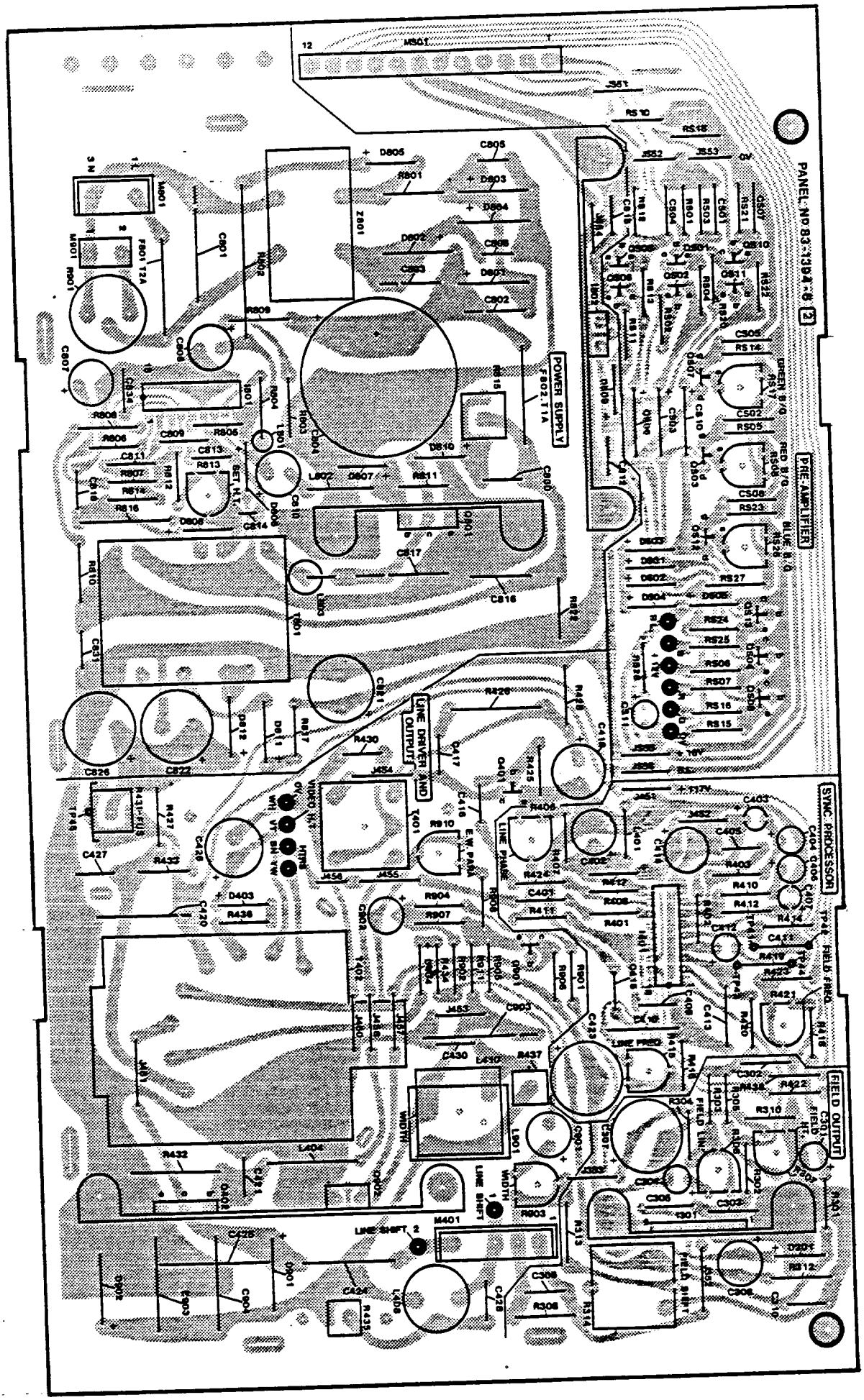


Fig. 10b - Main Panel

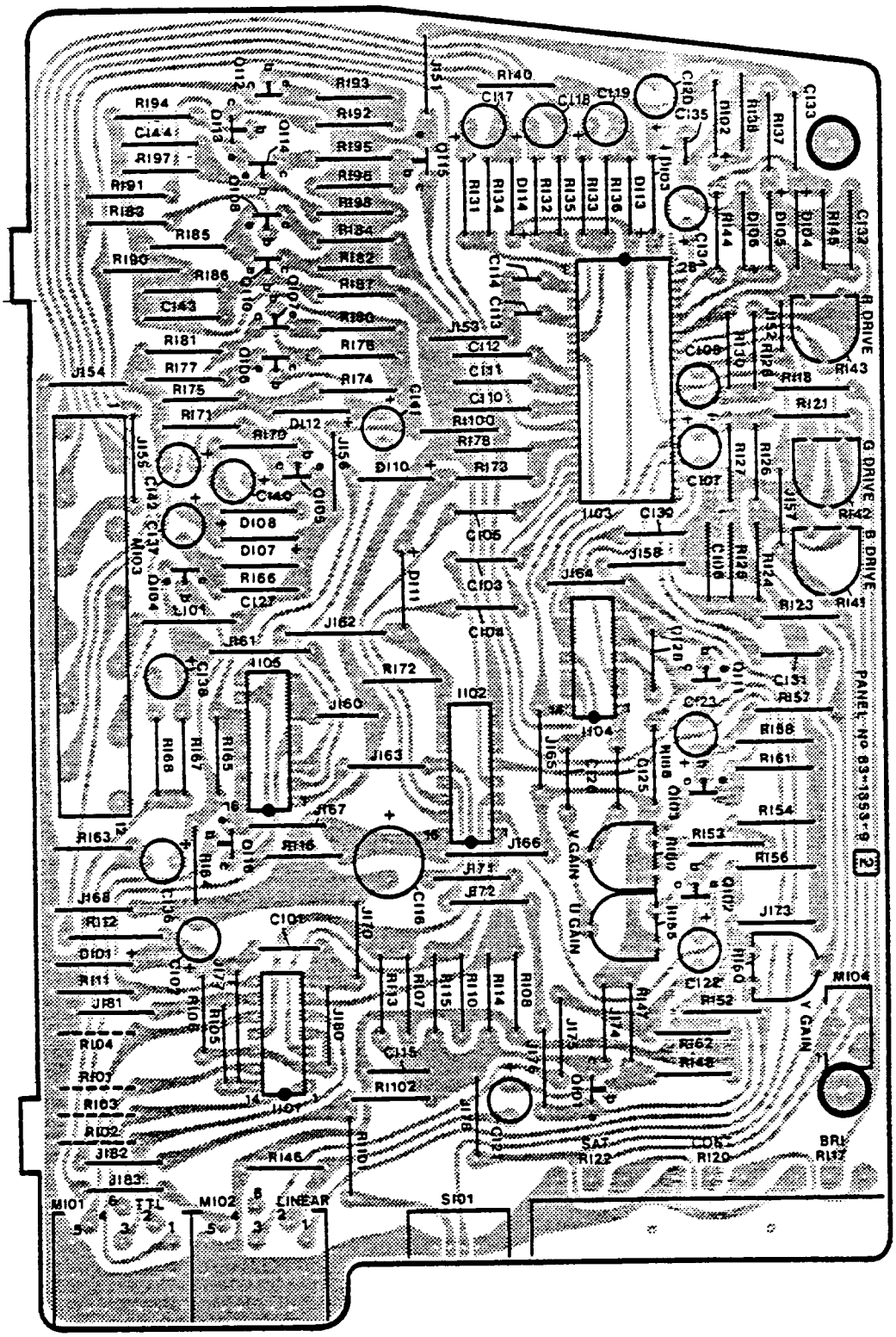


Fig. 10c - RGB/YUV Interface Panel (component side view)

ALL DIMENSIONS IN MILLIMETRES

SAFETY AND ISOLATION

Most of the circuitry on the chassis is isolated from the mains by T801, C831, R822 and a 6mm air gap. To maintain this safety factor ensure that after repair the air gap and leakage paths are not reduced by protruding wires, etc, which may exist after component replacement.

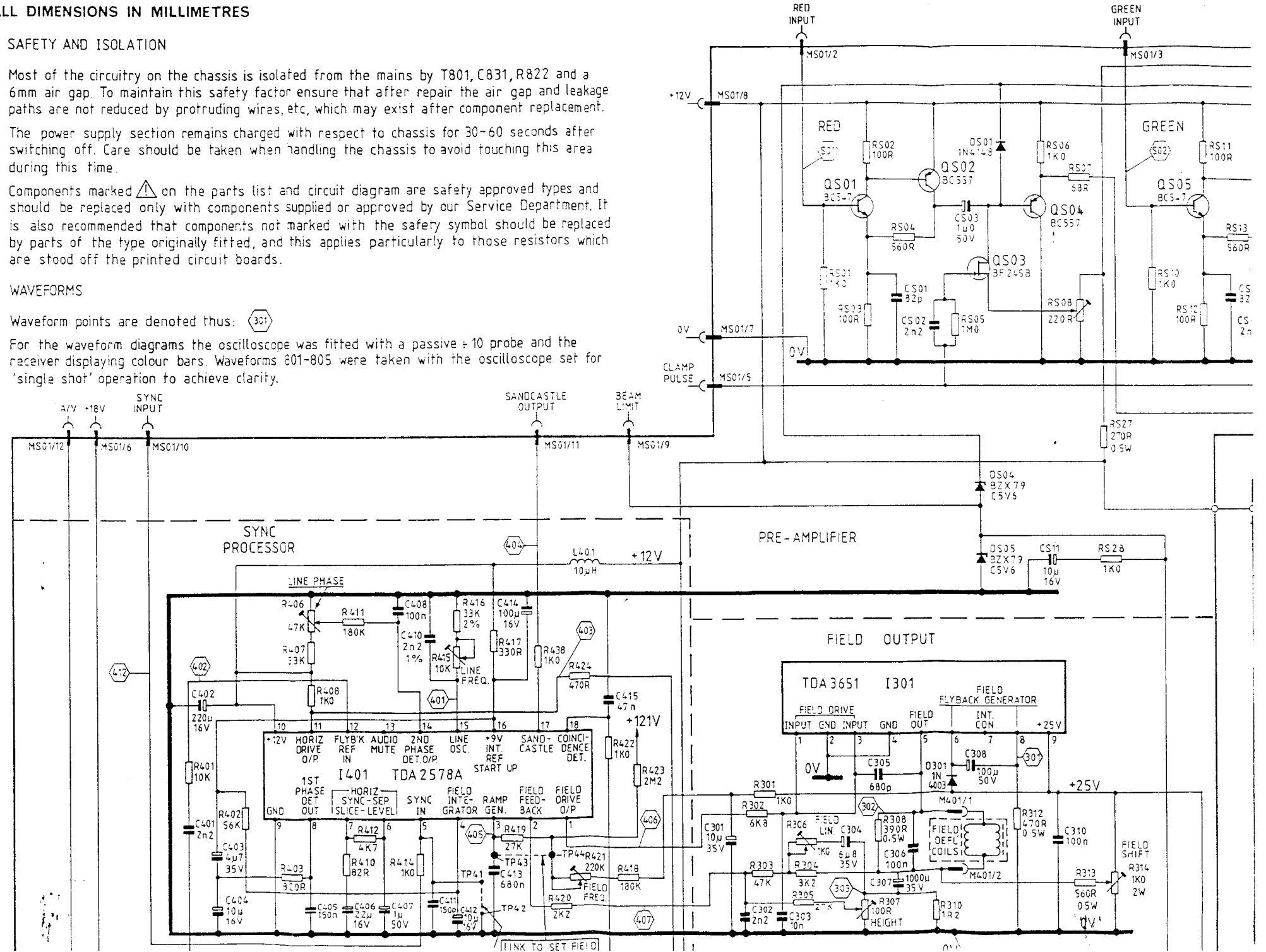
The power supply section remains charged with respect to chassis for 30-60 seconds after switching off. Care should be taken when handling the chassis to avoid touching this area during this time.

Components marked ⚠ on the parts list and circuit diagram are safety approved types and should be replaced only with components supplied or approved by our Service Department. It is also recommended that components not marked with the safety symbol should be replaced by parts of the type originally fitted, and this applies particularly to those resistors which are stood off the printed circuit boards.

WAVEFORMS

Waveform points are denoted thus: (301)

For the waveform diagrams the oscilloscope was fitted with a passive ÷10 probe and the receiver displaying colour bars. Waveforms 801-805 were taken with the oscilloscope set for 'single shot' operation to achieve clarity.



1, R822 and a
gap and leakage
ent replacement.

seconds after
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roved types and
ce Department. It
hould be replaced
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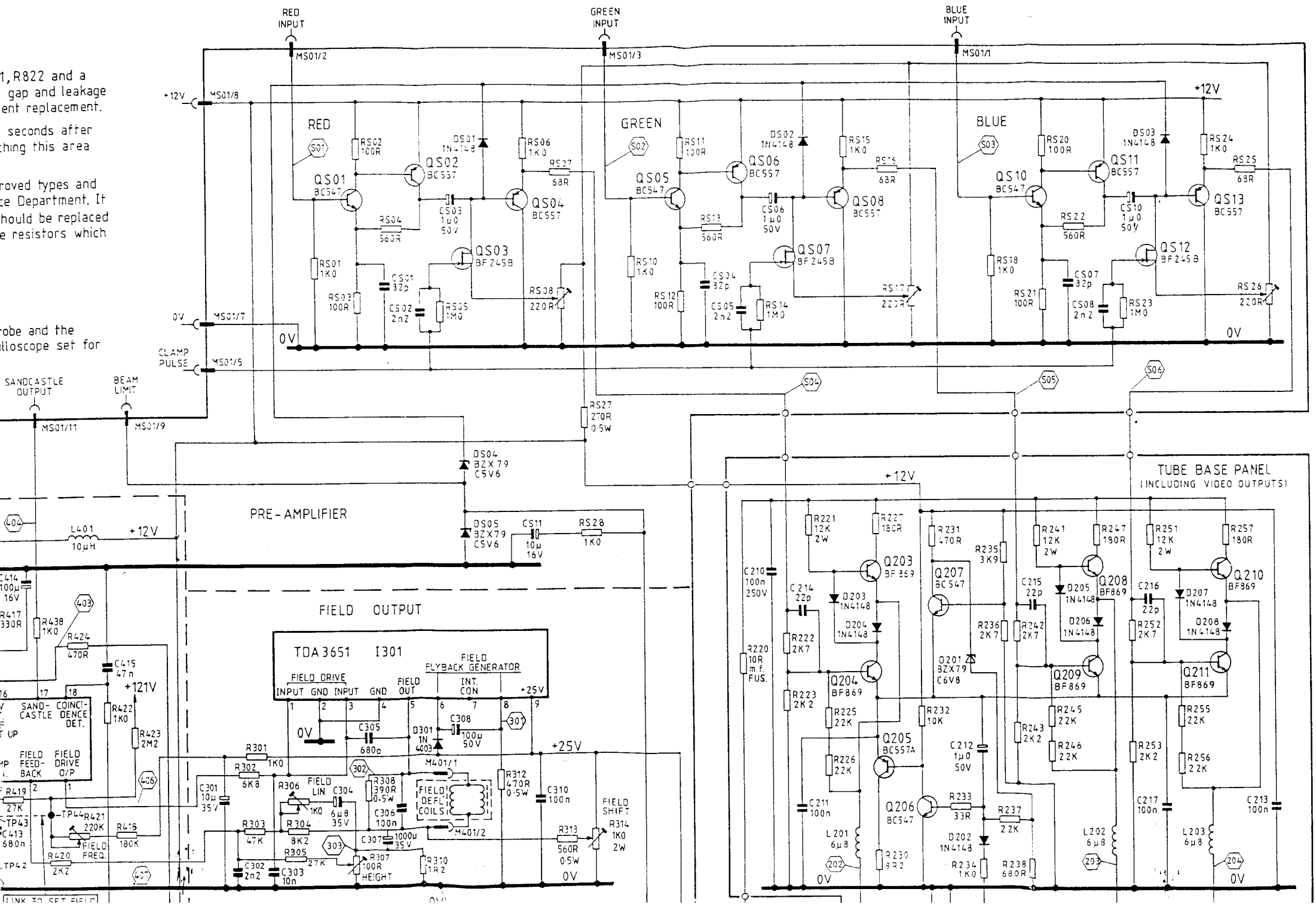
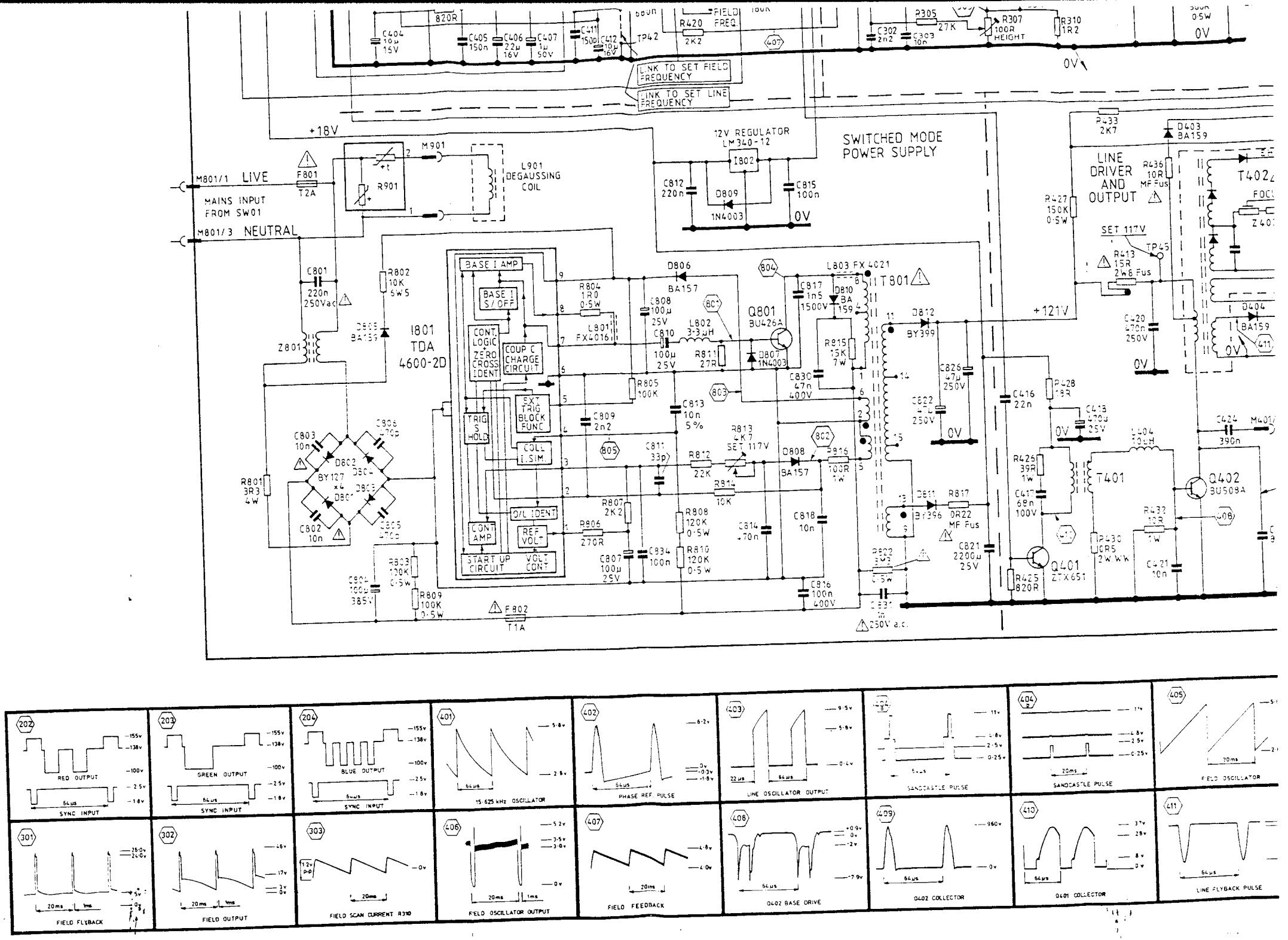
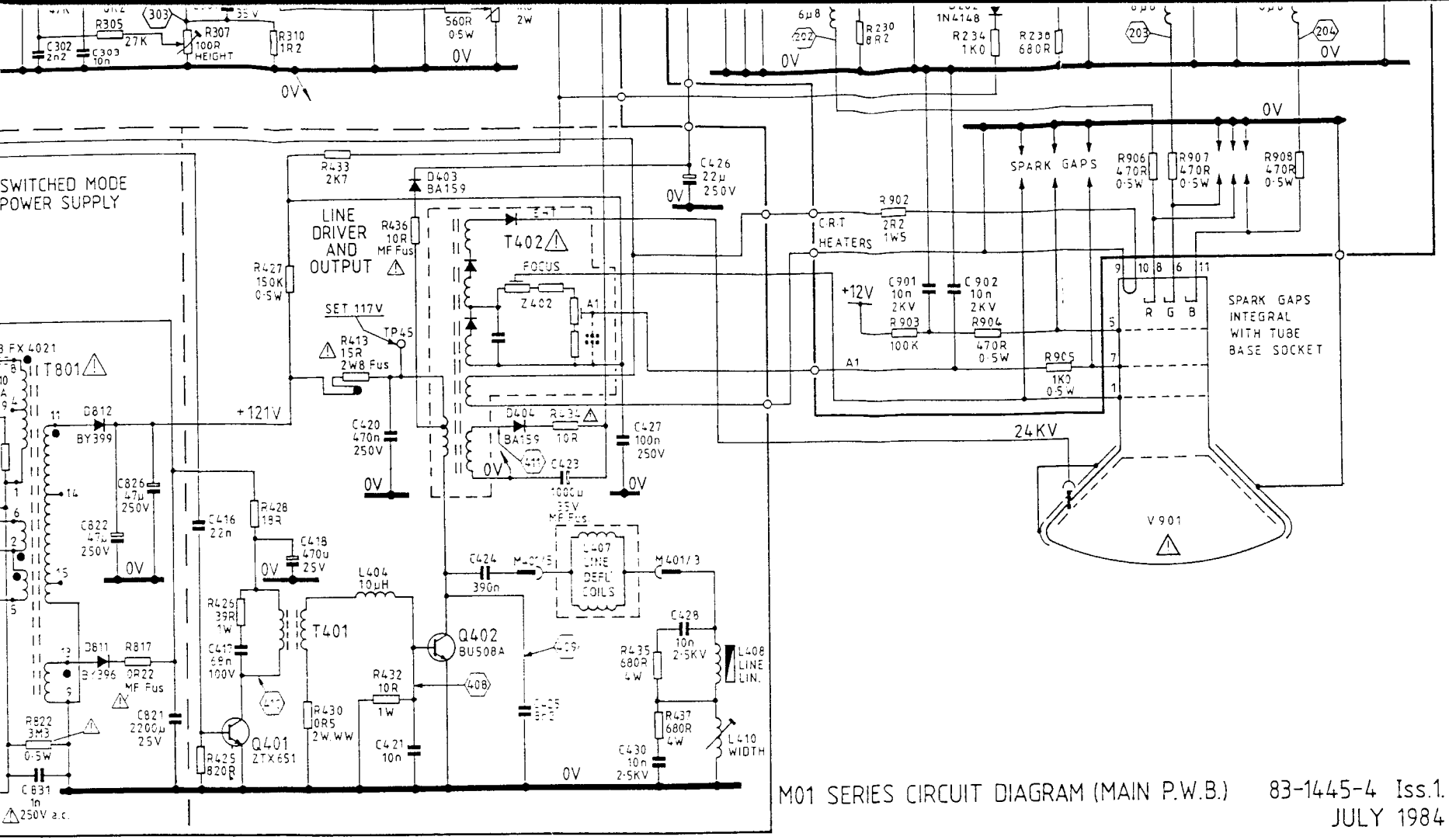
robe and the
illoscope set for




SWITCHED MODE POWER SUPPLY
+18V
M801/1 LIVE
MAINS INPUT FROM SW01
M801/3 NEUTRAL
F801 T2A
M901
R901
L901 DEGAUSSING COIL
12V REGULATOR LM340-12
I802
C812 220n
D809 1N4003
C815 100n
0V
I801 TDA 4600-2D
BASE I AMP
BASE I S/OFF
CONT. LOGIC ZERO CROSS IDENT
COUP C CHARGE CIRCUIT
EXT TRIG BLOCK FUNC
TRIG S HOLD
COLL i.SIM.
O/L IDENT
CONT AMP
REF VOLT
START UP CIRCUIT
VOLT CONT
Z801
D805 BA159
C801 220n 250Vac
R802 10K 5W5
C803 10n
C806 470p
D802 D804 BY127 x4 D803 D801
C802 10n
C805 470p
R801 3R3 4W
C804 100µ 385V
R803 130K 0·5W
R809 100K 0·5W
F802 T1A
R804 1R0 0·5W
L801 FX4016
D806 BA157
C808 100µ 25V
C810 100µ 25V
L802 3·3µH
R811 27R
D807 1N4003
Q801 BU426A
L803 FX4021
T801
C817 1n5 1500V
D810 BA 159
D812 BY399
R815 15K 7W
C830 47n 400V
C826 47µ 250V
C822 47µ 250V
0V
C809 2n2
C813 10n 5%
R805 100K
C811 33p
R812 22K
R813 4K7 SET 117V
R814 10K
D808 BA157
D816 100R 1W
C814 470n
C818 10n
R807 2K2
R806 270R
C807 100µ 25V
C834 100n
R808 120K 0·5W
R810 120K 0·5W
C816 100n 400V
D811 BY396
R817 DR22 MF Fus
C821 2200µ 25V
R802 3R3 0·5W
C831 10n
250V a.c.
R425 820R
Q401 ZTX651
R430 DR5 2W WW
R432 10R 1W
C421 10n
R426 39R 1W
C417 68n 100V
T401
L404 10µH
Q402 BU508A
C424 390n
M401
C416 22n
R428 39R
C418 470µ 25V
C420 470n 250V
+121V
LINE DRIVER AND OUTPUT
R436 10R MF Fus
R427 150K 0·5W
SET 117V
TP45
R413 15R 2W8 Fus
R433 2K7
D403 BA159
T402
D404 BA159
FOCUS
Z403
LINK TO SET FIELD FREQUENCY
LINK TO SET LINE FREQUENCY
C404 10µ 16V
820R
C405 150n
C406 22µ 16V
C407 1µ 50V
C411 150p
C412 10µ 16V
TP42
R420 2K2
FIELD FREQ
C302 2n2
C303 10n
R305 27K
R307 100R HEIGHT
R310 1R2
0·5W
0V
202 RED OUTPUT SYNC INPUT
203 GREEN OUTPUT SYNC INPUT
204 BLUE OUTPUT SYNC INPUT
401 15·625 kHz OSCILLATOR
402 PHASE REF. PULSE
403 LINE OSCILLATOR OUTPUT
404 SANDCASTLE PULSE
405 FIELD OSCILLATOR
301 FIELD FLYBACK
302 FIELD OUTPUT
303 FIELD SCAN CURRENT R310
406 FIELD OSCILLATOR OUTPUT
407 FIELD FEEDBACK
408 Q402 BASE DRIVE
409 Q402 COLLECTOR
410 Q401 COLLECTOR
411 LINE FLYBACK PULSE



M01 SERIES CIRCUIT DIAGRAM (MAIN P.W.B.) 83-1445-4 Iss.1.
JULY 1984