Advanced LCD Driver Lowers Cost of High Performance Data Projectors

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INTRODUCTION

Data projectors based on liquid crystal display (LCD) technology have made enormous strides in recent years—with smaller, lower cost units offering increased brightness and higher resolution. As a result, the projector has evolved from an installed large conference room display fixture to become an everyday tool for work groups and sales organizations, and a staple of home-entertainment systems. The DecDriver® IC, discussed here, is a major factor in present and future improvements to visual quality as well as cost reduction of these displays.

Today, the dominant technology used in projector display engines comprises three (RGB—red, green, blue) high-temperature polysilicon (HTPS) liquid crystal display (LCD) *microdisplays*. The three-color LCD microdisplays are presented with separate color data, and their light outputs are summed optically before being projected through the lens onto the screen. This system allows greater control over the color quality, with improved brightness and efficiency, and much less potential for 'color breakup' than field-sequential single-panel systems based on a rotating color wheel.

Recently, a newer LCD technology is emerging onto the projection market, based on lower cost silicon wafers—liquid crystal on silicon (LCOS). LCOS-based projection engines have the potential to enable low-cost home theater—as well as other large venue displays, such as public display and large rear-projection monitors or workstations. The benefits that LCOS microdisplays bring to these applications include higher resolutions than are presently achieved with HTPS LCD panels, combined with the potential—not yet materialized—for lower cost. Other LCOS advantages include higher pixel densities, smaller panel sizes, and higher aperture ratios. In home entertainment, the use of projector engines will include both front and rear projection—and will require resolutions in excess of 2 million full-color pixels (10-bit *gamma-corrected*—see Application Note AN-548).

Both LCOS and HTPS display technologies are LCD-based and require high-performance drive electronics to provide high-quality, high-resolution displays. (see Footnote, page 4).

The microdisplay interface differs from today's laptop displays, which are now most often *a-Si* (amorphous, active matrix LCD display). These laptop displays require an individual driver for each column of pixels. This interface is slow and the IC devices, which tend to integrate as many as 384 drivers per chip, are disproportionately long.

HTPS or LCOS *microdisplays*, on the other hand, have integrated a multiplexer (MUX) function to distribute the imaging signal among the pixel columns. The physical pixel itself serves as the load capacitance in a simple sample-and-hold circuit, which holds the imaging signal while the LCD material responds. The input of the MUX requires a greatly reduced number of interface channels, trading off increased speed for simpler circuitry. This reduces on-chip fanout to the microdisplay, which currently can measure as little as 0.5 inches along the diagonal. In addition, this configuration also reduces the power dissipation, area, and cost of the drive electronics. To top it off, while a high-end laptop display might include 8-bit drivers, the microdisplay used for projection engines today uses *10-bit* gamma-corrected inputs. Such higher quality images are needed because the projected image is so big, showing display artifacts not easily noticed on a 10-inch laptop display. The need for higher quality images and greater speed demands increased performance from the drive electronics.

Key figures of merit for these analog drivers now include good absolute output voltage *accuracy*, fast output voltage *settling* into capacitive loads, high *data rates*, compact *footprint*, and low power *dissipation*. Interface designs targeting home theater markets should continue to rely on analog inputs to the LCD microdisplays to avoid high-speed logic noise and enhance the quality of the signal applied to the display pixels.

Before the DecDriver chips came on the scene, the legacy drive electronics solution for microdisplays was based on sample-and-hold topologies to decimate the digital imaging data in time. Decimation is required to match the incoming high-speed data rate to the relatively limited bandwidth of the LCD pixel. A MUX function integrated onto the HTPS panel distributes the analog image signal across the pixel columns, loading a finite set of pixels on each clock cycle and continuing until a line of pixels fills. Sample-and-hold-based drivers suffer from several limitations that lead to poor image quality—large PCB area, limited ability to obtain resolutions greater than XGA (see Table 1, page 4), and high power dissipation. Errors in the sample-and-hold function—due to pedestal, droop, and settling time—limit the display quality of this architecture, affecting color match and hampering the system speed needed for higher resolutions. Whether or not the controller ASICs (responsible for timing, image signal processing, etc.) include high-speed video DACs, discrete video amplifiers are inherently needed to provide the necessary dynamic voltage range and settling time. They in turn drive the sample-and-hold amplifiers needed for decimating.

In addition, increasing the pixel counts—while keeping refresh rates fixed—dictates even faster drive electronics. This is particularly true of LCOS, because the faster response times and double frame rates of LCOS technology require panel interfaces with fewer (but much faster) channels than are required for HTPS.

Apart from speed issues, home theater quality LCOS displays have the same needs as HTPS. The analog inputs to the panels must have good channel-to-channel accuracy, wide dynamic range, and fast settling time.

Digitally decimated architecture

The AD8380 DecDriver (decimating driver) IC is a monolithic silicon solution that delivers all the performance needed to drive 10-bit gamma-corrected images directly onto high-resolution HTPS and LCOS panels with high speed and accuracy. It effectively replaces the sample-and-hold function by latching high-speed digital data from the controller, then transferring all channels on a given signal—thus accomplishing decimation-in-time by converting the data to parallel analog imaging signals.

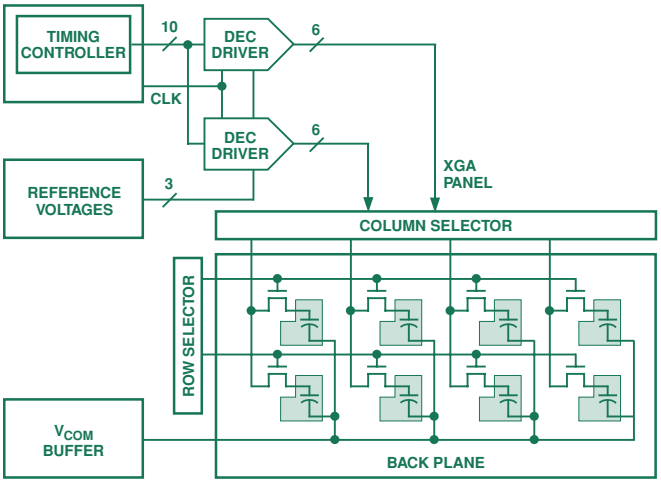

Figure 1. Simplified view of an XGA microdisplay panel driven by two DecDriver ICs.

The DecDriver is designed to optimize settling time and power dissipation by fabricating the DACs and drive amplifiers on the same chip, using a new high-density 26-V fast bipolar process. By integrating the high-voltage output drive amplifiers with the fast bipolar DACs, they can be factory-trimmed together to meet required absolute accuracy specifications.

This complete solution, designed for high output precision, also allows complete control of the imaging signal—including contrast, brightness, signal inversion, and output VCOM levels—with no sacrifice in accuracy. The combined speed, flexible logic control, and laser-trimmed output accuracy permit modular design using multiple DecDriver devices interchangeably in XGA, SXGA, and higher resolution systems.

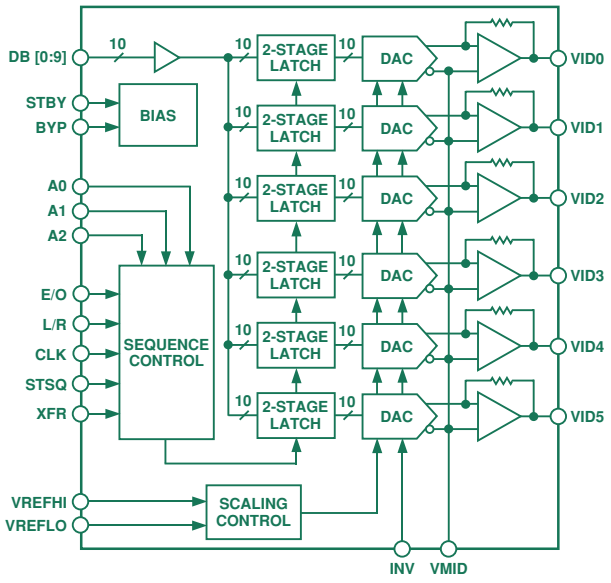

Figure 2. AD8380 DecDriver IC functional block diagram. Fast 10-bit input is latched, then passed through the DACs to output video amplifiers on XFR pulse. Output voltage levels are controlled with VREF, INV, and VMID controls.

Front- and rear-projection systems require scans in opposite directions from one another, so L/R controls are provided to determine the direction in which data is latched, making it easier to design both front- and rear-projection systems. E/O provides the ability to latch on alternate clock edges, simplifying the demultiplexing of dual high-speed data paths.

Display performance

Higher resolution displays call for higher pixel clock rates, and consequently faster drive electronics. Table 1 (page 4) shows the pixel clock and system clock rates of common video (VESA and SMPTE) formats.

Maximum assigned frequencies are 7 MHz for HTPS panels and 40 MHz for LCOS panels.

Table 2 tabulates the corresponding maximum settling times and number of required input channels of HTPS and LCOS panels with common video formats. Input data for LCOS panels is assumed frame-doubled since pixel density is too high to use column or line inversion without suffering crosstalk.

Inadequate driver operating frequency results in incompatibility with certain video formats or types of panels. A compatible driver must be able to operate at the system CLK frequency and provide the required output channels accurately within the required settling time. Excessive settling times or unmatched output channel accuracy will cause ghosting or mismatched column-to-column voltage levels, resulting in vertical lines on the image.

Accuracy

Light intensity of each color component of a given pixel depends on the driver output level, which depends on the digitally coded amplitude. Errors in D/A conversion and driver amplification in a given channel and from channel to channel and color to color lead to errors in intensity and color value; systematic errors degrade the display by producing annoying visual effects. *Absolute error* in driver outputs is proportional to rms error in the output of each driver. The absolute error specifications of the DecDriver include *all* errors: i.e., DAC nonlinearity, full-scale error, offset error, amplifier offset, and channel-matching errors.

To best correlate image artifacts and driver errors, the rms or differential error voltage, V_{DE}, (Figure 3) is defined as:

$$V_{DE}(n) = \tfrac{1}{2}\left[V_{OUTN}(n) - V_{OUTP}(n)\right] - \left[V_{FS} \times (1 - n/1023)\right]$$

where

$V_{OUTN}(n)$ is the output voltage when INV is driven high

$V_{OUTP}(n)$ is the output voltage when INV is driven low

$1/2[V_{OUTN}(n) - V_{OUTP}(n)]$ is the rms value of the output

$(V_{FS} \times (1 - n/1023))$ is the rms value of the ideal output

n is one of 2^{10} input code values

V_{FS} is the full-scale output voltage

A common-mode error (Figure 4) which shifts the transfer function away from the midpoint, V_{MID}, is defined as:

$$V_{CME}(n) = \tfrac{1}{2}\{\tfrac{1}{2}\left[V_{OUTN}(n) + V_{OUTP}(n)\right] - V_{MID}\}$$

where

$$\tfrac{1}{2}\left[V_{OUTN}(n) + V_{OUTP}(n)\right]$$

is the dc average value of the output.

Common-mode errors result in increasing crosstalk as pixel density increases (i.e., as pitch decreases).

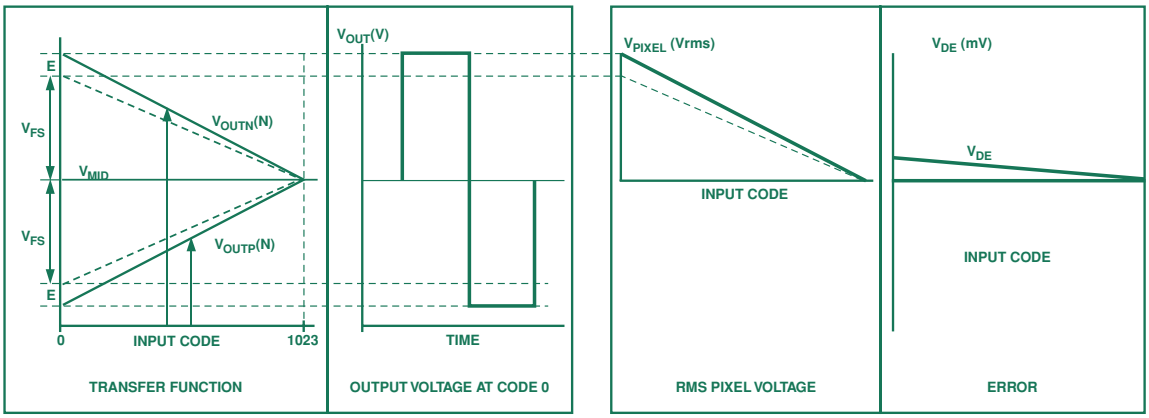

Figure 3. A typical case of V_{DE} or differential error. From left to right, plots show transfer function, time-domain rms signal at code zero, rms voltage as seen by the pixel, and the error vs. DAC code.

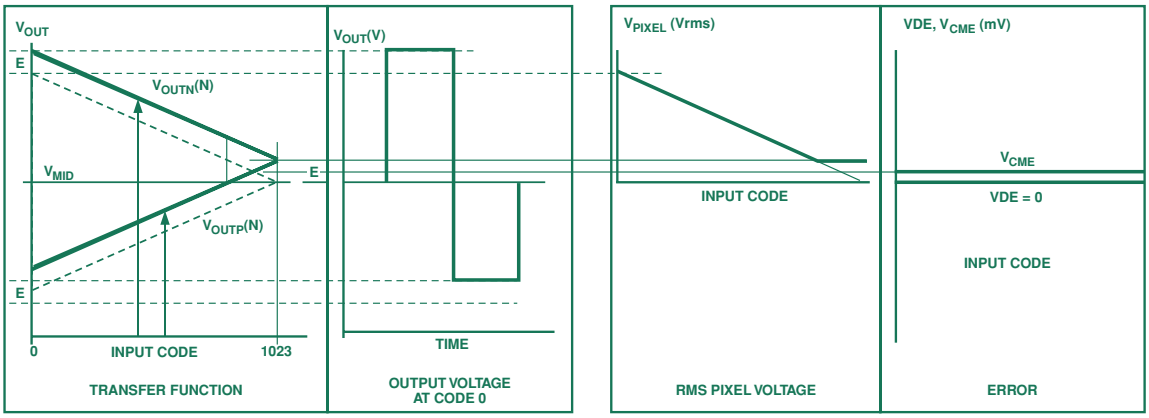

Figure 4. A typical example of V_{CME} or common-mode (offset) error. As in Figure 3, AD8380 transfer function, time-domain rms signal at code zero, rms voltage seen by the pixel, and the V_{CME} error as a function of DAC code.

Device characteristics

The AD8380, a 10-bit, 6-channel device, is the first implementation of the DecDriver architecture and is currently available in production quantity. Its analog controls adjust output reference and full-scale levels; its digital controls include Invert, Right/Left loading, Even/Odd data, and sequential- and addressed-latch loading.

It dissipates 550 mW from 15-V analog and 3.3-V digital supplies, or less than 100 mW per analog channel.

Reference inputs and logic controls foster modular design with common inputs and controls. SXGA and higher resolution projection systems have been constructed using multiple devices per color panel. Operation over the rated temperature range has been achieved with input data clock rates as high as 150 MSPS.

Maximum V_{DE} error is less than ±7.5 mV (or 1.5 gray-scale levels). As noted above, this includes all errors due to DAC nonlinearity, offset and full-scale errors, as well as amplifier gain errors. Common-mode or V_{CME} errors are less than ±3.5 mV (0.7 gray-scale levels). See Figure 5.

Output amplifier settling time (Figure 6) is typically 35 ns to 0.25% for a 5-V step into a 150-pF load. Table 2 shows that this is fast enough to drive LCOS panels with HDTV resolution.

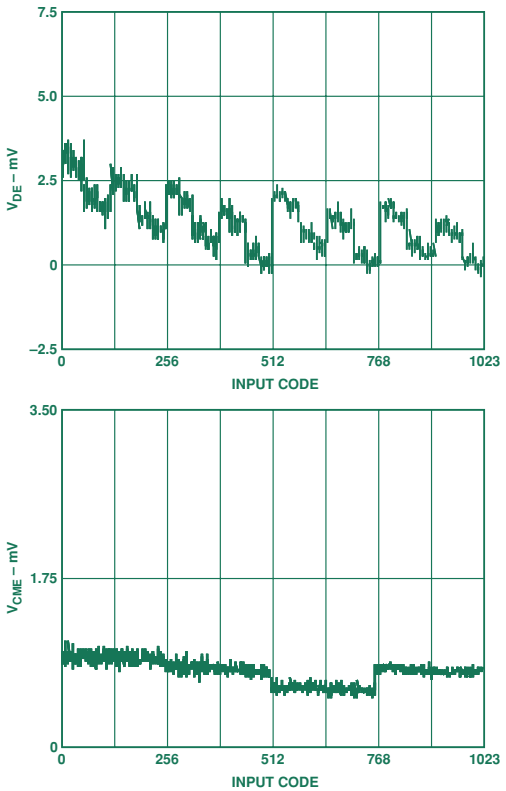

Figure 5. Typical V_{DE} and V_{CME} as functions of input code.

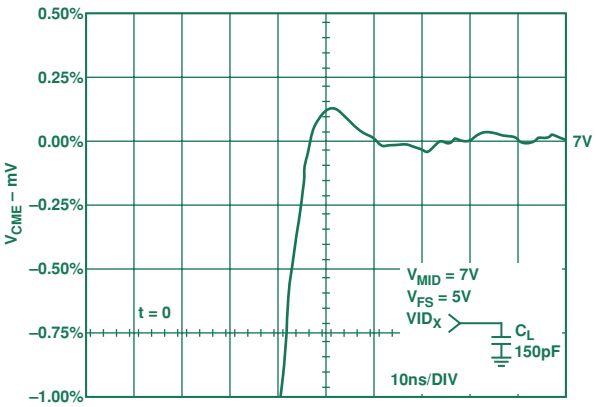

Figure 6. Typical DecDriver output settling time.

SUMMARY

In a projected image of a commercially available 12-channel XGA system using HTPS panels, no vertical lines or other image artifacts are visible. Superb color matching can be observed on such a projection system with 1000-lumen output, a significant improvement over legacy systems. The circuit footprint is reduced by elimination of external trim components between DACs integrated on the CMOS controller, gain amplifiers, and sample-holds used for de-multiplexing. Integrated control of both input logic options and output image signal levels makes the DecDriver IC a complete drive electronics subsystem, directly interfacing to both the CMOS controller and the LCD panel, with a further saving in board area. Superior dynamic performance of the integrated output drive amplifiers, coupled with fast logic inputs and output accuracy, means that multiple DecDriver ICs can be used to implement higher resolution systems for SXGA or UXGA projectors. Similar results have been demonstrated with SXGA LCOS panels—and higher resolution systems using the DecDriver architecture are in evaluation.

FOOTNOTE

About pixels, resolution, formats, clock speed, etc.

A digital video display originates with a grid of small areas each of which is briefly stimulated to produce, transmit, or reflect an individual electrically determined light intensity, which is retained during a frame's display. These areas are known as picture elements or *pixels*. A digital color display system involves three sources of pixels (red, green, blue, or RGB), whose intensities combine to illuminate the area in color. In the simplest form of *monochrome* display, the pixel areas in the top line are illuminated in horizontal sequence, then the pixels in the next line are illuminated in sequence, and so on, until the last pixel in the last line has been illuminated; then the scan starts a new *frame*.

The number of pixels per line, multiplied by the number of lines, is called the *resolution*, and the ratio of horizontal to vertical pixels is called the *aspect ratio*. In the real world, the electrical signals that control the display need time for instructions at the end of each line and at the end of each frame, so some time is allowed for additional samples. Thus, for example, in a standard computer *format* called *SVGA*, the visible display area resolution is 800 pixels per line with 600 lines per picture—but the theoretical number of possible samples is 1056 per line, and there are in effect 632 lines per frame.

To the average human visual apparatus, in order for the display to appear to provide a constant picture without flickering and to show continuous motion, the number of frames shown per second should be at least 50, and is more usually about 60. A simple calculation for this example shows that the electrical signal defining the picture must be capable of displaying with correct intensity $800 \times 600 \times 60 = 28.8$ million pixels per second and handling up to $1056 \times 632 \times 60 = 40.04$ million samples per second. This huge number is known as the *pixel clock rate*.

Table 1 compares the resolution and speed numbers for a variety of standard formats used in digital television, digitized analog TV, and computers. It also shows a key difference between computer formats and some TV formats: *interlacing*. In standard analog TV, the complete picture is displayed by two interlaced frames with half as many lines per frame; the lines of the alternate frames are interlaced to fill the display space, relying for continuity on persistence of vision. Formats retaining those vestiges require a pixel clock only half as fast as the system clock.

Table 1. Pixel clock rates for common video formats.

VIDEO DISPLAY FORMATS AND REQUIRED NUMBER OF HTPS AND LCOS CHANNELS BASED ON THE MAXIMUM DATA UPDATE FREQUENCY SUPPORTED BY THE PANEL.										INTERLACED VIDEO LINE DOUBLED
NAME	ASPECT RATIO	RESOLUTION PIXELS	LINES	SAMPLES/ LINES	LINES/ FRAME	V. RATE (Hz)	H. RATE (kHz)	PIXELS CLOCK (MHz)	SYSTEM CLOCK (MHz)
DIGITAL TV FORMAT									
HDTV 1080i	16:9	1920	1080	2200	1125	60.00	33.75	74.25	148.50
HDTC 720p	16:9	1280	720	1650	750	60.00	45.00	74.25	74.25
SDTV 480p	16:9/4:3	704	480	858	525	59.94	31.47	27.00	27.00
SDTV 480i	16:9/4:3	704	480	858	525	59.94	15.73	13.50	27.00
DIGITIZED ANALOG TV FORMATS									
NTSC 525i	4:3	640	480	858	525	59.94	15.73	13.50	27.00
PAL 625i	4:3	768	576	960	625	50.00	15.63	15.00	30.00
COMPUTER FORMATS									
VGA	4:3	640	480	800	525	60.00	31.50	25.20	25.20
SVGA	4:3	800	600	1056	632	60.00	37.92	40.04	40.04
XGA	4:3	1024	768	1343	807	60.00	48.42	65.03	65.03
SXGA	5:4	1280	1024	1688	1067	60.00	64.02	108.07	108.07
UXGA	4:3	1600	1200	2160	1250	60.00	75.00	162.00	162.00

Panels and pixels

The number of D/A conversion and driver channels required depends on the type of display and the video format. Both HTPS and LCOS require more than a single channel per color, but the slower HTPS displays require more channels, from six to as many as 24 for HDTV, SXGA, and UXGA, while LCOS displays require from two to eight channels. The 6-channel AD8380 DecDriver is designed to meet this need for driving multiple channels of 10-bit data with adequate settling time, as well as to provide many of the control functions. Table 2 indicates the channel and settling time requirements for each of the formats in Table 1.

Table 2. Maximum allowable settling times for HTPS and LCOS panels, with assumed number of channels.

VIDEO DISPLAY FORMATS	CHANNELS REQUIRED		CHANNELS USED		REQUIRED SETTLING TIME IN ns AT CHANNELS USED	
	HTPS	LCOS	HTPS	LCOS		
	f_{MAX} (MHz)		f_{MAX} (MHz)		HTPS	LCOS
NAME	7	40	7	40		
DIGITAL TV						
HDTV 1080i	21.2	7.4	24	8	162	27
HDTC 720p	10.6	3.7	12	4	162	27
SDTV 480p	3.9	1.3	6	2	222	37
SDTV 480i	3.9	1.3	6	2	222	37
DIGITIZED ANALOG TV						
NTSC 525i	3.9	1.3	6	2	222	37
PAL 625i	4.3	1.5	6	2	200	33
COMPUTER FORMATS						
VGA	3.6	1.3	6	40	238	40
SVGA	5.7	2.0	6	25	150	25
XGA	9.3	3.3	12	31	182	31
SXGA	15.4	5.4	24	37	222	37
UXGA	23.1	8.1	24	25	148	25