

BP2.3U AA
BP2.3UAA**Model-Chassis relation****Related Model-Chassis Number(s)**

The following models have been found for chassis: BP2.3UAA
Please select one of the listed chassis to fetch its related documents.

- | | | |
|---------------------|---------------------|---------------------|
| 1.
42PF7220A/37 | 4.
42PF7320A/37B | 7.
50PF7320A/37 |
| 2.
42PF7220A/37B | 5.
50PF7220A/37 | 8.
50PF7320A/37B |
| 3.
42PF7320A/37 | 6.
50PF7220A/37B | |
-

Service Service Service

BP2.1U, BP2.2U, BP2.3U

AA

Service Manual SDI Plasma Panels: 3122 785 14990



Service Manual

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PHILIPS

1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

- 1.1 Technical Specifications
- 1.2 Connection Overview
- 1.3 Chassis Overview

Notes:

- Data below can deviate slightly from the actual situation, due to the different set executions
- Specifications are indicative (subject to change).

1.1 Technical Specifications

1.1.1 Vision

Display type	: Plasma (SDI)
Screen size	: 42" (107 cm), 16:9
	: 50" (127 cm), 16:9
Resolution (HxV pixels)	: 1024(*3)x768p (42")
	: 1366(*3)x768p (50")
Min. contrast ratio	: 8000:1 (42")
	: 9000:1 (50")
Min. light output (cd/m ²)	: 900
Viewing angle (HxV degrees)	: 160x160
Tuning system	: PLL
TV Color systems	: ATSC
	: NTSC
Video playback	: NTSC
Cable	: Unscrambled digital cable - QAM
	: Digital cable ready - CableCard
Tuner bands	: VHF
	: UHF
	: S-band
	: Hyper-band
Supported video formats	: 640x480i - 1fH
	: 640x480p - 2fH
	: 720x576i - 1fH
	: 720x576p - 2fH
	: 1280x720p - 3fH
	: 1920x1080i - 2fH
Supported computer formats	: 640x480 @ 60Hz
	: 800x600 @ 60Hz
	: 1024x768 @ 60Hz
	: 1366x768 @ 60Hz

1.1.2 Sound

Sound systems	: AV Stereo
	: BTSC
Maximum power (W _{RMS})	: 2 x 15

1.1.3 Multimedia

Supported digital media	: Compact Flash I & II
	: Memory Stick
	: Microdrive (upto 2GB)
	: SD / mini SD Card
	: Multi Media Card
	: Smart Media Card
Supported file formats	: JPEG
	: MP3
	: MP3-pro
	: Slideshow (.alb)
USB input	: USB1.1 (12 Mbps)

1.1.4 Miscellaneous

Power supply:	
- Mains voltage (V _{AC})	: 100 - 240
- Mains frequency (Hz)	: 50/60
Ambient conditions:	
- Temperature range (°C)	: +5 to +40
- Maximum humidity	: 90% R.H.

Power consumption (values are indicative)

- Normal operation (W)	: ≈ 400 (42")
	: ≈ 467 (50")
- Standby (W)	: < 2

Dimensions (WxHxD in cm)	: 124x68x10.4 (42")
	: 141x78x10.4 (50")

Weight (kg/lbs)	: 42/92.6 (42")
	: 60/132.3 (50")

1.2 Connection Overview

Note: The following connector color abbreviations are used (acc. to DIN/IEC 757): Bk= Black, Bu= Blue, Gn= Green, Gy= Grey, Rd= Red, Wh= White, and Ye= Yellow.

1.2.1 Side Connections

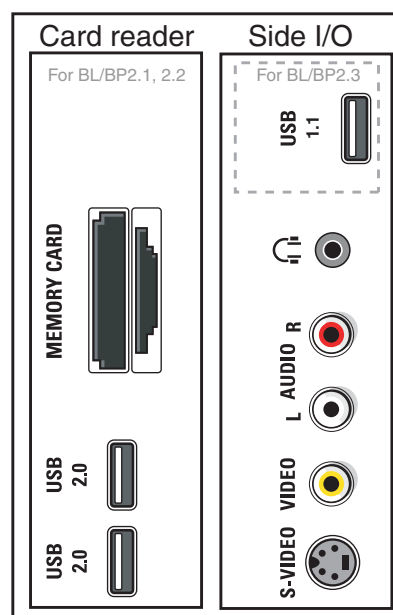


Figure 1-1 Side I/O connections

USB

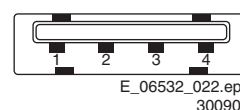
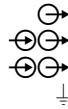


Figure 1-2 USB (type A)

- | | | |
|---|------------|-----|
| 1 | - +5V | |
| 2 | - Data (-) | |
| 3 | - Data (+) | |
| 4 | - Ground | Gnd |



Mini Jack: Audio Headphone - Out

Bk - Headphone 32 - 600 ohm / 10 mW



Cinch: Video CVBS - In, Audio - In

Ye	- Video CVBS	1 V _{PP} / 75 ohm
Wh	- Audio L	0.5 V _{RMS} / 10 kohm
Rd	- Audio R	0.5 V _{RMS} / 10 kohm



S-Video (Hosiden): Video Y/C - In

1	- Ground Y	Gnd
2	- Ground C	Gnd
3	- Video Y	1 V _{PP} / 75 ohm
4	- Video C	0.3 V _{PP} / 75 ohm



1.2.2 Digital Media Reader with USB2.0 (not for BP2.3)

In some versions, a 6-in-1 card reader unit is available, which is connected via USB to the Small Signal Board (see also par. "Technical Specifications" -> "Multimedia"). This unit also contains two USB2.0 connectors (see figure rear connections).

1.2.3 Rear Connections (under side)

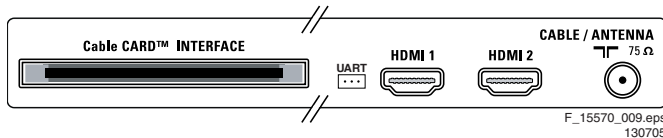


Figure 1-3 Rear connections (under side)

POD: CableCARD Interface

68p - See diagram B10A



Service Connector (UART)

1	- UART_TX	Transmit
2	- Ground	Gnd
3	- UART_RX	Receive



HDMI 1 & 2: Digital Video, Digital Audio - In

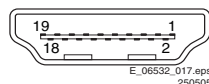


Figure 1-4 HDMI (type A) connector

1	- D2+	Data channel
2	- Shield	Gnd
3	- D2-	Data channel
4	- D1+	Data channel
5	- Shield	Gnd
6	- D1-	Data channel
7	- D0+	Data channel
8	- Shield	Gnd
9	- D0-	Data channel
10	- CLK+	Data channel
11	- Shield	Gnd
12	- CLK-	Data channel
13	- n.c.	
14	- n.c.	
15	- DDC_SCL	DDC clock
16	- DDC_SDA	DDC data
17	- Ground	Gnd
18	- +5V	
19	- HPD	Hot Plug Detect



20 - Ground Gnd

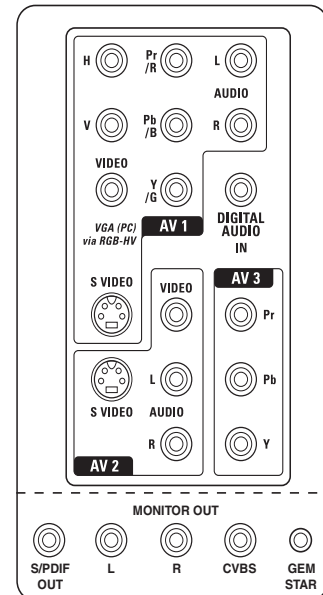


Aerial - In

- - F-type (US) Coax, 75 ohm



1.2.4 Rear Connections (rest)



F_15400_001.eps
130705

Figure 1-5 Rear connections (rest)

AV1 Cinch: Video YPbPrHV- In

Gn	- Video Y	1 V _{PP} / 75 ohm
Bu	- Video Pb	0.7 V _{PP} / 75 ohm
Rd	- Video Pr	0.7 V _{PP} / 75 ohm
Bk	- H-sync	0 - 5 V
Bk	- V-sync	0 - 5 V



AV1 Cinch: Video CVBS - In, Audio - In

Ye	- Video CVBS	1 V _{PP} / 75 ohm
Wh	- Audio L	0.5 V _{RMS} / 10 kohm
Rd	- Audio R	0.5 V _{RMS} / 10 kohm



DIGITAL AUDIO Cinch: S/PDIF - In

Bk - Coaxial 0.2 - 0.6V_{PP} / 75 ohm



AV1 S-Video (Hosiden): Video Y/C - In

1	- Ground Y	Gnd
2	- Ground C	Gnd
3	- Video Y	1 V _{PP} / 75 ohm
4	- Video C	0.3 V _{PP} / 75 ohm



AV2 S-Video (Hosiden): Video Y/C - In

1	- Ground Y	Gnd
2	- Ground C	Gnd
3	- Video Y	1 V _{PP} / 75 ohm
4	- Video C	0.3 V _{PP} / 75 ohm



AV2 Cinch: Video CVBS - In, Audio - In

Ye	- Video CVBS	1 V _{PP} / 75 ohm
Wh	- Audio L	0.5 V _{RMS} / 10 kohm
Rd	- Audio R	0.5 V _{RMS} / 10 kohm



AV3 Cinch: Video YPbPr - In

Rd	- Video Pr	0.7 V _{PP} / 75 ohm
Bu	- Video Pb	0.7 V _{PP} / 75 ohm
Gn	- Video Y	1 V _{PP} / 75 ohm



DIGITAL AUDIO Cinch: S/PDIF - Out

Bk - Coaxial 0.4 - 0.6V_{PP} / 75 ohm ⊕⊙

MONITOR OUT Cinch: Video CVBS - Out, Audio - Out

Ye - Video CVBS 1 V_{PP} / 75 ohm ⊕⊙
Wh - Audio L 0.5 V_{RMS} / 10 kohm ⊕⊙
Rd - Audio R 0.5 V_{RMS} / 10 kohm ⊕⊙

GEMSTAR Mini Jack: Remote Control - In/Out

1	- Ground	Gnd	⊕
2	- RXD		⊕
3	- TXD		⊕
4	- IR-OUT		⊕
5	- RXD		⊕

1.3 Chassis Overview

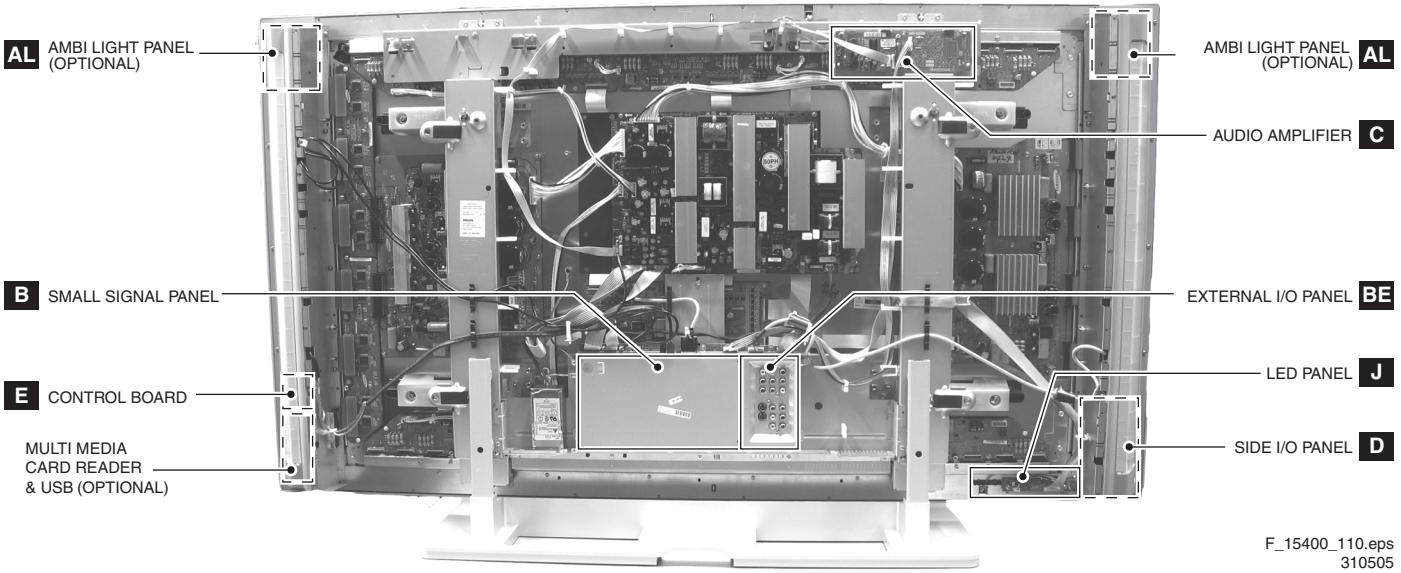


Figure 1-6 PWB/CBA locations

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

- 2.1 Safety Instructions
- 2.2 Warnings
- 2.3 Notes

2.1 Safety Instructions

Safety regulations require that **during** a repair:

- Connect the set to the Mains/AC Power via an isolation transformer (> 800 VA).
- Replace safety components, indicated by the symbol ▲, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that **after** a repair, the set must be returned in its original condition. Pay in particular attention to the following points:

- Route the wire trees correctly and fix them with the mounted cable clamps.
- Check the insulation of the Mains/AC Power lead for external damage.
- Check the strain relief of the Mains/AC Power cord for proper function.
- Check the electrical DC resistance between the Mains/AC Power plug and the secondary side (only for sets which have a Mains/AC Power isolated power supply):
 1. Unplug the Mains/AC Power cord and connect a wire between the two pins of the Mains/AC Power plug.
 2. Set the Mains/AC Power switch to the "on" position (keep the Mains/AC Power cord unplugged!).
 3. Measure the resistance value between the pins of the Mains/AC Power plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between 4.5 Mohm and 12 Mohm.
 4. Switch "off" the set, and remove the wire between the two pins of the Mains/AC Power plug.
- Check the cabinet for defects, to avoid touching of any inner parts by the customer.

2.2 Warnings

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD ▲). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential. Available ESD protection equipment:
 - Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
 - Wristband tester 4822 344 13999.
- Be careful during measurements in the high voltage section.
- Never replace modules or other components while the unit is switched "on".
- When you align the set, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

2.3 Notes

2.3.1 General

- Measure the voltages and waveforms with regard to the chassis (= tuner) ground (\perp), or hot ground (\rightarrow), depending on the tested area of circuitry. The voltages and waveforms shown in the diagrams are indicative. Measure them in the

Service Default Mode (see chapter 5) with a color bar signal and stereo sound (L: 3 kHz, R: 1 kHz unless stated otherwise) and picture carrier at 475.25 MHz for PAL, or 61.25 MHz for NTSC (channel 3).

- Where necessary, measure the waveforms and voltages with (⏏) and without (⏏) aerial signal. Measure the voltages in the power supply section both in normal operation (⏏) and in stand-by (⏏). These values are indicated by means of the appropriate symbols.
- The semiconductors indicated in the circuit diagram and in the parts lists, are interchangeable per position with the semiconductors in the unit, irrespective of the type indication on these semiconductors.
- Manufactured under license from Dolby Laboratories. "Dolby", "Pro Logic" and the "double-D symbol", are trademarks of Dolby Laboratories.

2.3.2 Schematic Notes

- All resistor values are in ohms and the value multiplier is often used to indicate the decimal point location (e.g. 2K2 indicates 2.2 kohm).
- Resistor values with no multiplier may be indicated with either an "E" or an "R" (e.g. 220E or 220R indicates 220 ohm).
- All capacitor values are given in micro-farads (μ = $\times 10^{-6}$), nano-farads (n= $\times 10^{-9}$), or pico-farads (p= $\times 10^{-12}$).
- Capacitor values may also use the value multiplier as the decimal point indication (e.g. 2p2 indicates 2.2 pF).
- An "asterisk" (*) indicates component usage varies. Refer to the diversity tables for the correct values.
- The correct component values are listed in the Spare Parts List. Therefore, always check this list when there is any doubt.

2.3.3 Rework on BGA (Ball Grid Array) ICs

General

Although (LF)BGA assembly yields are very high, there may still be a requirement for component rework. By rework, we mean the process of removing the component from the PWB and replacing it with a new component. If an (LF)BGA is removed from a PWB, the solder balls of the component are deformed drastically so the removed (LF)BGA has to be discarded.

Device Removal

As is the case with any component that, it is essential when removing an (LF)BGA, the board, tracks, solder lands, or surrounding components are not damaged. To remove an (LF)BGA, the board must be uniformly heated to a temperature close to the reflow soldering temperature. A uniform temperature reduces the chance of warping the PWB. To do this, we recommend that the board is heated until it is certain that all the joints are molten. Then carefully pull the component off the board with a vacuum nozzle. For the appropriate temperature profiles, see the IC data sheet.

Area Preparation

When the component has been removed, the vacant IC area must be cleaned before replacing the (LF)BGA. Removing an IC often leaves varying amounts of solder on the mounting lands. This excessive solder can be removed with either a solder sucker or solder wick. The remaining flux can be removed with a brush and cleaning agent.

After the board is properly cleaned and inspected, apply flux on the solder lands and on the connection balls of the (LF)BGA.

Note: Do not apply solder paste, as this has shown to result in problems during re-soldering.

Device Replacement

The last step in the repair process is to solder the new component on the board. Ideally, the (LF)BGA should be aligned under a microscope or magnifying glass. If this is not possible, try to align the (LF)BGA with any board markers. So as not to damage neighboring components, it may be necessary to reduce some temperatures and times.

More Information

For more information on how to handle BGA devices, visit this URL: www.atyourservice.ce.philips.com (needs subscription, not available for all regions). After login, select "Magazine", then go to "Workshop Information". Here you will find Information on how to deal with BGA-ICs.

2.3.4 Lead Free Solder

Philips CE is producing lead-free sets (PBF) from 1.1.2005 onwards.

Identification: The bottom line of a type plate gives a 14-digit serial number. Digits 5 and 6 refer to the production year, digits 7 and 8 refer to production week (in example below it is 1991 week 18).



E_06532_024.eps
230205

Figure 2-1 Serial number example

Regardless of the special lead-free logo (which is not always indicated), one must treat all sets from this date onwards according to the rules as described below.



Figure 2-2 Lead-free logo

Due to lead-free technology some rules have to be respected by the workshop during a repair:

- Use only lead-free soldering tin Philips SAC305 with order code 0622 149 00106. If lead-free solder paste is required, please contact the manufacturer of your soldering equipment. In general, use of solder paste within workshops should be avoided because paste is not easy to store and to handle.
- Use only adequate solder tools applicable for lead-free soldering tin. The solder tool must be able
 - To reach at least a solder-tip temperature of 400°C.
 - To stabilize the adjusted temperature at the solder-tip.
 - To exchange solder-tips for different applications.
- Adjust your solder tool so that a temperature around 360°C - 380°C is reached and stabilized at the solder joint. Heating time of the solder-joint should not exceed ~ 4 sec. Avoid temperatures above 400°C, otherwise wear-out of tips will rise drastically and flux-fluid will be destroyed. To avoid wear-out of tips, switch "off" unused equipment or reduce heat.
- Mix of lead-free soldering tin/parts with leaded soldering tin/parts is possible but PHILIPS recommends strongly to

avoid mixed regimes. If not to avoid, clean carefully the solder-joint from old tin and re-solder with new tin.

- Use only original spare-parts listed in the Service-Manuals. Not listed standard material (commodities) has to be purchased at external companies.
- Special information for lead-free BGA ICs: these ICs will be delivered in so-called "dry-packaging" to protect the IC against moisture. This packaging may only be opened short before it is used (soldered). Otherwise the body of the IC gets "wet" inside and during the heating time the structure of the IC will be destroyed due to high (steam-)pressure inside the body. If the packaging was opened before usage, the IC has to be heated up for some hours (around 90°C) for drying (think of ESD-protection!).
Do not re-use BGAs at all!
- For sets produced before 1.1.2005, containing leaded soldering tin and components, all needed spare parts will be available till the end of the service period. For the repair of such sets nothing changes.

In case of doubt whether the board is lead-free or not (or with mixed technologies), you can use the following method:

- Always use the highest temperature to solder, when using SAC305 (see also instructions below).
- De-solder thoroughly (clean solder joints to avoid mix of two alloys).

Caution: For BGA-ICs, you **must** use the correct temperature-profile, which is coupled to the 12NC. For an overview of these profiles, visit the website www.atyourservice.ce.philips.com (needs subscription, but is not available for all regions) You will find this and more technical information within the "Magazine", chapter "Workshop information". For additional questions please contact your local repair help desk.

2.3.5 Practical Service Precautions


- **It makes sense to avoid exposure to electrical shock.** While some sources are expected to have a possible dangerous impact, others of quite high potential are of limited current and are sometimes held in less regard.
- **Always respect voltages.** While some may not be dangerous in themselves, they can cause unexpected reactions that are best avoided. Before reaching into a powered TV set, it is best to test the high voltage insulation. It is easy to do, and is a good service precaution.

3. Directions for Use

You can download this information from the following websites:
<http://www.philips.com/support>
<http://www.p4c.philips.com>


As the software upgrade is a new feature, it is explained below.

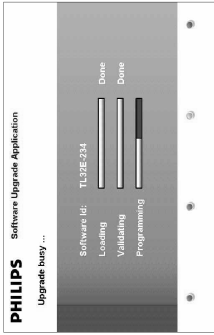
Automatic software upgrade procedure

- Power off your TV and remove all memory devices.
- Insert the USB portable memory that contains the downloaded software upgrade.
- Switch on your TV with the power switch  at the right side of the TV.
- At startup the TV will scan the USB portable memory until it finds the update content. The TV will automatically go to the upgrade mode. After a few seconds it will display the status of the upgrade procedure.

Warning

- You are not allowed to remove the USB portable memory during the software upgrade procedure!
- In case of a power drop during the upgrade procedure, don't remove the USB portable memory from the TV. The TV will continue the upgrade as soon as the power comes back.
- If you try to upgrade to a software version lower than the current version, a confirmation will be asked. Downgrading to older software should only be done in case of real necessity.
- If an error occurs during the upgrade, you should retry the procedure or contact your dealer.

- When the software upgrade was successful, remove the USB portable memory and restart your TV with the power switch  at the right side of the TV.
Your TV will start up with the new software.
Note: Once the upgrade is finished use your PC to remove the TV software from your USB portable memory.




Manual software upgrade procedure

For a manual software upgrade copy the "autounupg" file in a directory called "Upgrades" located in the root of the USB portable memory.

- Insert the portable memory that contains the downloaded software upgrade.
- Select **Software Upgrade** in the Installation menu. Go to **Local upgrades/applications**.
- The TV will list all compatible images available on the USB portable memory and display the data for each selected upgrade image.
- Select the correct upgrade image and press the red color button to start the upgrade.
Your TV will restart and will automatically go to the upgrade mode. After a few seconds it will display the status of the upgrade procedure.

Warning

If you try to upgrade to a software version equal or lower than the current version, a confirmation will be asked. Downgrading to older software should only be done in case of real necessity.

- When the software upgrade was successful, remove the USB portable memory and restart your TV with the power switch  at the right side of the TV.
Your TV will start up with the new software.

Annex 1 - Philips TV software upgrade with portable memory

Introduction

Philips offers software upgrade capability for your TV using portable memory.

After you have completed a software upgrade, your TV will typically perform better.

What improvements are made depends on the upgrade software you are using as well as the software your TV contained before the upgrade.

You can execute the software upgrade procedure yourself.

Be aware that the content of this document is addressing technical or software skilled users.

Preparing a portable memory for software upgrade

For the procedure you will require:

- A personal computer with web browsing capability.
- An archive utility that supports the ZIP-format (e.g. WinZip for Windows or Stuffit for Mac OS).
- A preferably empty USB memory stick or memory card (if available).

Supported memory cards (if available): CompactFlash Card Type I & II, IBM Microdrive, Memory Stick, SecureDigital Card / Mini SD Card, SmartMedia Card, MultiMedia Card.

Note: Only FAT/DOS-formatted portable memory is supported.

New software can be obtained from your dealer or can be downloaded from the www.philips.com/support website:

- Go to www.philips.com/support using the web browser on your PC.
- Follow the procedure to find the information and the software related to your TV.
- Select the latest software upgrade file and download it to your PC.
- Decompress the ZIP file and copy the file "autounupg" to the root directory of the USB portable memory.

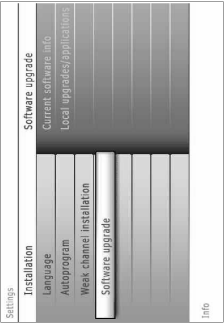
Note: Only use software upgrades that can be found on the www.philips.com/support web site.

Verifying the version of the TV software

Before starting the software upgrade procedure, it is advised to check what the current TV software is.

- Select **Software Upgrade** in the Installation menu.
- Press the cursor right.
- The Software Upgrade menu moves to the left panel.

Select **Current Software Info** to observe the version and the description of the current software.



4. Mechanical Instructions

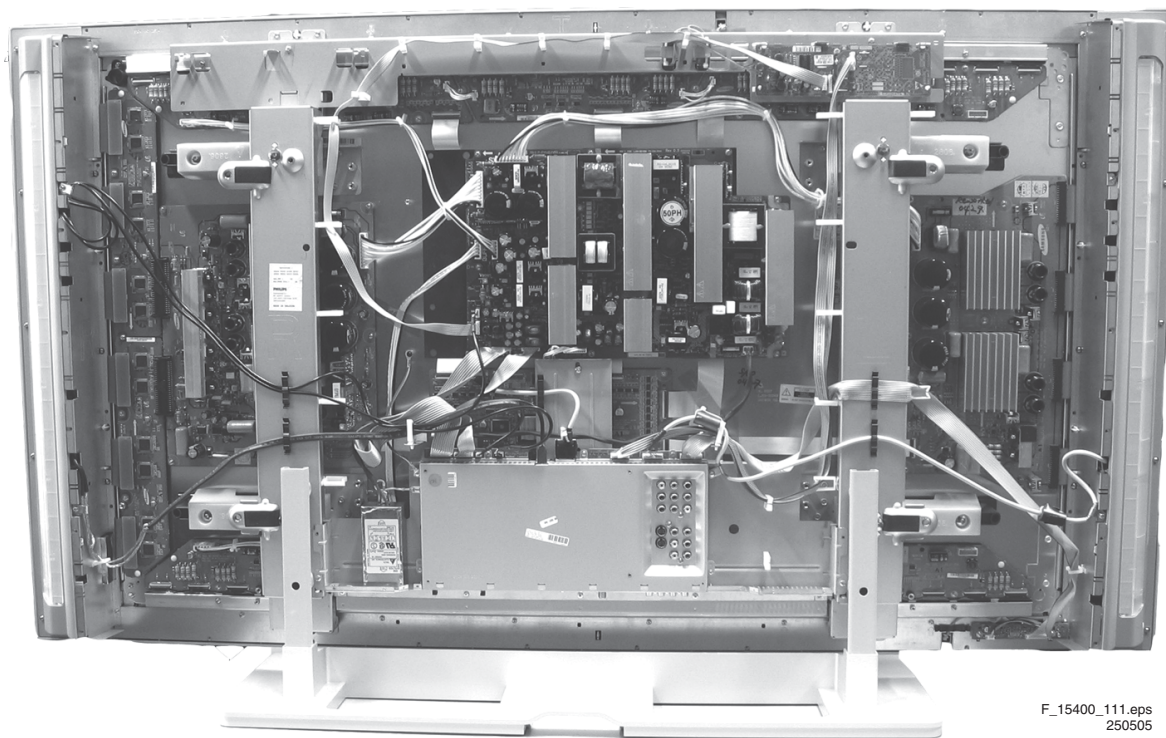
Index of this chapter:

- 4.1 Cable Dressing
- 4.2 Service Positions
- 4.3 Assy/Panel Removal
- 4.4 Set Re-assembly

Notes:

- Figures below can deviate slightly from the actual situation, due to the different set executions.
- Follow the disassemble instructions in described order.

4.1 Cable Dressing



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250505

Figure 4-1 Cable dressing (BP2.2U)

4.2 Service Positions

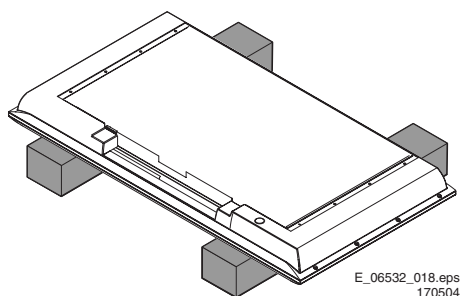
For easy servicing of this set, there are a few possibilities created:

- The buffers from the packaging.
- Foam bars (created for service).
- Aluminium service stands (created for Service).

By placing a mirror under the TV, you can monitor the screen.

4.2.2 Aluminium Stands

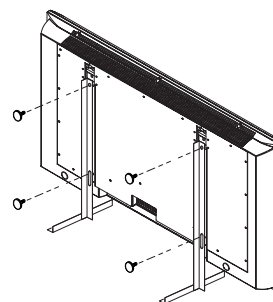
4.2.1 Foam Bars



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170504

Figure 4-2 Foam bars

The foam bars (order code 3122 785 90580 for two pieces) can be used for all types and sizes of Flat TVs. By laying the TV face down on the (ESD protective) foam bars, a stable situation is created to perform measurements and alignments.



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170504

Figure 4-3 Aluminium stands (drawing of MkI)

The new MkII aluminium stands (not on drawing) with order code 3122 785 90690, can also be used to do measurements, alignments, and duration tests. The stands can be (dis)mounted quick and easy by means of sliding them in/out the "mushrooms". The new stands are backwards compatible with the earlier models.

Important: For (older) FTV sets without these "mushrooms", it is obligatory to use the provided screws, otherwise it is possible to damage the monitor inside!

4.3 Assy/Panel Removal

4.3.1 Metal Rear Cover

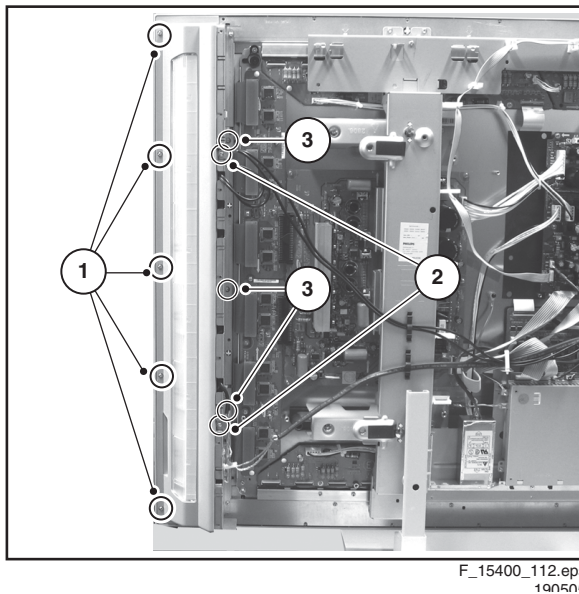
Caution: Disconnect the Mains/AC Power cord before you remove the rear cover!

1. Place the TV set upside down on a table top, using the foam bars (see part "Foam Bars").
Caution: do **not** put pressure on the display, but let the monitor lean on the speakers or the Front cover.
2. Remove all T10 screws around the edges of the metal rear cover: "parker" screws around the outer rim, "tapping" screws around the connector plate.
3. Remove the four "mushrooms" from the rear cover.
4. Lift the metal rear cover from the set. Make sure that wires and flat foils are not damaged.

4.3.2 Speaker Compartment Cover

After removing the metal rear cover, you gain access to the Speaker Compartment covers.

1. Remove all T10 screws [1] around the outer rim of the cover.
2. Remove the T10 screws [2] on top of the inner rim.
3. **For sets with AmbiLight:** Remove the T10 screws [3] at the bottom of the inner rim.
4. After removal of all the screws, slightly push the top of the cover inwards. This will lift the outer rim slightly up so you can take the cover out.

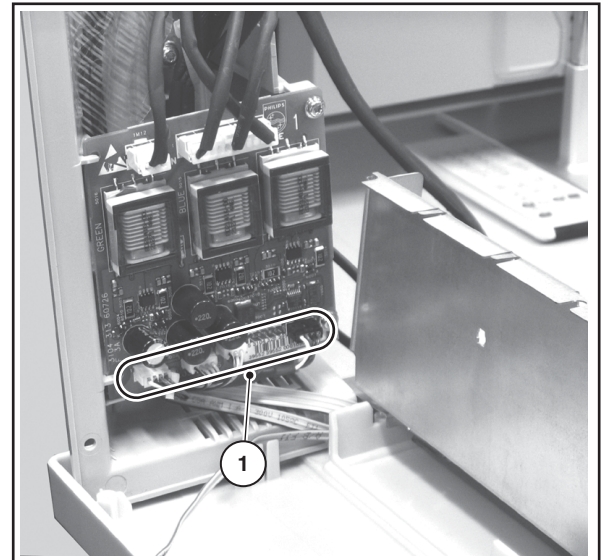


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Figure 4-4 Speaker compartment cover removal

To release the complete cover (only for models with the AmbiLight feature, as in figure above):

- Lift the cover up; let it hinge at the top side.
- Now, unplug the cables [1] at the AmbiLight Inverter panel.



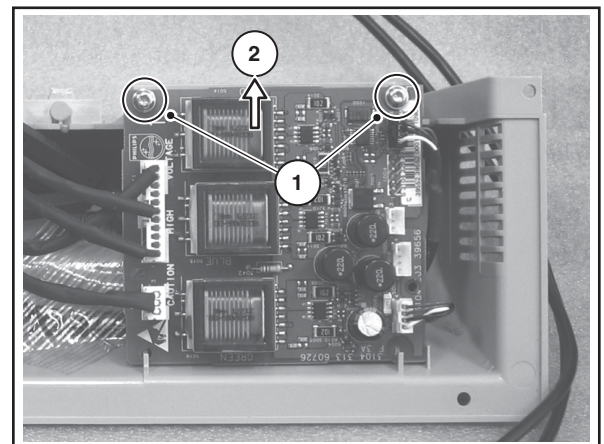
F_15400_114.eps
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Figure 4-5 AmbiLight inverter panel connections

4.3.3 AmbiLight Inverter Panel (if present)

After removal of the Speaker Compartment Covers, this panel is accessible.

1. Disconnect the cable(s) from the panel.
2. Remove the T10 mounting screws [1] that hold the assy.
3. Take out the panel from its bracket [2].



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190505

Figure 4-6 AmbiLight inverter panel removal

4.3.4 Control Panel

After removal of the Speaker Compartment Covers, this panel is accessible. Release the clamps and take out the panel

4.3.5 Speakers

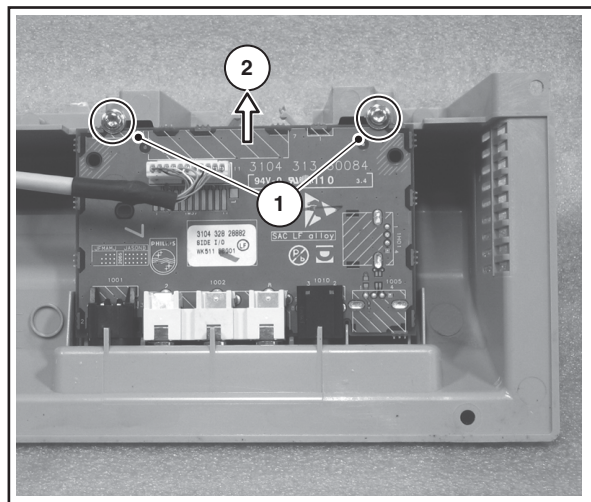
After removal of the Speaker Compartment Covers, you can access the speakers.

4.3.6 Side I/O Panel

After removal of the Speaker Compartment Covers, this panel is accessible.

1. Disconnect the cable(s) from the panel.
2. Remove the T10 mounting screws [1] that hold the assy.
3. Take out the panel from its bracket [2].

When defective, replace the whole unit.



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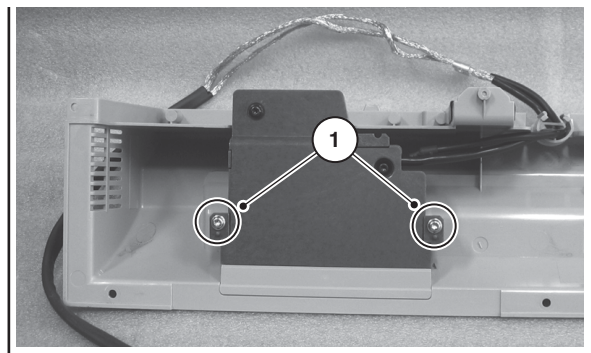
Figure 4-7 Side I/O panel removal

4.3.7 Multimedia Card Reader (if present)

After removal of the Speaker Compartment Covers, this panel is accessible.

1. Unplug the related USB cable at the top of the SSB.
2. Remove the two T10 mounting screws [1] that hold the assy.

When defective, replace the whole unit.



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Figure 4-8 Multimedia card reader removal

4.3.8 Audio Amplifier Panel

1. Disconnect all cables from the Audio Amplifier panel.
2. Remove the T10 mounting screw from the Audio panel.
3. Release the two plastic fixation pins.
4. Take out the Audio panel (it hinges at the top side).

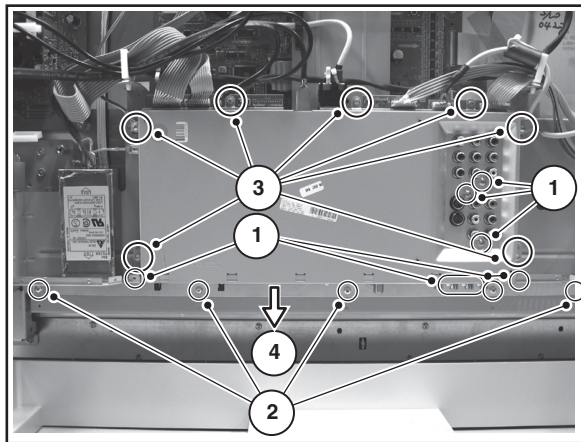
4.3.9 LED Panel

1. Disconnect the cable(s) from the panel.
2. Remove the T10 mounting screws that hold the panel.
3. Take out the panel.

When defective, replace the whole unit.

4.3.10 Small Signal Board (SSB)

1. Remove all connector fixation screws [1] at the connector plate (bottom side), and at the shielding plate (rear side).
2. Remove the fixation screws [2] of the connector plate itself.
3. Remove all shielding fixing screws [3].
4. Slide the connector plate away from the SSB [4], and lift the shielding from the SSB.
5. Unplug all cables on the SSB.
6. Remove the mounting screws that hold the SSB, and lift the panel from the set.

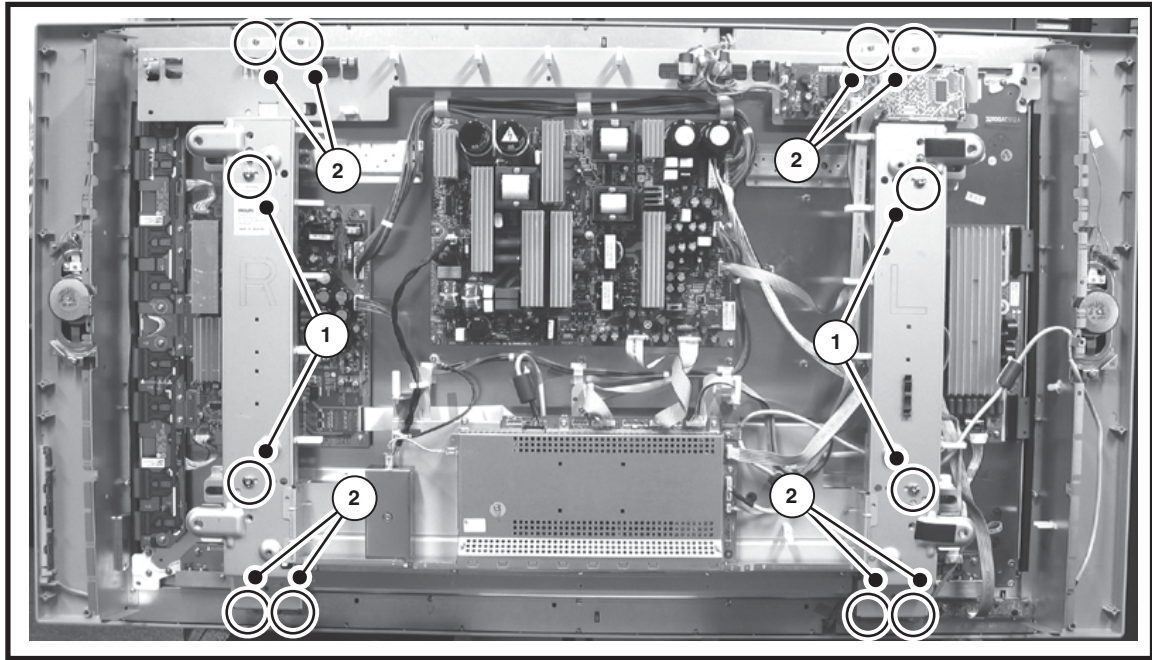


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Figure 4-9 SSB top shielding

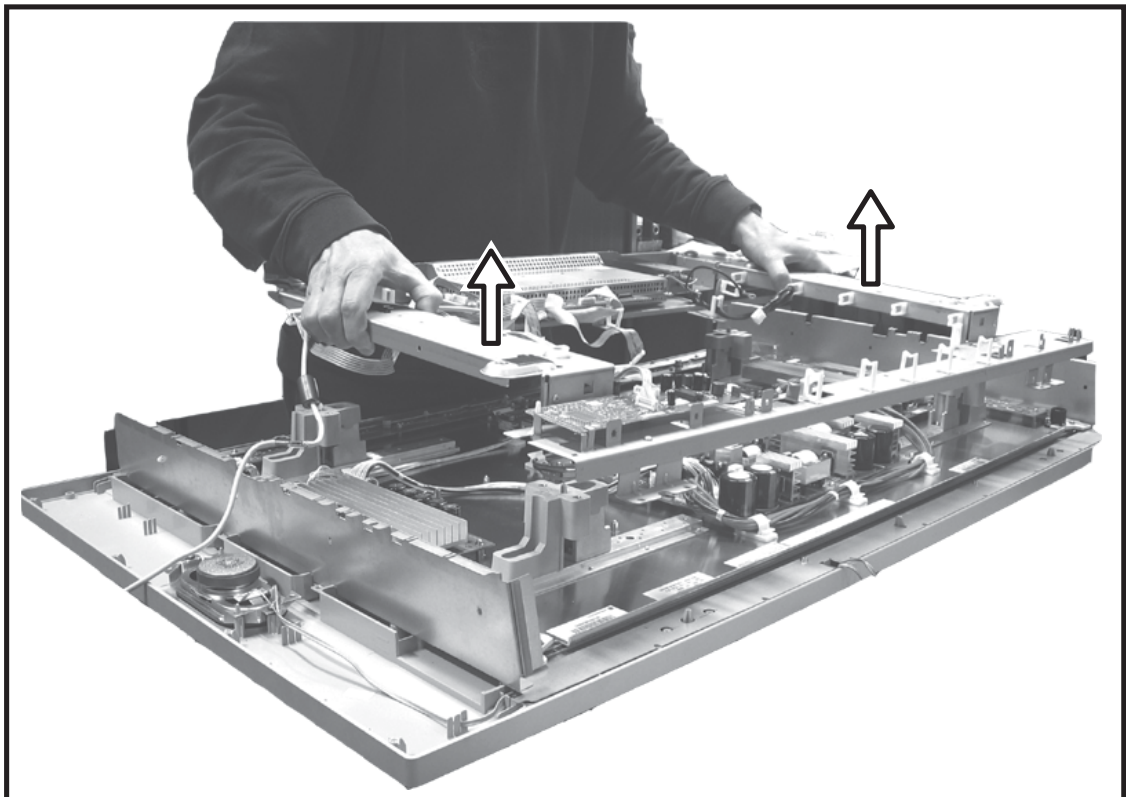
4.3.11 Plasma Display Panel / Glass Plate

1. Remove the T20 display panel mounting screws [1].
2. Remove the T10 screws [2] from the mounting frame.
3. Unplug all cable(s):
 - LVDS cable at SSB side (fragile connector!).
 - SSB supply cables at the Main Supply board.
 - Mains cable at the Main Supply board.
 - Side I/O cable at SSB side (fragile connector!).
4. Lift the metal frame (together with all PWBs) from the display panel (see figure “Frame lift”).
5. After removal of the frame, lift the PDP from the set.



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Figure 4-10 Display panel removal (photo from LC4.9 chassis)



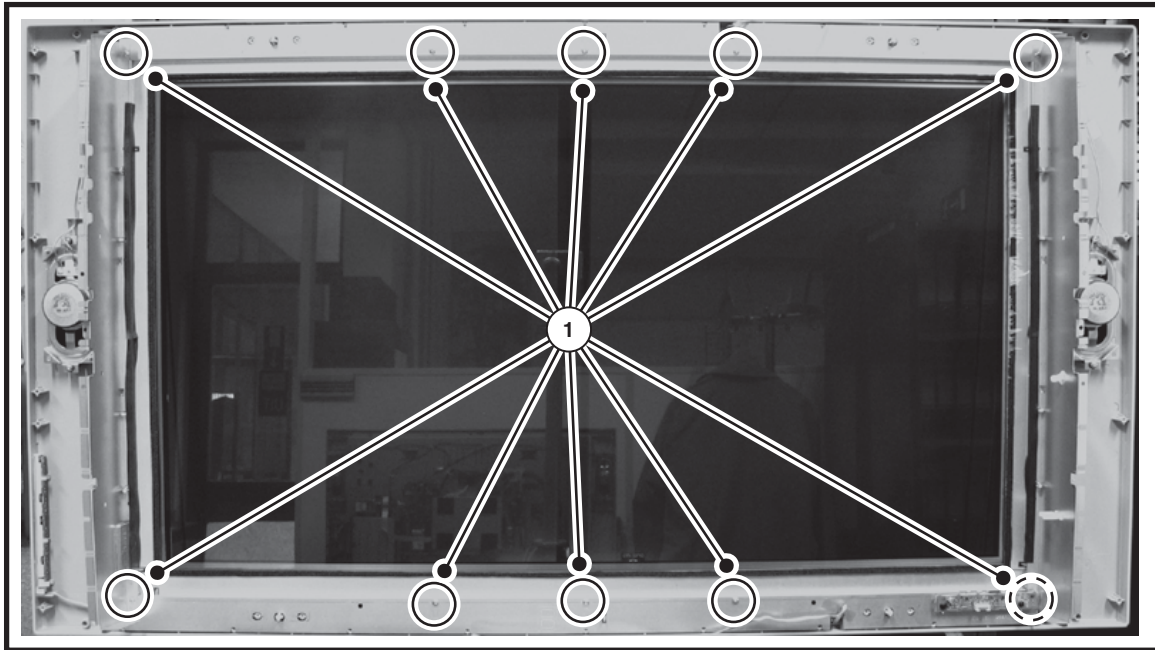
F_15400_120.eps
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Figure 4-11 Frame lift (photo from LC4.9 chassis)

4.3.12 PDP Glass Plate

In order to remove/exchange the PDP glass plate:

1. Remove the PDP as described earlier.
2. Remove the T10 screws [1] from the mounting frame.
3. After removal of the frame, you can lift the glass plate from the set.



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200505

Figure 4-12 Glass plate removal (photo from LC4.9 chassis)

4.4 Set Re-assembly

To re-assemble the whole set, execute all processes in reverse order.

Notes:

- While re-assembling, make sure that all cables are placed and connected in their original position. See figure "Cable dressing".
- Pay special attention not to damage the EMC foams on the SSB shields. Ensure that EMC foams are mounted correctly.

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

- 5.1 Test Points
- 5.2 Service Modes
- 5.3 Stepwise Start-up
- 5.4 Service Tools
- 5.5 Error Codes
- 5.6 The Blinking LED Procedure
- 5.7 Protections
- 5.8 Fault Finding and Repair Tips
- 5.9 Software Upgrading

5.1 Test Points

The chassis is equipped with test points (Fxxx) printed on the circuit board assemblies. As most signals are digital, it will be almost impossible to measure waveforms with a standard oscilloscope. Therefore, waveforms are not given in this manual. Several key ICs are capable of generating test patterns, which can be controlled via ComPair. In this way it is possible to determine which part is defective.

Perform measurements under the following conditions:

- Service Default Mode.
- Video: Color bar signal.
- Audio: 3 kHz left, 1 kHz right.

5.2 Service Modes

Service Default Mode (SDM) and Service Alignment Mode (SAM) offer several features for the service technician, while the Customer Service Mode (CSM) is used for communication between a Customer Helpdesk and a customer.

There is also the option of using ComPair, a hardware interface between a computer (see requirements below) and the TV chassis. It offers the ability of structured troubleshooting, test pattern generation, error code reading, software version readout, and software upgrading.

Minimum requirements for ComPair: a Pentium processor, Windows 95/98, and a CD-ROM drive (see also paragraph "ComPair").

5.2.1 Service Default Mode (SDM)

Purpose

- To create a pre-defined setting, to get the same measurement results as given in this manual.
- To override SW protections (only applicable for protections detected by stand-by processor) and make the TV start up to the step just before protection (a sort of automatic stepwise start up). See paragraph "Stepwise Start Up".
- To start the blinking LED procedure (not valid in protection mode).

Specifications

Table 5-1 SDM default settings

Region	Freq. (MHz)	Default system
Europe, AP-PAL/Multi	475.25	PAL B/G
NAFTA, AP-NTSC, LATAM	61.25 (ch. 3)	NTSC M

- Tuning frequency 61.25 MHz for NTSC: The TV shall tune to physical channel 3 only if channel 3 is an analog channel or if there is no channel 3 installed in the channel map. If there is a digital channel installed in channel 3, then the

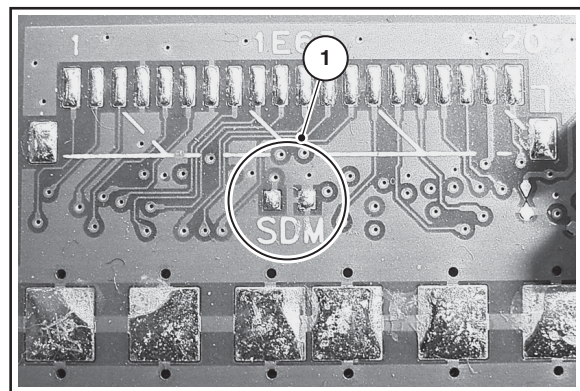
frequency to which the set will tune, would be as specified in the channel map and could be different from the one corresponding to the physical channel 3.

- All picture settings at 50% (brightness, color, contrast).
- All sound settings at 50%, except volume at 25%.
- All service-unfriendly modes (if present) are disabled, like:
 - (Sleep) timer.
 - Child/parental lock.
 - Picture mute (blue mute or black mute).
 - Automatic volume levelling (AVL).
 - Auto switch "off" (when no video signal was received for 10 minutes).
 - Skip/blank of non-favorite pre-sets.
 - Smart modes.
 - Auto store of personal presets.
 - Auto user menu time-out.

How to Activate SDM

Use one of the following methods:

- Use the standard RC-transmitter and key in the code "062596", directly followed by the "MENU" button.
Note: It is possible that, together with the SDM, the main menu will appear. To switch it "off", push the "MENU" button again.
- Short for a moment the two solder pads [1] on the SSB, with the indication "SDM". They are located outside the shielding. Activation can be performed in all modes, except when the set has a problem with the Stand-by Processor. See figure "SDM service pads".



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Figure 5-1 SDM service pads

After activating this mode, "SDM" will appear in the upper right corner of the screen (if you have picture).

How to Navigate

When you press the "MENU" button on the RC transmitter, the set will toggle between the SDM and the normal user menu (with the SDM mode still active in the background).

How to Exit SDM

Use one of the following methods:

- Switch the set to STAND-BY via the RC-transmitter.
- Via a standard customer RC-transmitter: key in "00"-sequence.

5.2.2 Service Alignment Mode (SAM)

Purpose

- To perform (software) alignments.
- To change option settings.
- To easily identify the used software version.
- To view operation hours.

- To display (or clear) the error code buffer.

How to Activate SAM

Via a standard RC transmitter: key in the code "062596" directly followed by the "INFO" button. After activating SAM with this method a service warning will appear on the screen, you can continue by pressing the red button on the RC.

Contents of SAM:

- Hardware Info.**
 - A. VIPER SW Version.** Displays the software version of the VIPER software (main software) (**example:** BX23U-1.2.3.4_12345 = AAAAB_X.Y.W.Z_NNNNN).
 - AAAA**= the chassis name.
 - B**= the region: A= AP, E= EU, L= Latam, U = US.
 - X.Y.W.Z**= the software version, where X is the main version number (different numbers are not compatible with one another) and Y is the sub version number (a higher number is always compatible with a lower number). The last two digits are used for development reasons only, so they will always be zero in official releases.
 - NNNNN**= last five digits of 12nc code of the software.
 - B. SBY PROC Version.** Displays the software version of the stand-by processor.
 - C. Production Code.** Displays the production code of the TV, this is the serial number as printed on the back of the TV set. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee in a possibility to do this.
- Operation Hours.** Displays the accumulated total of operation hours (not the stand-by hours). Every time the TV is switched "on/off", 0.5 hours is added to this number.
- Errors.** (Followed by maximal 10 errors). The most recent error is displayed at the upper left (for an error explanation see paragraph "Error Codes").
- Defective Module.** Here the module that generates the error is displayed. If there are multiple errors in the buffer, which are not all generated by a single module, there is probably another defect. It will then display the message "UNKNOWN" here.
- Reset Error Buffer.** When you press "cursor right" and then the "OK" button, the error buffer is reset.
- Alignments.** This will activate the "ALIGNMENTS" sub-menu.
- Dealer Options.** Extra features for the dealers.
- Options.** Extra features for Service.
- Initialise NVM.** When an NVM was corrupted (or replaced) in the former EMG based chassis, the microprocessor replaces the content with default data (to assure that the set can operate). However, all preferences and alignment values are gone now, and option numbers are not correct. Therefore, this was a very drastic way. In this chassis, the procedure is implemented in another way: The moment the processor recognizes a corrupted NVM, the "initialize NVM" line will be highlighted. Now, you can do two things (dependent of the service instructions at that moment):
 - Save the content of the NVM via ComPair for development analysis, **before** initializing. This will give the Service department an extra possibility for diagnosis (e.g. when Development asks for this).
 - Initialize the NVM (same as in the past, however now it happens conscious).

Note: When you have a corrupted NVM, or you have replaced the NVM, there is a high possibility that you will not have picture any more because your display option is not correct. So, before you can initialize your NVM via the SAM, you need to have a picture and therefore you need the correct display option. To adapt this option, use ComPair. The correct HEX values for the options can be found in the table below.

Table 5-2 Display option code overview

Display Option	HEX	Display Type	Size	Vertical Resolution
000	00	PDP SDI HD V3	42"	768p
001	01	PDP SDI HD V3	50"	768p
002	02	PDP FHP ALIS 1024i	42"	1024i
003	03	LPL	30"	768p
004	04	LPL:	37"	768p
005	05	LPL	42"	768p
006	06	SHARP	32"	768p
007	07	PDP SDI SD V3	42"	480p
008	08	PDP FHP ALIS 1024i	37"	1024i
009	09	LCOS XION	-	720p
010	0A	LCD AUO	30"	768p
011	0B	LCD LPL	32"	768p
012	0C	LCD AUO	32"	768p
013	0D	LCD SHARP	37"	768p
014	0E	LCD LPL HD	42"	1080p
015	0F	PDP SDI SD	37"	480p
016	10	PDP FHP ALIS 1080i	37"	1080i
017	11	PDP FHP ALIS 580i	42"	1080i
018	12	PDP FHP	55"	768p
019	13	LCOS VENUS	-	720p
020	14	LCOS VENUS	-	1080p
021	15	LCD LPL	26"	768p
022	16	LCD LPL scanning BL.	32"	768p
023	17	LG SD	42"	480p
024	18	PDP SDI SD V4	42"	480p
025	19	PDP SDI HD V4	42"	768p
026	1A	PDP FHP HD A2	42"	1024i
027	1B	PDP SDI HD V4	50"	768p
028	1C	LCD Sharp full HD	37"	1080p

- Store.** All options and alignments are stored when pressing "cursor right" and then the "OK"-button
- SW Maintenance.**
 - SW Events.** Not useful for service purposes. In case of specific software problems, the development department can ask for this info.
 - HW Events.** Not functional at the moment this manual is released, description will be published in an update manual if the function becomes available.

How to Navigate

- In SAM, you can select the menu items with the "CURSOR UP/DOWN" key on the RC-transmitter. The selected item will be highlighted. When not all menu items fit on the screen, move the "CURSOR UP/DOWN" key to display the next/previous menu items.
- With the "CURSOR LEFT/RIGHT" keys, it is possible to:
 - (De) activate the selected menu item.
 - (De) activate the selected submenu.

How to Exit SAM

Use one of the following methods:

- Press the "MENU" button on the RC-transmitter.
- Switch the set to STAND-BY via the RC-transmitter.

Note: As long as SAM is activated, it is not possible to change a channel. This could hamper the White Point alignments because you cannot choose your channel/frequency any more. Workaround: after you have sent the RC code "062596 INFO" you will see the service-warning screen, and in this stage it is still possible to change the channel (so before pressing the "OK" button).

5.2.3 Customer Service Mode (CSM)

Purpose

When a customer is having problems with his TV-set, he can call his dealer or the Customer Helpdesk. The service technician can then ask the customer to activate the CSM, in order to identify the status of the set. Now, the service technician can judge the severity of the complaint. In many cases, he can advise the customer how to solve the problem, or he can decide if it is necessary to visit the customer. The CSM is a read only mode; therefore, modifications in this mode are not possible.

How to Activate CSM

Key in the code "123654" via the standard RC transmitter.

Note: Activation of the CSM is only possible if there is no (user) menu on the screen!

How to Navigate

By means of the "CURSOR-DOWN/UP" knob on the RC-transmitter, you can navigate through the menus.

Contents of CSM

- **SW Version (example: BX23U-1.2.3.4_12345).** Displays the built-in main software version. In case of field problems related to software, software can be upgraded. As this software is consumer upgradeable, it will also be published on the Internet.
- **SBY Processor Version.** Displays the built-in stand-by processor software version. Upgrading this software will be possible via a PC and a ComPair interface (see chapter Software upgrade).
- **Set Type.** This information is very helpful for a helpdesk/workshop as reference for further diagnosis. In this way, it is not necessary for the customer to look at the rear of the TV-set. Note that if an NVM is replaced or is initialized after corruption, this set type has to be re-written to NVM. ComPair will foresee a possibility to do this.
- **Production Code.** Displays the production code (the serial number) of the TV. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee a possibility to do this.
- **Code 1.** Gives the latest five errors of the error buffer. As soon as the built-in diagnose software has detected an error the buffer is adapted. The last occurred error is displayed on the leftmost position. Each error code is displayed as a 2-digit number. When less than 10 errors occur, the rest of the buffer is empty (00). See also paragraph Error Codes for a description.
- **Code 2.** Gives the first five errors of the error buffer. See also paragraph Error Codes for a description.
- **Headphone Volume.** Gives the last status of the headphone volume, as set by the customer. The value can vary from 0 (volume is minimum) to 100 (volume is maximum). Change via "MENU", "TV", "SOUND", "HEADPHONE VOLUME".
- **Dolby.** Indicates whether the received transmitter transmits Dolby sound ("ON") or not ("OFF"). Attention: The presence of Dolby can only be tested by the software on the Dolby Signaling bit. If a Dolby transmission is received without a Dolby Signaling bit, this indicator will show "OFF" even though a Dolby transmission is received.
- **Sound Mode.** Indicates the by the customer selected sound mode (or automatically chosen mode). Possible values are "STEREO" and "VIRTUAL DOLBY SURROUND". Change via "MENU", "TV", "SOUND", "SOUND MODE". It can also have been selected automatically by signaling bits (internal software).
- **Tuner Frequency.** Not applicable for US sets.
- **Digital Processing.** Indicates the selected digital mode. Possible values are "STANDARD" and "PIXEL PLUS".

Change via "MENU", "TV", "PICTURE", "DIGITAL PROCESSING".

- **TV System.** Gives information about the video system of the selected transmitter.
 - M: NTSC M signal received
 - ATSC: ATSC signal received
- **Center Mode.** Not applicable.
- **DNR.** Gives the selected DNR setting (Dynamic Noise Reduction), "OFF", "MINIMUM", "MEDIUM", or "MAXIMUM". Change via "MENU", "TV", "PICTURE", "DNR".
- **Noise Figure.** Gives the noise ratio for the selected transmitter. This value can vary from 0 (good signal) to 127 (average signal) and to 255 (bad signal). For some software versions, the noise figure will only be valid when "Active Control" is set to "medium" or "maximum" before activating CSM.
- **Source.** Indicates which source is used and the video/audio signal quality of the selected source. (Example: Tuner, Video/NICAM) Source: "TUNER", "AV1", "AV2", "AV3", "HDMI 1", "SIDE". Video signal quality: "VIDEO", "S-VIDEO", "RGB 1FH", "YPBPR 1FH 480P", "YPBPR 1FH 576P", "YPBPR 1FH 1080I", "YPBPR 2FH 480P", "YPBPR 2FH 576P", "YPBPR 2FH 1080I", "RGB 2FH 480P", "RGB 2FH 576P" or "RGB 2FH 1080I". Audio signal quality: "STEREO", "SPDIF 1", "SPDIF 2", or "SPDIF".
- **Audio System.** Gives information about the audible audio system. Possible values are "Stereo", "Mono", "Mono selected", "Analog In: No Dig. Audio", "Dolby Digital 1+1", "Dolby Digital 1/0", "Dolby Digital 2/0", "Dolby Digital 2/1", "Dolby Digital 2/2", "Dolby Digital 3/0", "Dolby Digital 3/1", "Dolby Digital 3/2", "Dolby Digital Dual I", "Dolby Digital Dual II", "MPEG 1+1", "MPEG 1/0", "MPEG 2/0". This is the same info as you will see when pressing the "INFO" button in normal user mode (item "signal"). In case of ATSC receiving there will be no info displayed.
- **Tuned Bit.** Not applicable for US sets.
- **Preset Lock.** Indicates if the selected preset has a child lock: "LOCKED" or "UNLOCKED". Change via "MENU", "TV", "CHANNELS", "CHANNEL LOCK".
- **Lock After.** Indicates at what time the channel lock is set: "OFF" or e.g. "18:45" (lock time). Change "MENU", "TV", "CHANNELS", "LOCK AFTER".
- **TV Ratings Lock.** Indicates the "TV ratings lock" as set by the customer. Change via "MENU", "TV", "CHANNELS", "TV RATINGS LOCK". Possible values are: "ALL", "NONE", "TV-Y", "TV-Y7", "TV-G", "TV-PG", "TV-14" and "TV-MA".
- **Movie Ratings Lock.** Indicates the "Movie ratings lock" as set by the customer. Change via "MENU", "TV", "CHANNELS", "MOVIE RATINGS LOCK". Possible values are: "ALL", "NR", "G", "PG", "PG-13", "R", "NC-17" and "X".
- **V-Chip Tv Status.** Indicates the setting of the V-chip as applied by the selected TV channel. Same values can be shown as for "TV RATINGS LOCK".
- **V-Chip Movie Status.** Indicates the setting of the V-chip as applied by the selected TV channel. Same values can be shown as for "MOVIE RATINGS LOCK".
- **Options 1.** Gives the option codes of option group 1 as set in SAM (Service Alignment Mode).
- **Options 2.** Gives the option codes of option group 2 as set in SAM (Service Alignment Mode).
- **AVL.** Indicates the last status of AVL (Automatic Volume Level): "ON" or "OFF". Change via "MENU", "TV", "SOUND", "AVL". AVL can not be set in case of digital audio reception (e.g. Dolby Digital or AC3).
- **Delta Volume.** Indicates the last status of the delta volume for the selected preset as set by the customer: from "-12" to "+12". Change via "MENU", "TV", "SOUND", "DELTA VOLUME".
- **HDMI key validity.** Indicates the key's validity.
- **IEEE key validity.** Indicates the key's validity (n.a.).
- **POD key validity.** Indicates the key's validity.
- **Digital Signal Quality.** Indicates quality of the received digital signal (0= low).

How to Exit CSM

Press any key on the RC-transmitter (with exception of the "CHANNEL +/-", "VOLUME", "MUTE" and digit (0-9) keys).

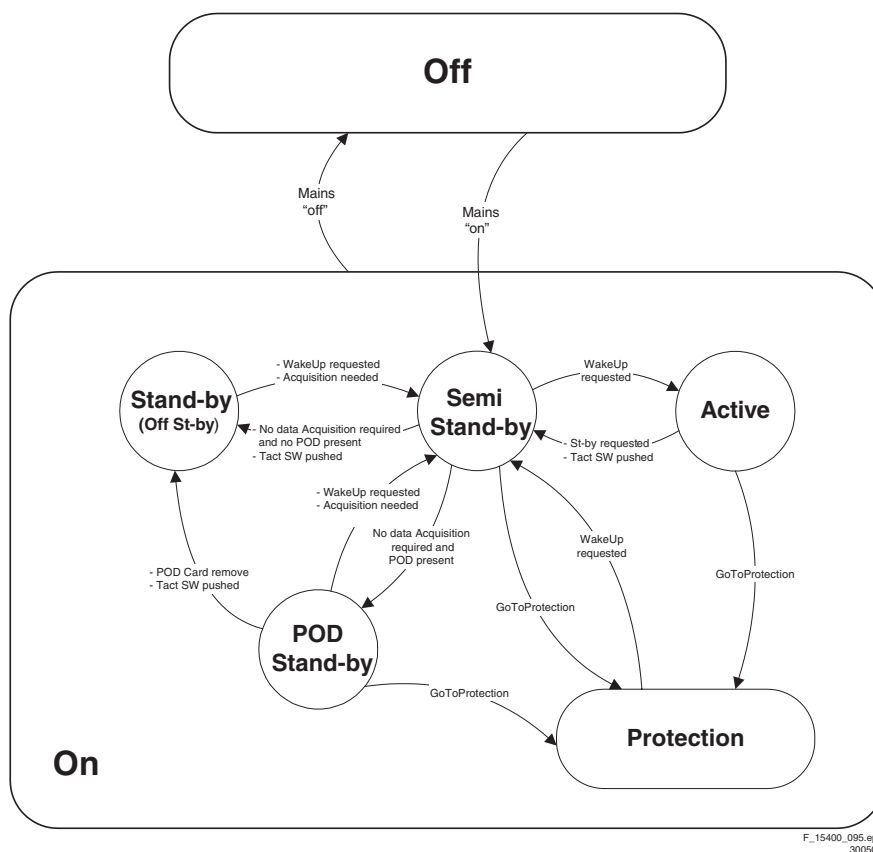
5.3 Stepwise Start-up

The stepwise start-up method, as known from FTL/FTP sets is not valid any more. The situation for this chassis is as follows: when the TV is in a protection state detected via the Stand-by Processor (and thus blinking an error) **and** SDM is activated via shortcutting the pins on the SSB, the TV starts up until it reaches the situation just before protection. So, this is a kind of automatic stepwise start-up. In combination with the start-up diagrams below, you can see which supplies are present at a certain moment.

Important to know here is, that if e.g. the 3V3 detection fails (and thus error 11 is blinking) **and** the TV is restarted via SDM, the Stand-by Processor will enable the 3V3, but will not go to protection now. The TV will stay in this situation until it is reset (Mains/AC Power supply interrupted).

The abbreviations "SP" and "MP" in the figures stand for:

- SP: protection or error detected by the **Stand-by Processor**.
- MP: protection or error detected by the **VIPER Main Processor**.



F_15400_085.eps
300505

Figure 5-2 Transition diagram

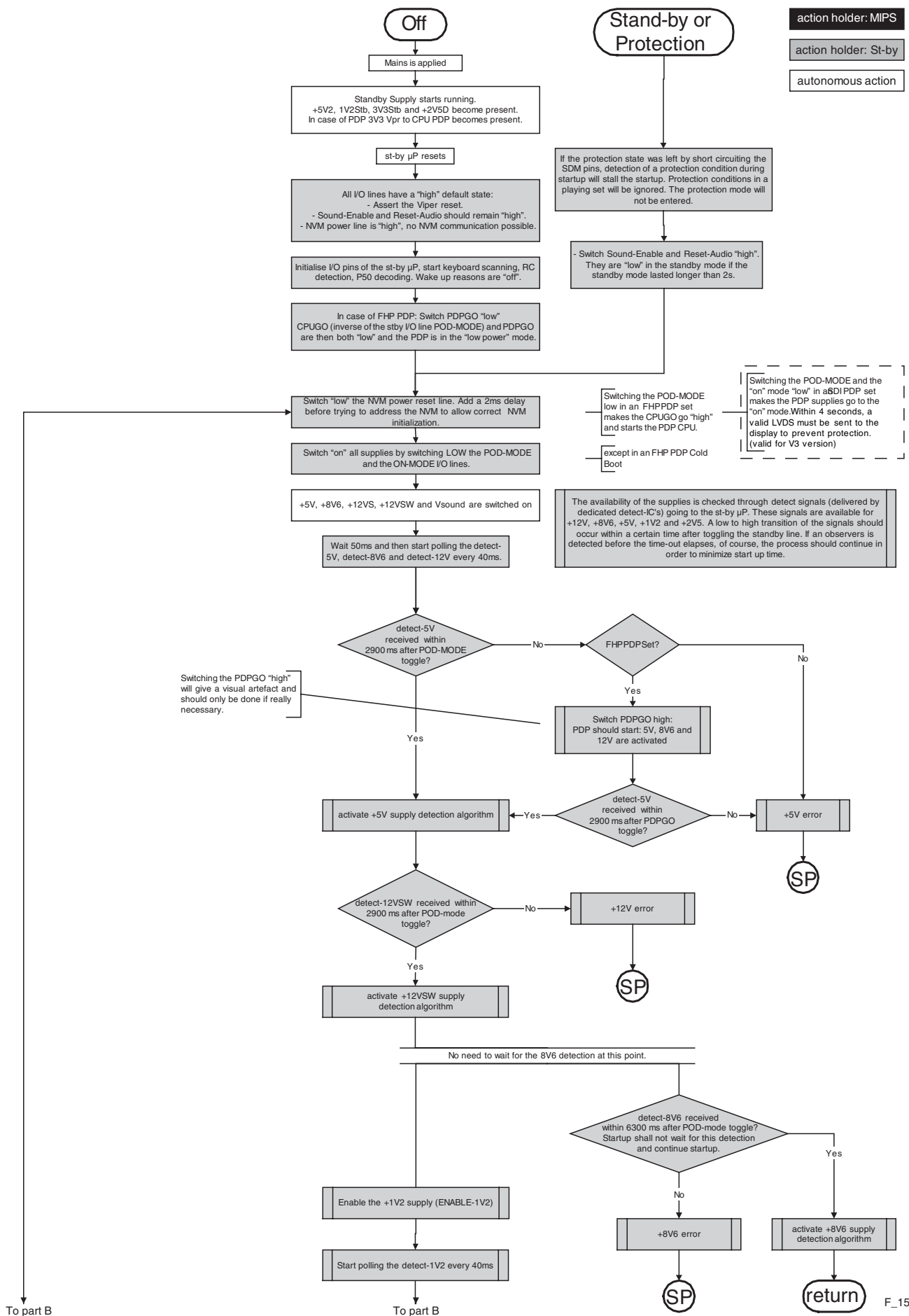


Figure 5-3 "Off" to "Semi Stand-by" flowchart (part 1)

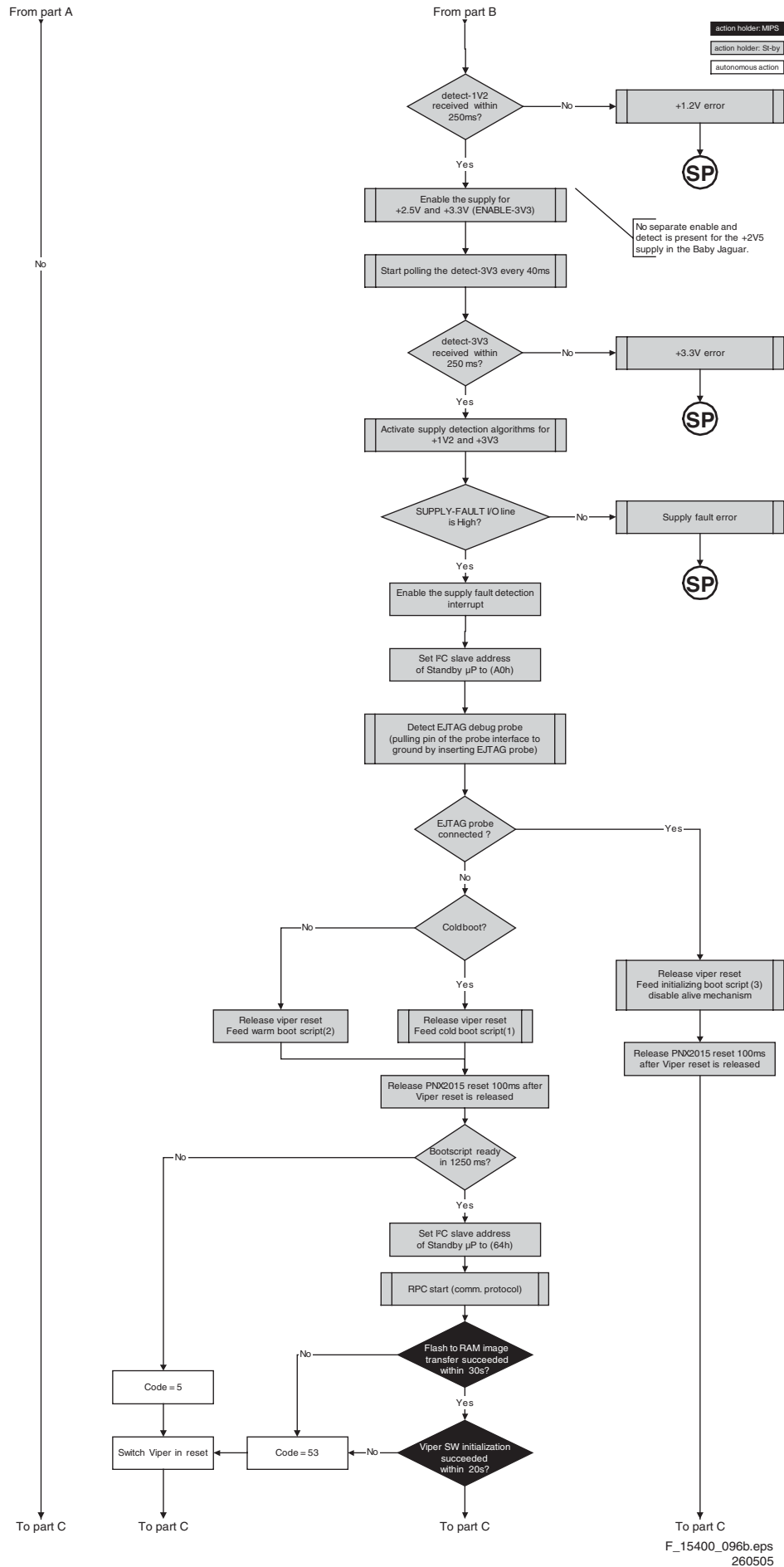


Figure 5-4 “Off” to “Semi Stand-by” flowchart (part 2)

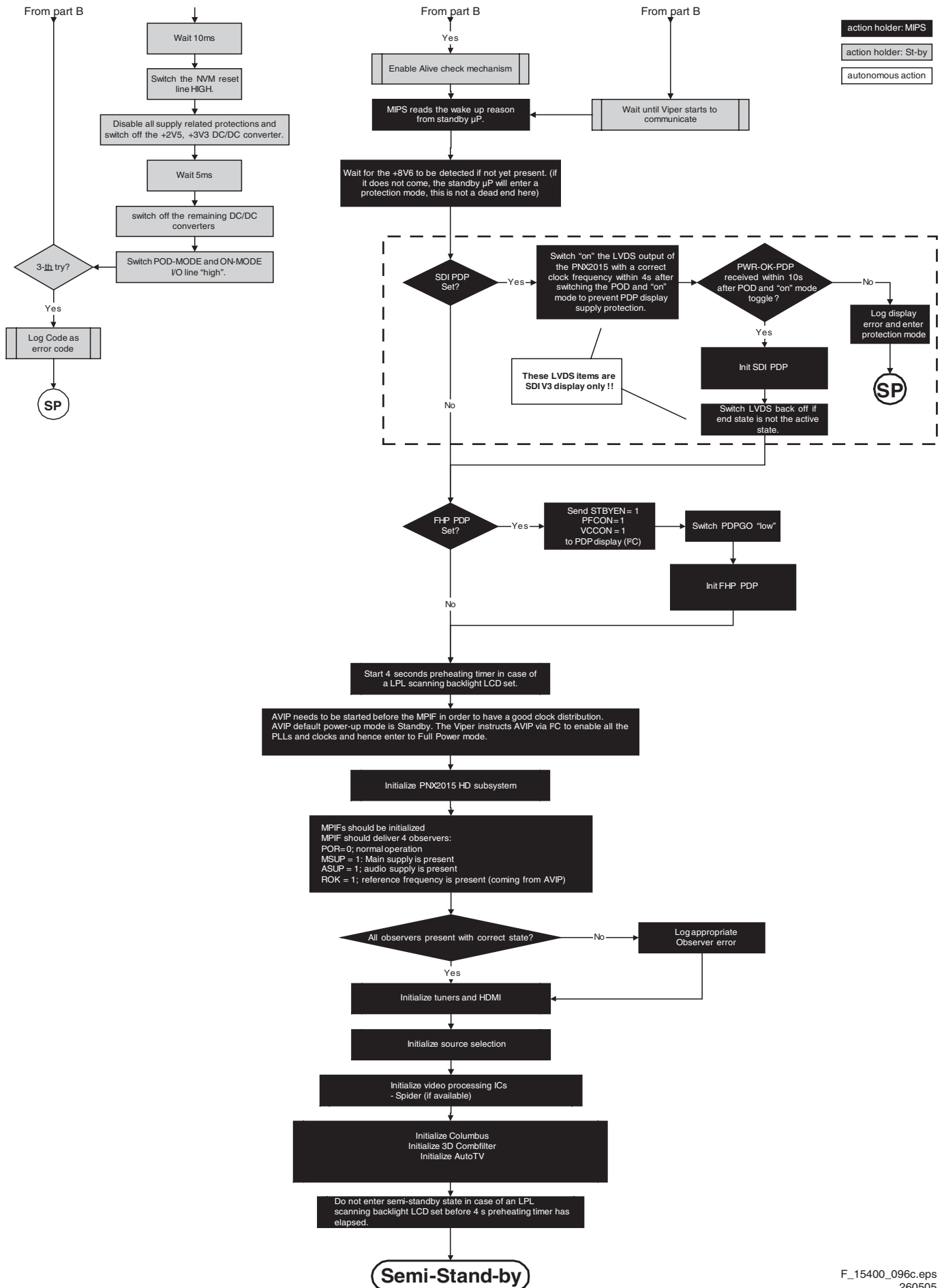


Figure 5-5 "Off" to "Semi Stand-by" flowchart (part 3)

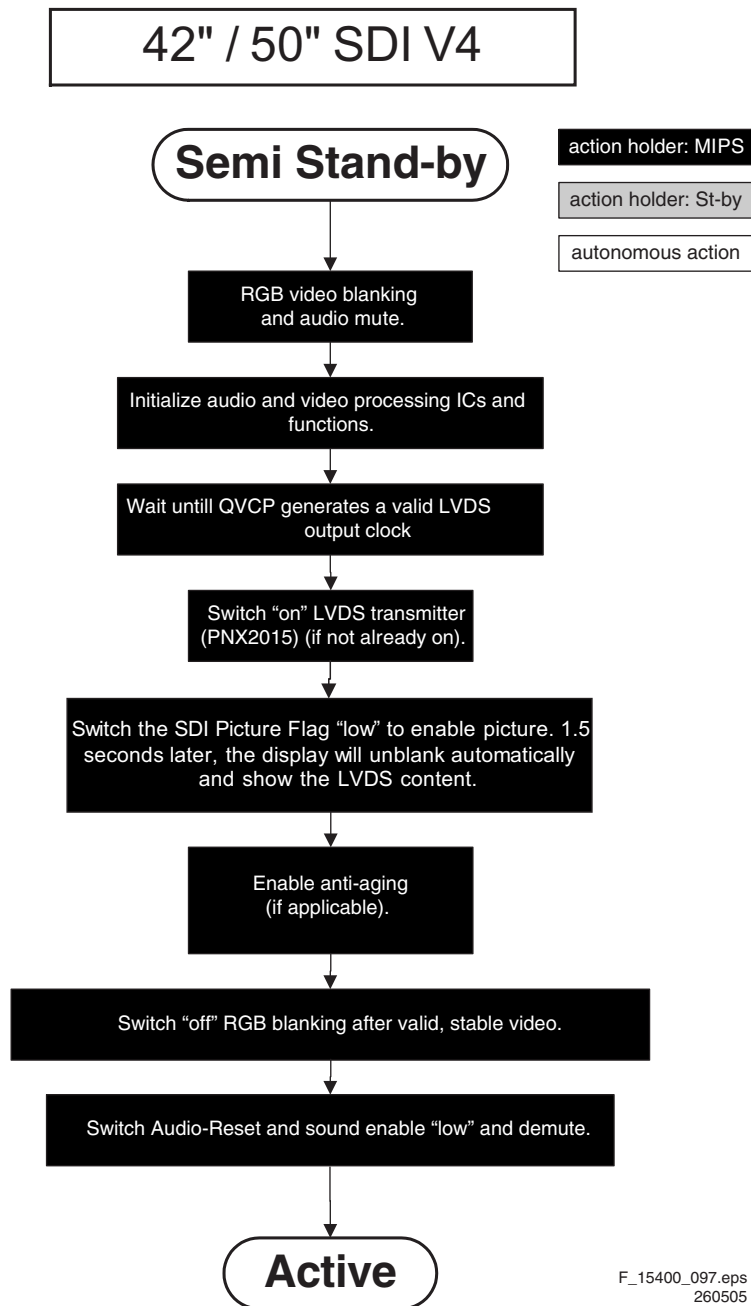


Figure 5-6 "Semi Stand-by" to "Active" flowchart

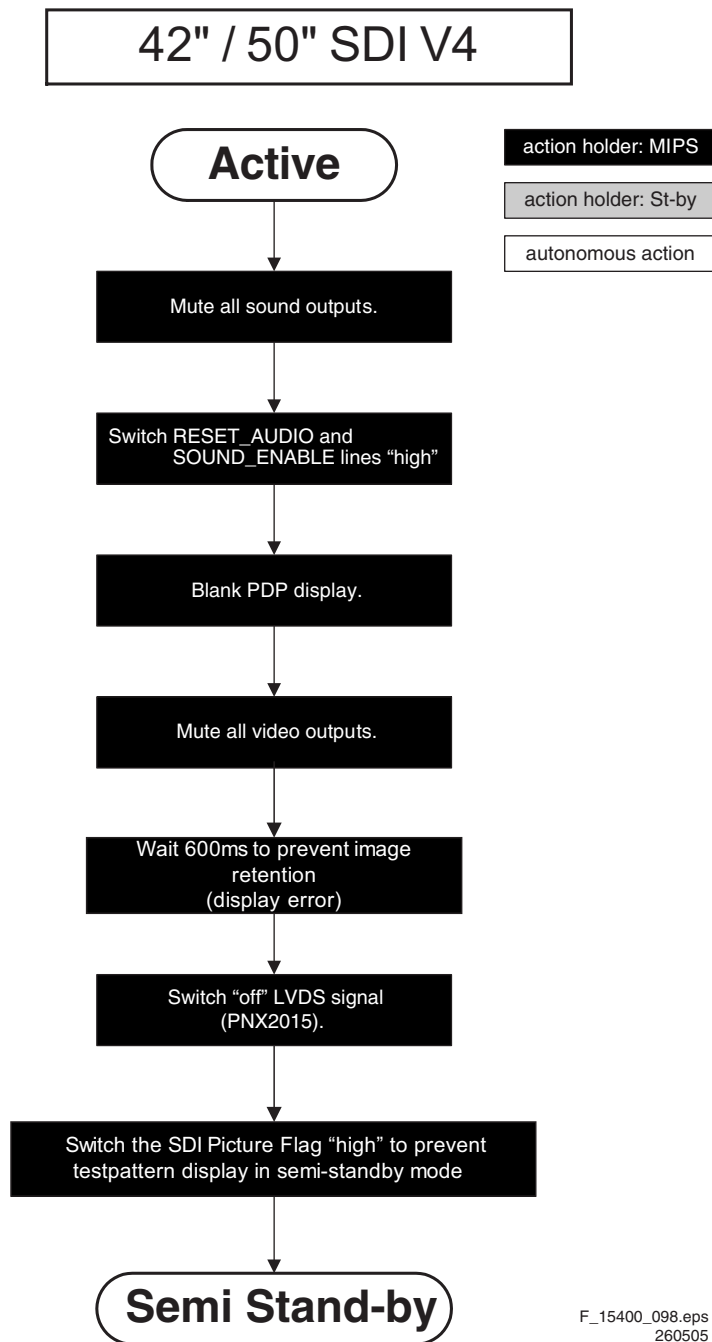


Figure 5-7 "Active" to "Semi Stand-by" flowchart

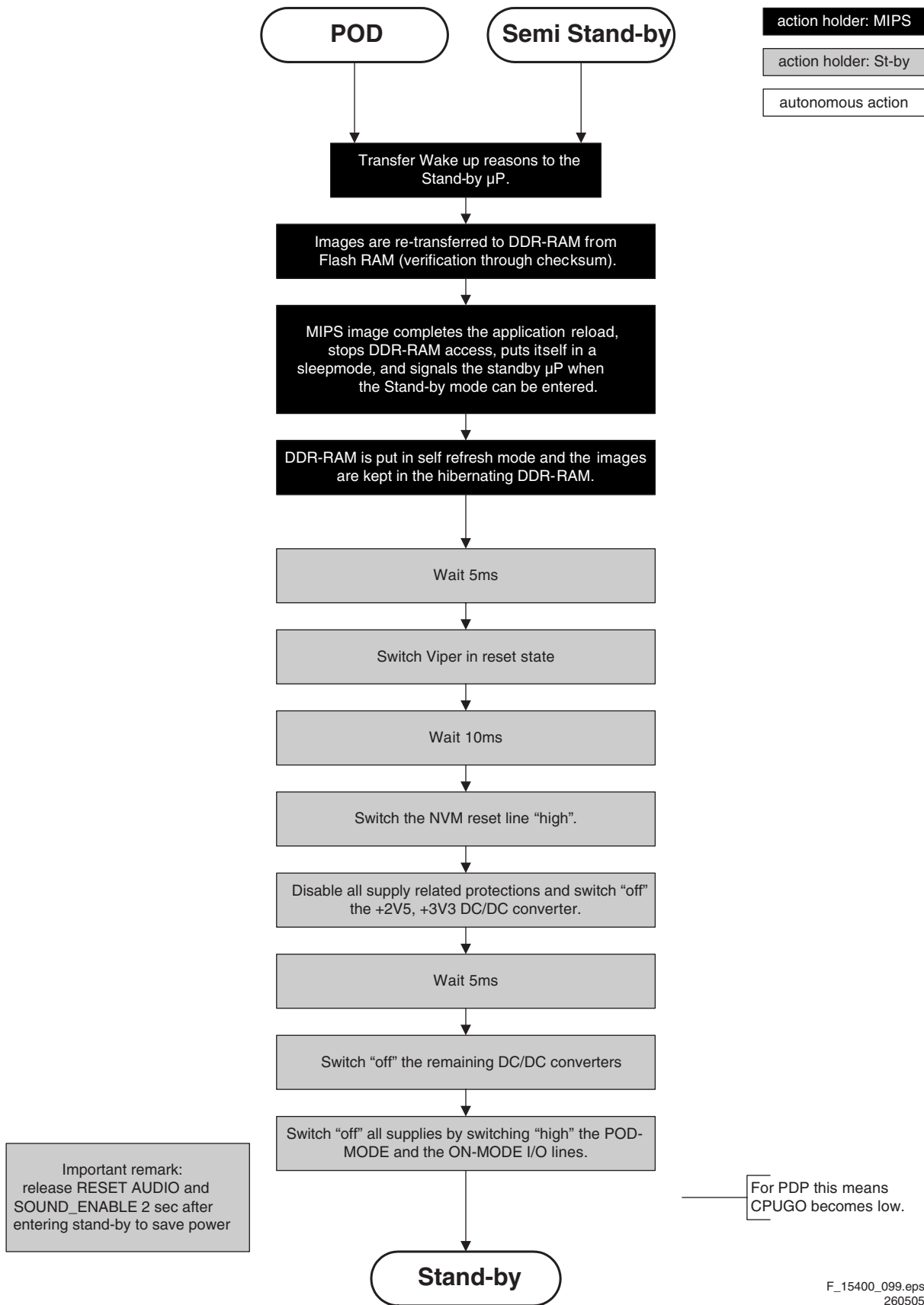


Figure 5-8 “Semi Stand-by” / ”POD” to “Stand-by” flowchart

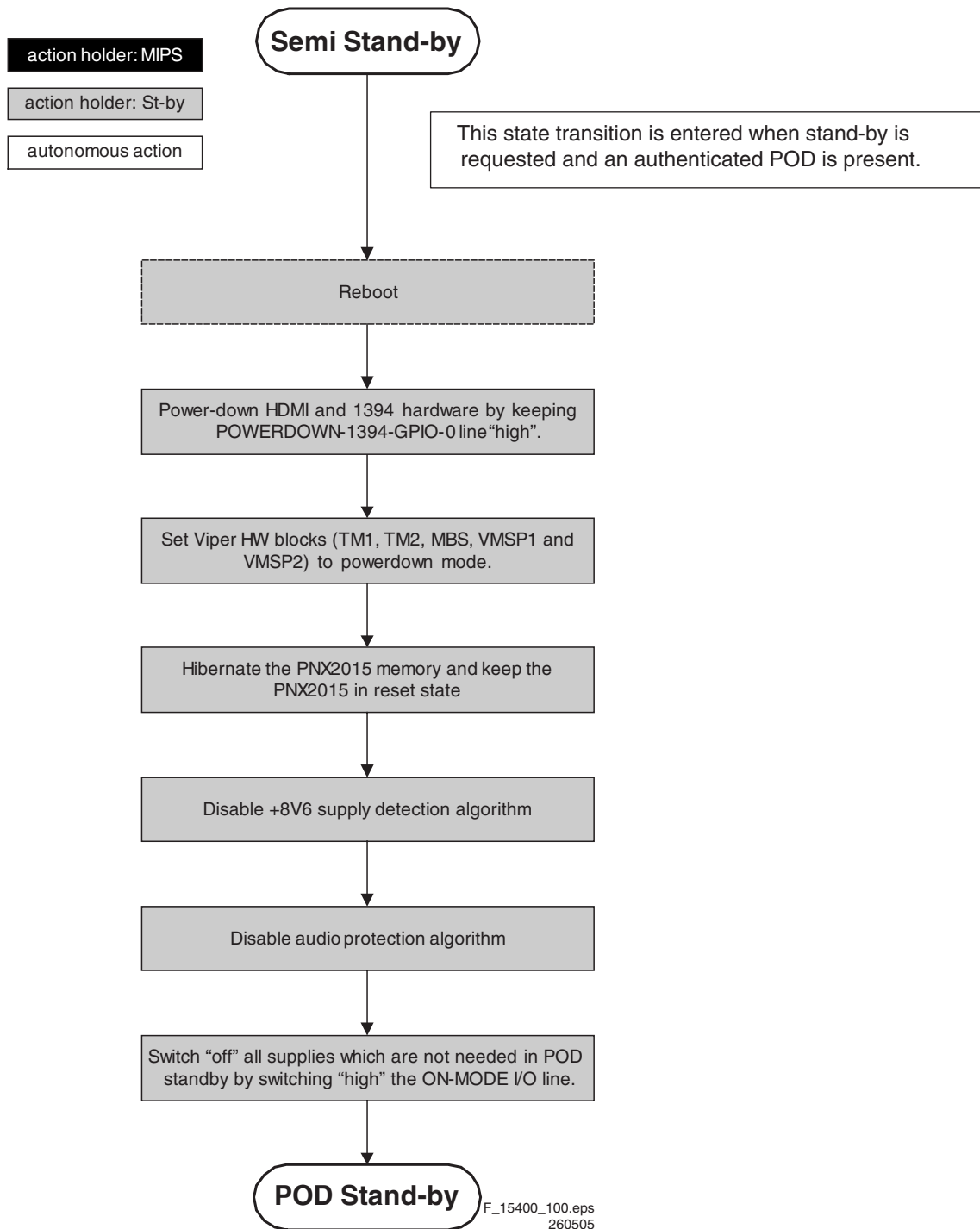


Figure 5-9 "Semi Stand-by" to "POD Stand-by" flowchart

action holder: MIPS

action holder: St-by

autonomous action

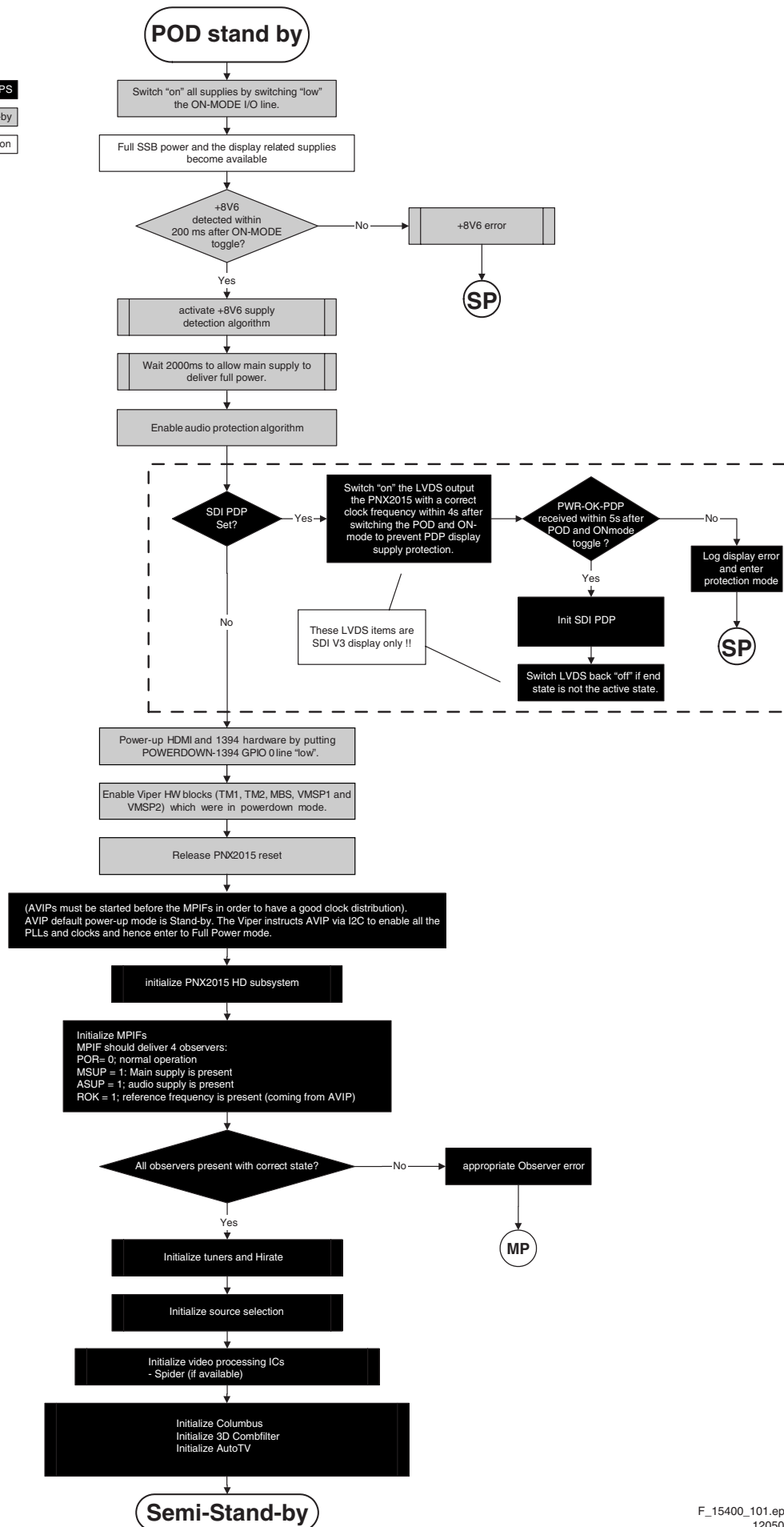


Figure 5-10 "POD Stand-by" to "Semi Stand-by" flowchart

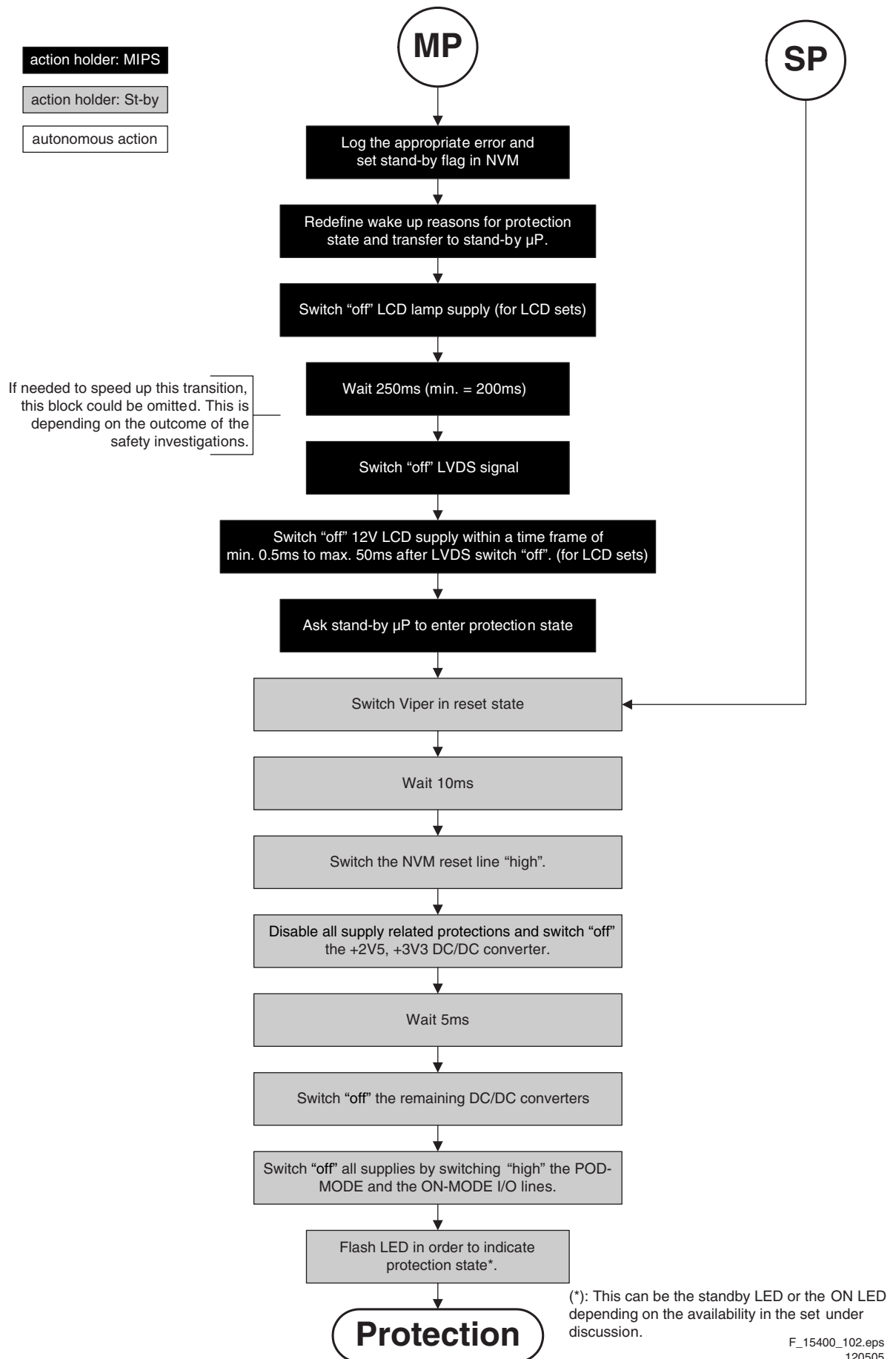


Figure 5-11 "Protection" flowchart

5.4 Service Tools

5.4.1 ComPair

Introduction

ComPair (Computer Aided Repair) is a service tool for Philips Consumer Electronics products. ComPair is a further development on the European DST (service remote control), which allows faster and more accurate diagnostics. ComPair has three big advantages:

1. ComPair helps you to quickly get an understanding on how to repair the chassis in a short time by guiding you systematically through the repair procedures.
2. ComPair allows very detailed diagnostics (on I²C level) and is therefore capable of accurately indicating problem areas. You do not have to know anything about I²C commands yourself because ComPair takes care of this.
3. ComPair speeds up the repair time since it can automatically communicate with the chassis (when the microprocessor is working) and all repair information is directly available. When ComPair is installed together with the Force/SearchMan electronic manual of the defective chassis, schematics and PWBs are only a mouse click away.

Specifications

ComPair consists of a Windows based fault finding program and an interface box between PC and the (defective) product. The ComPair interface box is connected to the PC via a serial (or RS-232) cable.

For this chassis, the ComPair interface box and the TV communicate via a bi-directional service cable via the service connector(s).

The ComPair fault finding program is able to determine the problem of the defective television. ComPair can gather diagnostic information in two ways:

- Automatically (by communicating with the television): ComPair can automatically read out the contents of the entire error buffer. Diagnosis is done on I²C/UART level. ComPair can access the I²C/UART bus of the television. ComPair can send and receive I²C/UART commands to the microcontroller of the television. In this way, it is possible for ComPair to communicate (read and write) to devices on the I²C/UART buses of the TV-set.
- Manually (by asking questions to you): Automatic diagnosis is only possible if the microcontroller of the television is working correctly and only to a certain extent. When this is not the case, ComPair will guide you through the fault finding tree by asking you questions (*e.g. Does the screen give a picture? Click on the correct answer: YES / NO*) and showing you examples (*e.g. Measure test-point I7 and click on the correct oscillogram you see on the oscilloscope*). You can answer by clicking on a link (*e.g. text or a waveform picture*) that will bring you to the next step in the fault finding process.

By a combination of automatic diagnostics and an interactive question / answer procedure, ComPair will enable you to find most problems in a fast and effective way.

How To Connect

This is described in the chassis fault finding database in ComPair.

Caution: It is compulsory to connect the TV to the PC as shown in the picture below (with the ComPair interface in between), as the ComPair interface acts as a level shifter. If one connects the TV directly to the PC (via UART), ICs will be blown!

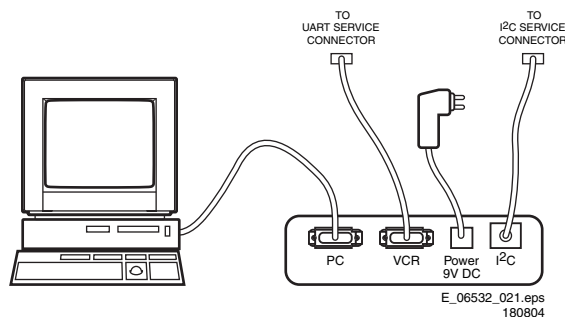


Figure 5-12 ComPair interface connection

How To Order

ComPair order codes:

- ComPair Software: ST4191.
- ComPair Interface Box: 4822 727 21631.
- AC Adapter: T405-ND.
- ComPair Quick Start Guide: ST4190.
- ComPair interface extension cable: 3139 131 03791.
- ComPair UART interface cable: 3122 785 90630.

Note: If you encounter any problems, contact your local support desk.

5.4.2 LVDS Tool

Introduction

This service tool (also called "ComPair Assistant 1") may help you to identify, in case the TV does not show any picture, whether the Small Signal Board (SSB) or the display of a Flat TV is defective.

Furthermore it is possible to program EPLDs with this tool (Byte blaster). Read the user manual for an explanation of this feature.

Since 2004, the LVDS output connectors in our Flat TV models are standardised (with some exceptions). With the two delivered LVDS interface cables (31p and 20p) you can cover most chassis (in special cases, an extra cable will be offered).

When operating, the tool will show a small (scaled) picture on a VGA monitor. Due to a limited memory capacity, it is not possible to increase the size when processing high-resolution LVDS signals (> 1280x960). Below this resolution, or when a DVI monitor is used, the displayed picture will be full size.

Generally this tool is intended to determine if the SSB is working or not. Thus to determine if LVDS, RGB, and sync signals are okay.

How to Connect

Connections are explained in the user manual, which is packed with the tool.

Note: To use the LVDS tool, you must have ComPair release 2004-1 (or later) on your PC (engine version >= 2.2.05). For every TV type number and screen size, one must choose the proper settings via ComPair. The ComPair file will be updated regularly with new introduced chassis information.

How to Order

- LVDS tool (incl. two LVDS cables: 31p and 20p): 3122 785 90671.
- LVDS tool Service Manual: 3122 785 00810.

5.5 Error Codes

5.5.1 Introduction

The error code buffer contains all detected errors since the last time the buffer was erased. The buffer is written from left to right, new errors are logged at the left side, and all other errors shift one position to the right.

When an error has occurred, the error is added to the list of errors, provided the list is not full or the error is a protection error.

When an error occurs and the error buffer is full, then the new error is not added, and the error buffer stays intact (history is maintained), except when the error is a protection error.

To prevent that an occasional error stays in the list forever, the error is removed from the list after 50+ operation hours.

When multiple errors occur (errors occurred within a short time span), there is a high probability that there is some relation between them.

Basically there are three kinds of errors:

- **Errors detected by the Stand-by Processor.** These errors will always lead to protection and an automatic start of the blinking LED for the concerned error (see paragraph "The Blinking LED Procedure"). In these cases SDM can be used to start up (see chapter "Stepwise Start-up").
- **Errors detected by VIPER that lead to protection.** In this case the TV will go to protection and the front LED will blink at 3 Hz. Further diagnosis via service modes is not possible here (see also paragraph "Error Codes" -> "Error Buffer" -> "Extra Info").
- **Errors detected by VIPER that do not lead to protection.** In this case the error can be read out via ComPair, via blinking LED method, or in case you have picture, via SAM.

5.5.2 How to Read the Error Buffer

Use one of the following methods:

- On screen via the SAM (only if you have a picture). E.g.:

- **00 00 00 00 00:** No errors detected
- **06 00 00 00 00:** Error code 6 is the last and only detected error
- **09 06 00 00 00:** Error code 6 was first detected and error code 9 is the last detected error
- Via the blinking LED procedure (when you have no picture). See next paragraph.
- Via ComPair.

5.5.3 How to Clear the Error Buffer

Use one of the following methods:

- By activation of the "RESET ERROR BUFFER" command in the SAM menu.
- With a normal RC, key in sequence "MUTE" followed by "062599" and "OK".
- If the content of the error buffer has not changed for 50+ hours, it resets automatically.

5.5.4 Error Buffer

In case of non-intermittent faults, clear the error buffer before you begin the repair (**before** clearing the buffer, write down the content, as this history can give you significant information). This to ensure that old error codes are no longer present.

If possible, check the entire contents of the error buffer. In some situations, an error code is only the result of another error code and not the actual cause (e.g., a fault in the protection detection circuitry can also lead to a protection). There are several mechanisms of error detection:

- Via error bits in the status registers of ICs.
- Via polling on I/O pins going to the stand-by processor.
- Via sensing of analogue values on the stand-by processor.
- Via a "not acknowledge" of an I²C communication

Take notice that some errors need more than 90 seconds before they start blinking. So in case of problems wait 2 minutes from start-up onwards, and then check if the front LED is blinking.

Table 5-3 Error code overview

Error	Description	Error/Prot	Detected by	Device	Defective module	Result
1	I ² C1	P	VIPER	n.a.	I ² C1_blocked	Protection + 3 Hz blinking
2	I ² C2	P	VIPER	n.a.	I ² C2_blocked	Protection + 3 Hz blinking
3	I ² C3	P	Stby µP	n.a.	/	Protection + Error blinking
4	I ² C4	P	VIPER	n.a.	I ² C4_blocked	Protection + 3 Hz blinking
5	VIPER does not boot	P	Stby µP	PNX8550	/	Protection + Error blinking
6	5V supply	P	Stby µP	n.a.	/	Protection + Error blinking
7	8V6 supply	P	Stby µP	n.a.	/	Protection + Error blinking
8	1.2V DC/DC	P	Stby µP	n.a.	/	Protection + Error blinking
11	3.3V DC/DC	P	Stby µP	n.a.	/	Protection + Error blinking
12	12V supply	P	Stby µP	n.a.	/	Protection + Error blinking
14	Supply Class D amplifiers	P	Stby µP	/	/	Protection + Error blinking
14	Supply Audio part SSB	P	Stby µP	/	/	Protection + Error blinking
17	MPIF1 audio supply	E	VIPER	PNX3000	IF I/O	Error logged
18	MPIF1 ref freq	E	VIPER	PNX3000	IF I/O	Error logged
25	Supply fault	P	Stby µP	/	/	Protection + Error blinking
27	Phoenix	E	VIPER	PNX2015B	HD subsystem	Error logged
28	MOP	E	VIPER	XC3S	Output processor	Error logged
29	AVIP1	E	VIPER	PNX2015	AV input processor 1	Error logged
31	AVIP2	E	VIPER	PNX2015	AV input processor 2	Error logged
32	MPIF1	E	VIPER	PNX3000	/	Error logged
34	Tuner1	E	VIPER	/	Tuner 1	Error logged
37	Channel decoder	E	VIPER	NXT2003	/	Error logged
39	POD Interface	E	VIPER	STV701	/	Error logged
43	Hi Rate Front End	E	VIPER	TDA9975	HDMI	Error logged
44	Main NVM	E	VIPER	M24C64	/	Error logged
45	Columbus 1	E	VIPER	PNX2015	Comb filter	Error logged
53	VIPER	P	Stby µP	PNX8550	/	Protection + Error blinking
63	PDP Display (n.a.)	P	VIPER	/	Display	Protection + 3 Hz blinking

Extra Info

- **Error 1 (I²C bus 1 blocked).** When this error occurs, the TV will go to protection and the front LED will blink at 3 Hz. Now you can partially restart the TV via the SDM shortcut pins on the SSB. Depending on the software version it is possible that no further diagnose (error code read-out) is possible. With the knowledge that only errors 1, 2, 4, and 63 result in a 3 Hz blinking LED, the range of possible defects is limited.
- **Error 2 (I²C bus 2 blocked).** When this error occurs, the TV will go to protection and the front LED will blink at 3 Hz. Now you can partially restart the TV via the SDM shortcut pins on the SSB. Due to hardware restriction (I²C bus 2 is the fast I²C bus) it will be impossible to start up the VIPER and therefore it is also impossible to read out the error codes via ComPair or via the blinking LED method. With the knowledge that only errors 1, 2, 4, and 63 result in a 3 Hz blinking LED, the range of possible defects is limited. When you have restarted the TV via the SDM shortcut pins, and then pressed "CH+" on your remote control, the TV will go to protection again, and the front LED blink at 3 Hz again. This could be an indication that the problem is related to error 2.
- **Error 3 (I²C bus 3 blocked).** There are only three devices on I²C bus 3: VIPER, Stand-by Processor, and NVM. The Stand-by Processor is the detection device of this error, so this error will only occur if the VIPER or the NVM is blocking the bus. This error will also be logged when the NVM gives no acknowledge on the I²C bus (see error 44). Note that if the 12 V supply is missing (connector 1M46 on the SSB), the DC/DC supply on the SSB will not work. Therefore the VIPER will not get supplies and could block I²C bus 3. So, a missing 12 V can also lead to an error 3.
- **Error 4 (I²C bus 4 blocked).** Same remark as with error 1.
- **Error 5 (I²C bus 5 blocked).** This error will point to a severe hardware problem around the VIPER (supplies not OK, VIPER completely dead, I²C link between VIPER and Stand-by Processor broken, etc...).
- **Error 7 (8.6 V error).** Except a physical problem with the 8.6 V itself, it is also possible that there is something wrong with the Audio DC Protection: see paragraph "Hardware Protections" for this.
- **Error 12 (12 V error).** Except a physical problem with the 12 V itself, it is also possible that there is something wrong with the Audio DC Protection: see paragraph "Hardware Protections" for this.
- **Error 14 (Audio supply).** This error combines two fault conditions:
 - First detection is done on the "on-board" audio supplies (SSB). The current through resistor 3A95 (schematic B3E) is measured. An over-current will lead to protection and error 14 blinking.
 - The second detection is done on the audio board itself. Here, the absence of one of the audio supplies is sensed, and will also lead to protection and error 14 blinked. For LCD sets this circuit can be found on schematic SA3, for PDP sets this can be found on schematic C.
- **Error 17 (MPIF audio supply).** This error indicates that the 8V-AUD is missing on pin 98 of the MPIF. The result of this missing supply will be that there is no sound on external sources (you will have sound from tuner).
- **Error 29 (AVIP1).** This error will probably generate extra errors. You will probably also see errors 32 (MPIF) and error 31 (AVIP 2). Error 29 and 31 will always be logged together due to the fact that both AVIPs are inside the PNX2015 and are on the same I²C bus. In this case start looking for the cause around AVIP (part of PNX2015).
- **Error 31 (AVIP2).** See info on error 29.
- **Error 34 (Tuner 1).** When this error is logged, it is not sure that there is something wrong with the tuner itself. It is also possible that there is something wrong with the communication between channel decoder and tuner. See schematic B2B.

- **Error 37 (Channel decoder).** This error will always log error 34 (tuner) extra. This is due to the fact that the tuner I²C bus is coming from the channel decoder.
- **Error 44 (NVM).** This error will never occur because it is masked by error 3 (I²C bus 3). The detection mechanism for error 3 checks on an I²C acknowledge of the NVM. If NVM gives no acknowledge, the stand-by software assumes that the bus is blocked, the TV goes to protection and error 3 will be blinking.
- **Error 53.** This error will indicate that the VIPER has started to function (by reading his boot script, if this would have failed, error 5 would blink) but initialization was never completed because of hardware peripheral problems (NAND flash, ...) or software initialization problems. Possible cause could be that there is no valid software loaded (try to upgrade to the latest main software version).

5.6 The Blinking LED Procedure

5.6.1 Introduction

The blinking LED procedure can be split up into two situations:

- Blinking LED procedure in case of a protection detected by the stand-by processor. In this case the error is automatically blinked. This will be only one error, namely the one that is causing the protection. Therefore, you do not have to do anything special, just read out the blinks. A long blink indicates the decimal digit, a short blink indicates the units.
- Blinking LED procedure in the "on" state. Via this procedure, you can make the contents of the error buffer visible via the front LED. This is especially useful for fault finding, when there is no picture.

When the blinking LED procedure is activated in the "on" state, the front LED will show (blink) the contents of the error-buffer. Error-codes > 10 are shown as follows:

1. "n" long blinks (where "n" = 1 - 9) indicating decimal digit,
2. A pause of 1.5 s,
3. "n" short blinks (where "n" = 1 - 9),
4. A pause of approx. 3 s.
5. When all the error-codes are displayed, the sequence finishes with a LED blink of 3 s,
6. The sequence starts again.

Example: Error 12 9 6 0 0.

After activation of the SDM, the front LED will show:

1. 1 long blink of 750 ms (which is an indication of the decimal digit) followed by a pause of 1.5 s,
2. 2 short blinks of 250 ms followed by a pause of 3 s,
3. 9 short blinks followed by a pause of 3 s,
4. 6 short blinks followed by a pause of 3 s,
5. 1 long blink of 3 s to finish the sequence,
6. The sequence starts again.

5.6.2 How to Activate

Use one of the following methods:

- **Activate the SDM.** The blinking front LED will show the entire contents of the error buffer (this works in "normal operation" mode).
- **Transmit the commands "MUTE" - "062500" - "OK" with a normal RC.** The complete error buffer is shown. Take notice that it takes some seconds before the blinking LED starts.
- **Transmit the commands "MUTE" - "06250x" - "OK" with a normal RC** (where "x" is a number between 1 and 5). When x= 1 the last detected error is shown, x= 2 the second last error, etc.... Take notice that it takes some seconds before the blinking LED starts.

5.7 Protections

5.7.1 Software Protections

Most of the protections and errors use either the stand-by microprocessor or the VIPER controller as detection device. Since in these cases, checking of observers, polling of ADCs, filtering of input values are all heavily software based, these protections are referred to as software protections.

There are several types of software related protections, solving a variety of fault conditions:

- **Protections related to supplies:** check of the 12V, +5V, +8V6, +1.2V, +2.5V and +3.3V.
- **Protections related to breakdown of the safety check mechanism.** E.g. since a lot of protection detections are done by means of the VIPER, failing of the VIPER communication will have to initiate a protection mode since safety cannot be guaranteed anymore.

Remark on the Supply Errors

The detection of a supply dip or supply loss during the normal playing of the set does not lead to a protection, but to a cold reboot of the set.

Protections during Start-up

During TV start-up, some voltages and IC observers are actively monitored to be able to optimize the start-up speed, and to assure good operation of all components. If these monitors do not respond in a defined way, this indicates a malfunction of the system and leads to a protection. As the observers are only used during start-up, they are described in the start-up flow in detail (see paragraph "Stepwise Start-up").

5.7.2 Hardware Protections

There is one hardware protection in this chassis: "Audio DC Protection". This protection occurs when there is a DC voltage on the speakers. In that case the main supply is switched "off", but the stand-by supply is still working.

For the Samsung V4 PDP displays, the 8V6 supply is switched "off" and the LED on the display's Main Supply blinks eleven times, which means there is an overvoltage protection. The front LED of the TV will blink error 7 (8V6 error).

In case of LCD supplies, the 12V supply will drop. This will be detected by the stand-by processor, which will start blinking the 12 V error (error 12).

Repair Tips

- If there is an audio DC protection (DC voltage on your speakers), you will probably see error 12 blink in case of LCD TVs, and error 7 for TVs with SDI displays. To be sure there is an audio DC protection, disconnect the cable between the SSB and the Audio PWB and also the cable between the Main Supply and the Audio PWB. If the TV starts up, it is very likely that there is DC voltage on the speakers. Check, and replace if necessary, the audio amplifiers.
- It is also possible that you have an audio DC protection because of an interruption in one or both speakers (the DC voltage that is still on the circuit cannot disappear through the speakers).

5.8 Fault Finding and Repair Tips

Read also paragraph "Error Codes" - "Extra Info".

5.8.1 Exit "Factory Mode"

When an "F" is displayed in the screen's right corner, this means that the set is in "Factory" mode, and it normally happens after a new SSB has been mounted.

To exit this mode, push the "VOLUME minus" button on the TV's keyboard control for 5 seconds and restart the set

5.8.2 MPIF

Important things to make the MPIF work:

- Supply.
- Clock signal from the AVIP.
- I²C from the VIPER.

5.8.3 AVIP

Important things to make the AVIP work:

- Supplies.
- Clock signal from the VIPER.
- I²C from the VIPER (error 29 and 31).

5.8.4 DC/DC Converter

Introduction

- The best way to find a failure in the DC/DC converters is to check their starting-up sequence at power "on" via the Mains/AC Power cord, presuming that the Stand-by Processor is operational.
- If the input voltage of the DC/DC converters is around 12 V (measured on the decoupling capacitors 2U17/2U25/2U45) and the ENABLE signals are "low" (active), then the output voltages should have their normal values.
- First, the Stand-by Processor activates the +1V2 supply (via ENABLE-1V2).
- Then, after this voltage becomes present and is detected OK (about 100 ms), the other two voltages (+2V5 and +3V3) will be activated (via ENABLE-3V3).
- The current consumption of controller IC 7U00 is around 20 mA (that means around 200 mV drop voltage across resistor 3U22).
- The current capability of DC/DC converters is quite high (short-circuit current is 7 to 10 A), therefore if there is a linear integrated stabilizer that, for example delivers 1.8V from +3V3 with its output overloaded, the +3V3 stays usually at its normal value even though the consumption from +3V3 increases significantly.
- The +2V5 supply voltage is obtained via a linear stabilizer made with discrete components that can deliver a lot of current. Therefore, in case +2V5 (or +2V5D) is short-circuited to GND, the +3V3 will not have the normal value but much less. The +2V5D voltage is available in standby mode via a low power linear stabilizer that can deliver up to 30 mA. In normal operation mode, the value of this supply voltage will be close to +2V5 (20 - 30 mV difference).
- The supply voltages +5V and +8V6 are available on connector 1M46; they are not protected by fuses. +12VSW is protected for over-currents by fuse 1U04.

Fault Finding

- **Symptom:** +1V2, +2V5, and +3V3 not present (even for a short while ~10ms).
 1. Check 12V availability (fuse 1U01, resistor 3U22, power MOS-FETs) and enable signal ENABLE-1V2 (active low).
 2. Check the voltage on pin 9 (1.5 V).
 3. Check for +1V2 output voltage short-circuit to GND that can generate pulsed over-currents 7-10 A through coil 5U03.

4. Check the over-current detection circuit (2U12 or 3U97 interrupted).
- **Symptom:** +1V2 present for about 100 ms. Supplies +2V5 and +3V3 not rising.
 1. Check the ENABLE-3V3 signal (active "low").
 2. Check the voltage on pin 8 (1.5 V).
 3. Check the under-voltage detection circuit (the voltage on collector of transistor 7U10-1 should be less than 0.8 V).
 - 4. Check for output voltages short-circuits to GND (+3V3, +2V5 and +2V5D) that generate pulsed over-currents of 7-10 A through coil 5U00.
 - 5. Check the over-current detection circuit (2U18 or 3U83 interrupted).
- **Symptom:** +1V2 OK, but +2V5 and +3V3 present for about 100 ms. **Cause:** The SUPPLY-FAULT line stays "low" even though the +3V3 and +1V2 is available. The Stand-by Processor is detecting that and switches all supply voltages "off".
 1. Check the value of +2V5 and the drop voltage across resistor 3U22 (they could be too high)
 2. Check if the +1V2 or +3V3 are higher than their normal values. This can be due to defective DC feedback of the respective DC/DC converter (3U18 or 3UA7).
 - **Symptom:** +1V2, +2V5, and +3V3 look okay, except the ripple voltage is increased (audible noise can come from the filtering coils 5U00 or 5U03).
Cause: Instability of the frequency and/or duty cycle of one or both DC/DC converters.
 - Check resistor 3U06, the decoupling capacitors, the AC feedback circuits (2U20 + 2U21 + 3U14 + 3U15 for +1V2 or 2U19 + 2U85 + 3U12 + 3U13 for +3V3), the compensation capacitors 2U09, 2U10, 2U23 and 2U73, and IC 7U00.

Note 1: If fuse 1U01 is broken, this usually means a pair of defective power MOSFETs (7U01 or 7U03). Item 7U00 should be replaced as well in this case.

Note 2: The 12V switch and 8V6 switch (see "DC/DC CONNECTIONS" schematic) are not present on board: they are bypassed by jumpers.

5.9 Software Upgrading

5.9.1 Introduction

The set software and security keys are stored in a NAND-Flash (item 7P80), which is connected to the VIPER via the PCI bus.

It is possible **for the user** to upgrade the **main** software via the USB port. This allows replacement of a software image in a standalone set, without the need of an E-JTAG debugger. A description on how to upgrade the main software can be found in chapter 3 "Directions For Use".

Important: When the NAND-Flash must be replaced, a new SSB must be ordered, due to the presence of the security keys!!! See table "SSB service kits" for the order codes. Perform the following actions after SSB replacement:

1. Set the correct option codes (see sticker inside the TV).
2. Update the TV software (see chapter 3 for instructions).
3. Perform the alignments as described in chapter 8.
4. Check in CSM menu 5 if the HDMI and POD keys are valid.

Table 5-4 SSB service kits (for BL and BP chassis)

Model Number	New SSB order code
42PF9830A/37	3104 328 42601
50PF9630A/37	3104 328 42611
42PF9630A/37	
32PF9630A/37	3104 328 42621
50PF7320A/37	3104 328 42631
42PF7320A/37	
37PF7320A/37	3104 328 42641
32PF7320A/37	3104 328 42651
50PF9830A/37	3104 328 42661
42PF9730A/37	3104 328 42671

5.9.2 Main Software Upgrade

The software image resides in the NAND-Flash, and is formatted in the following way:

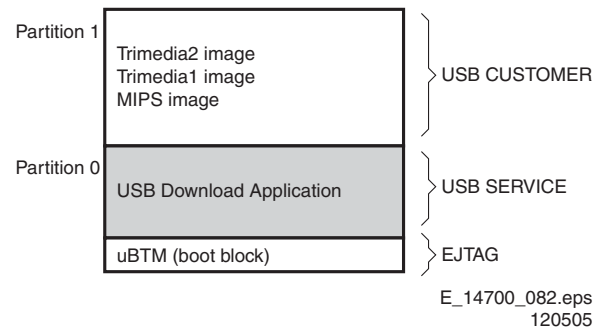


Figure 5-13 NAND-Flash format

Executables are stored as files in a file system. The boot loader (uBTM) will load the USB Download Application in partition 0 (USB drivers, bootscript, etc). This application makes it then possible to upgrade the main software via USB.

Installing "Partition 0" software is possible via an external EJTAG tool, but also in a special way with the USB stick (see description in paragraph "Partition 0").

Partition 1 (Customer)

To do a main software upgrade (partition 1) via USB, the set must be operational, and the "Partition 0" files for the VIPER **must** be installed in the NAND-Flash!

The new software can be uploaded to the TV by using a portable memory device or USB storage compliant devices (e.g. USB memory stick). You can download the new software from the Philips website to your PC.

Partition 0 (Service)

If the "Partition 0" software is corrupted, the software needs to be re-installed.

To upgrade this "USB download application" (partition 0 except the bootblock), insert an USB stick with the correct software, but press the "red" button on the remote control (in "TV" mode) when it is asked via the on screen text.

Caution:

- The USB download application will now erase **both** partitions (except the boot block), so you need to reload the main SW after upgrading the USB download application. As long as this is not done, the USB download application will start when the set is switched "on".
- When something goes wrong during the progress of this method (e.g. voltage dip or corrupted software file), the set will not start up, and can only be recovered via the EJTAG tool!

5.9.3 Manual Start of the Main Software Upgrade Application

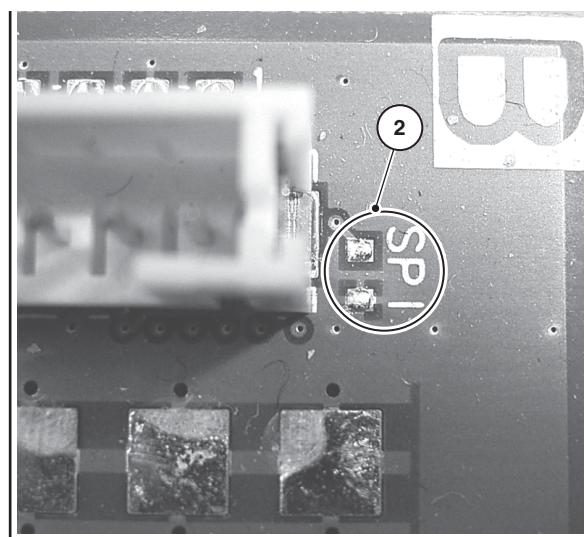
Normally, the software upgrading procedure will start automatically, when a memory device with the correct software is inserted, but in case this does not work, it is possible to force the TV into the software upgrade application. To do so:

- Disconnect the TV from the Mains/AC Power.
- Press the "OK" button on a Philips DVD RC-6 remote control (it is also possible to use the TV remote in "DVD" mode).
- Keep the "OK" button pressed while connecting the TV to the Mains/AC Power.
- The software upgrade application will start.
- When a memory device with upgrade software is connected, the upgrade process will start.

5.9.4 Stand-by Software Upgrade

It will be possible to upgrade the Stand-by software via a PC and the ComPair interface. Check paragraph "ComPair" on how to connect the interface. To upgrade the Stand-by software, use the following steps:

1. Disconnect the TV from the Mains/AC Power.
2. Short circuit the SPI pins [2] on the SSB. They are located outside the shielding (see figure "SPI service pads").
3. Keep the SPI pins shorted while connecting the TV to the Mains/AC Power.
4. Release the short circuit after approx. two seconds.
5. Start up HyperTerminal (can be found in every Windows application via Programs -> Accessories -> Communications -> HyperTerminal. Use the following settings:
 - COM1
 - Bits per second = 19200
 - Data bits = 8
 - Parity = none
 - Stop bits = 1
 - Flow control = Xon / Xoff.
6. Press "Shift U" on your PC keyboard. You should now see the following info:
 - PN2015 Loader V1.0
 - 19-09-2003
 - DEVID=0x05
 - Erasing
 - MCSUM=0x0000
 - =
7. If you do not see the above info, restart the above procedure, and check your HyperTerminal settings and the connections between PC and TV.
8. Via "Transfer" -> "Send text file ...", you can send the proper upgrade file to the TV. This file will be distributed via the Service Organization.
9. After successful programming, you must see the following info:
 - DCSUM=0xECB3
 - :Ok
 - MCSUM=0xECB3
 - Programming
 - PCSUM=0xECB3
 - Finished
10. If you do not see this info, restart the complete procedure.
11. Close HyperTerminal.
12. Disconnect and connect Mains/AC Power again.



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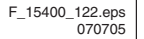
Figure 5-14 SPI service pads

Personal Notes:

6. Block Diagrams and Overviews

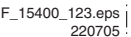
Wiring Diagram

WIRING 42" & 50" PLASMA

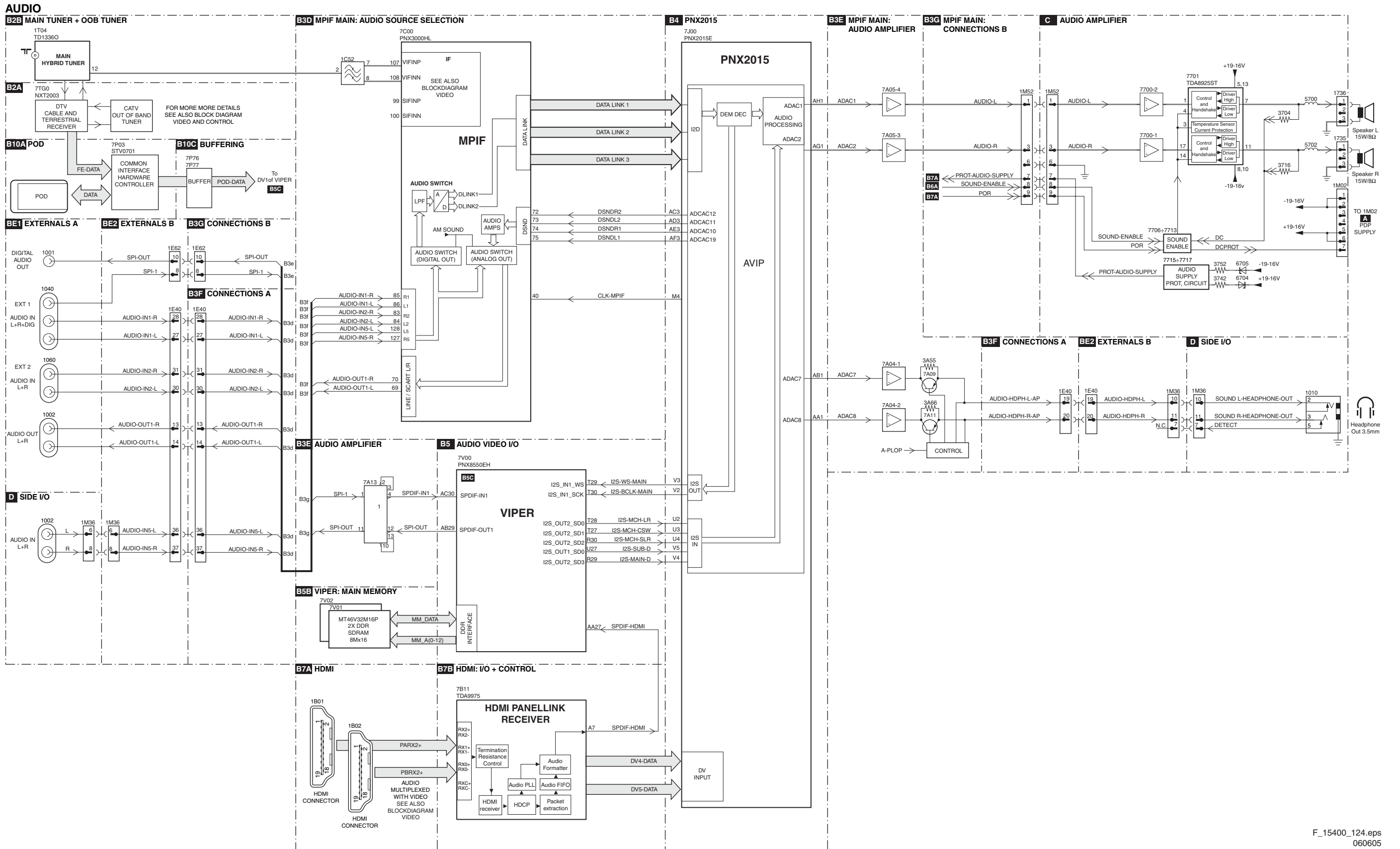


Block Diagram Video

VIDEO $\geq 37^{\circ}$

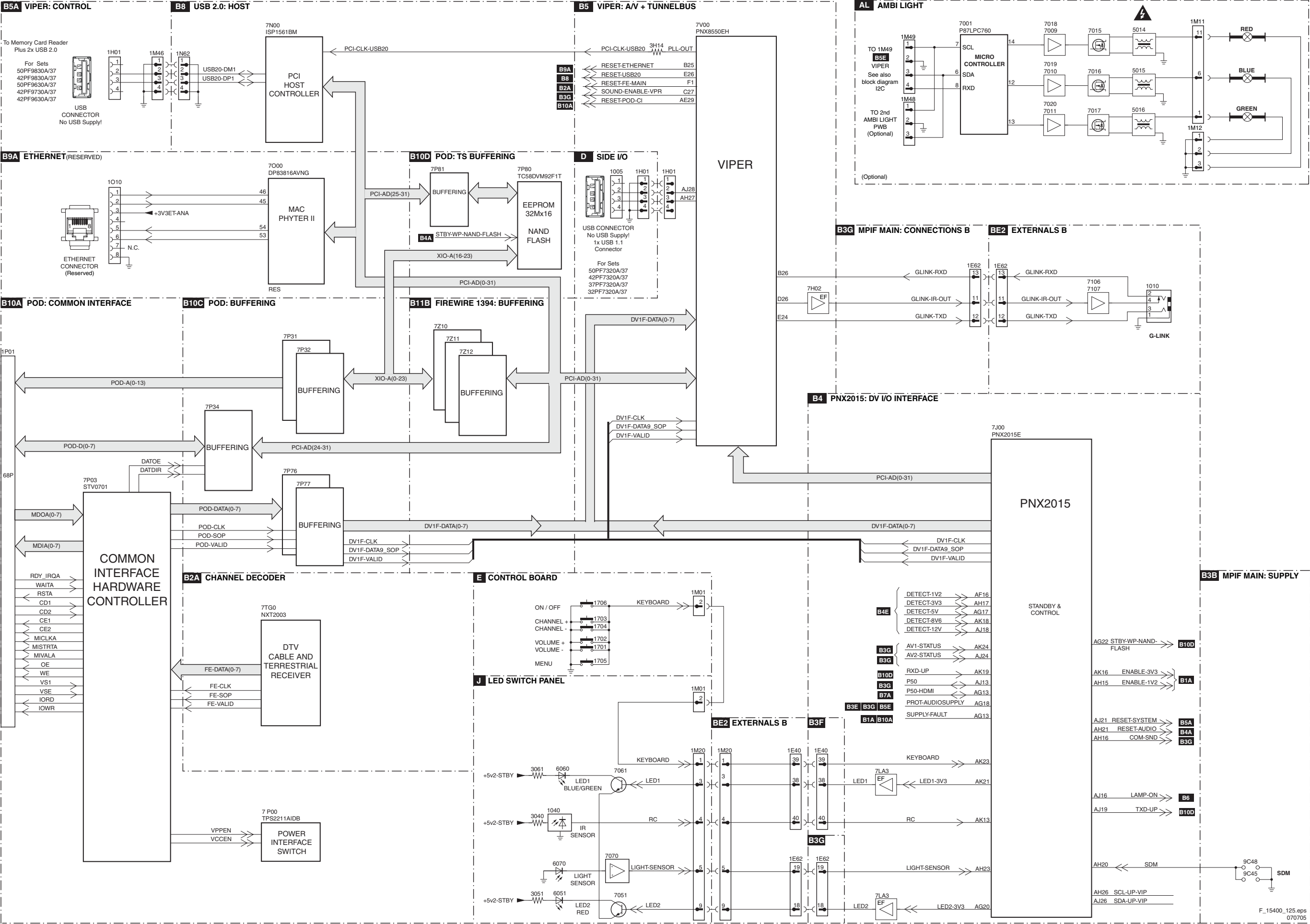


Block Diagram Audio



Block Diagram Control

CONTROL ≥ 37"

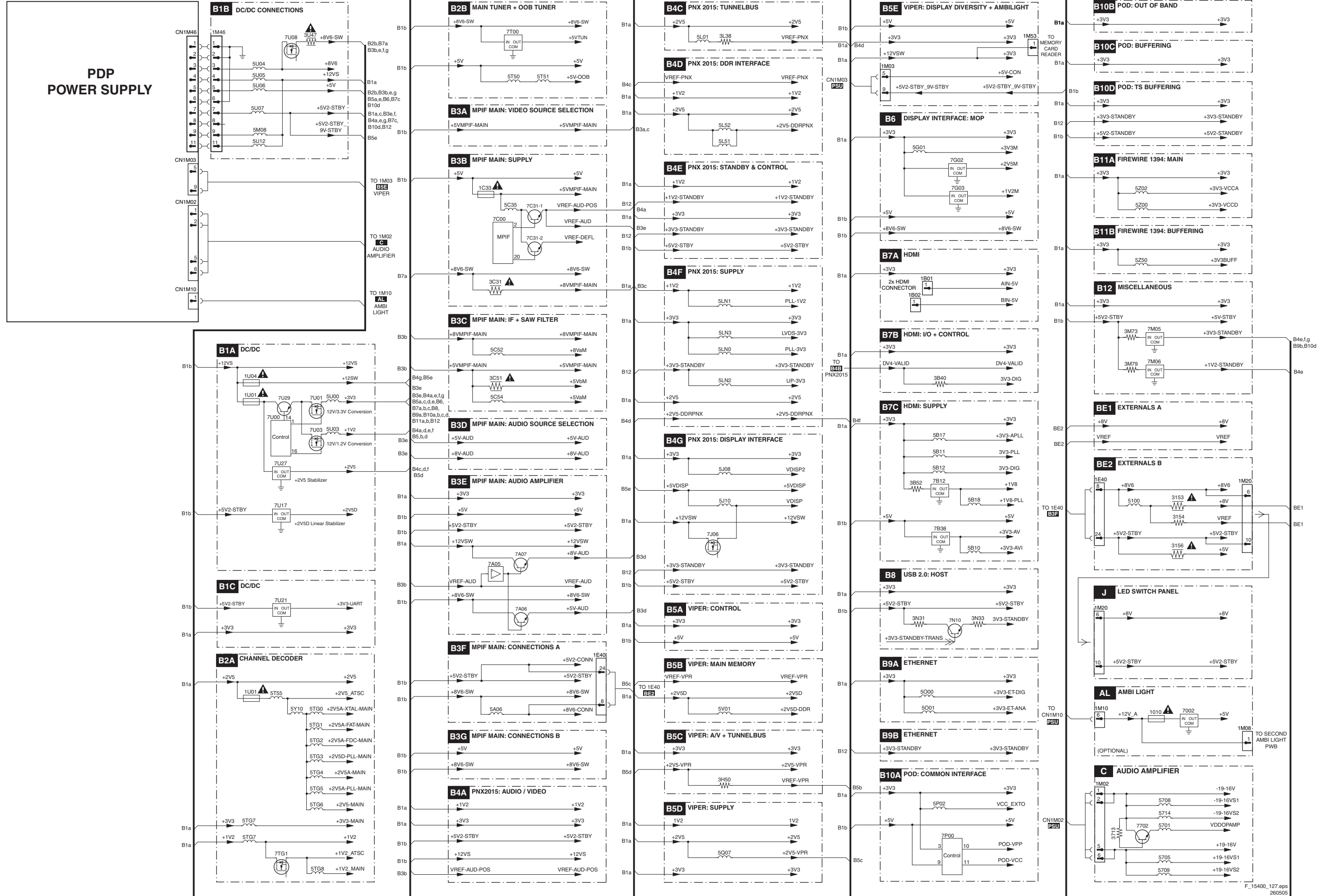


I²C

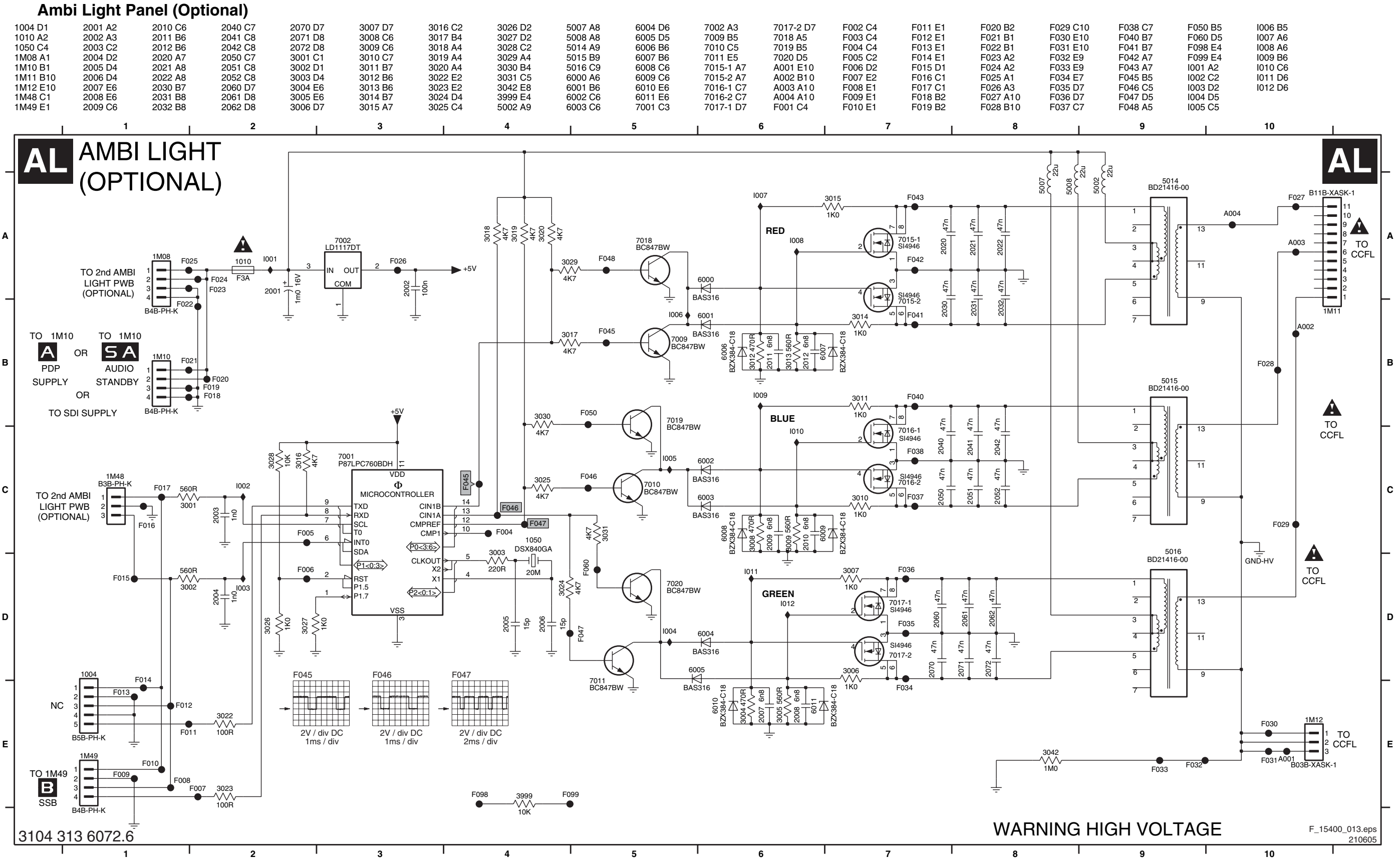


Supply Lines Overview

SUPPLY LINE OVERVIEW



7. Circuit Diagrams and PWB Layouts



1004 B2	2001 B1	2010 B2	2040 A1	2070 A1	3007 B1	3016 B2	3026 B2	5007 B1	6004 B1	7002 B2	7020 B1
1010 B1	2002 B2	2011 B2	2041 A1	2071 A1	3008 B2	3017 B2	3027 B2	5008 B1	6005 B1	7009 B2	
1050 B2	2003 B2	2012 B2	2042 A2	2072 A1	3009 B2	3018 B2	3028 B2	5014 A2	6006 B2	7010 B2	
1M08 B1	2004 B2	2020 A2	2050 A2	3001 B2	3010 B2	3019 B2	3029 B2	5015 A1	6007 B2	7011 B1	
1M10 B1	2005 B2	2021 A2	2051 A2	3002 B2	3011 B2	3020 B2	3030 B2	5016 A1	6008 B2	7015 B2	
1M11 A2	2006 B2	2022 A2	2052 A2	3003 B2	3012 B2	3022 B2	3031 B2	6000 B2	6009 B2	7016 B2	
1M12 A1	2007 B1	2030 A2	2060 A1	3004 B1	3013 B2	3023 B2	3042 A1	6001 B2	6010 B1	7017 B1	
1M48 B2	2008 B1	2031 A2	2061 A1	3005 B1	3014 B2	3024 B2	3999 B1	6002 B2	6011 B1	7018 B2	
1M49 B2	2009 B2	2032 A2	2062 A1	3006 B1	3015 B2	3025 B2	5002 B2	6003 B2	7001 B2	7019 B2	

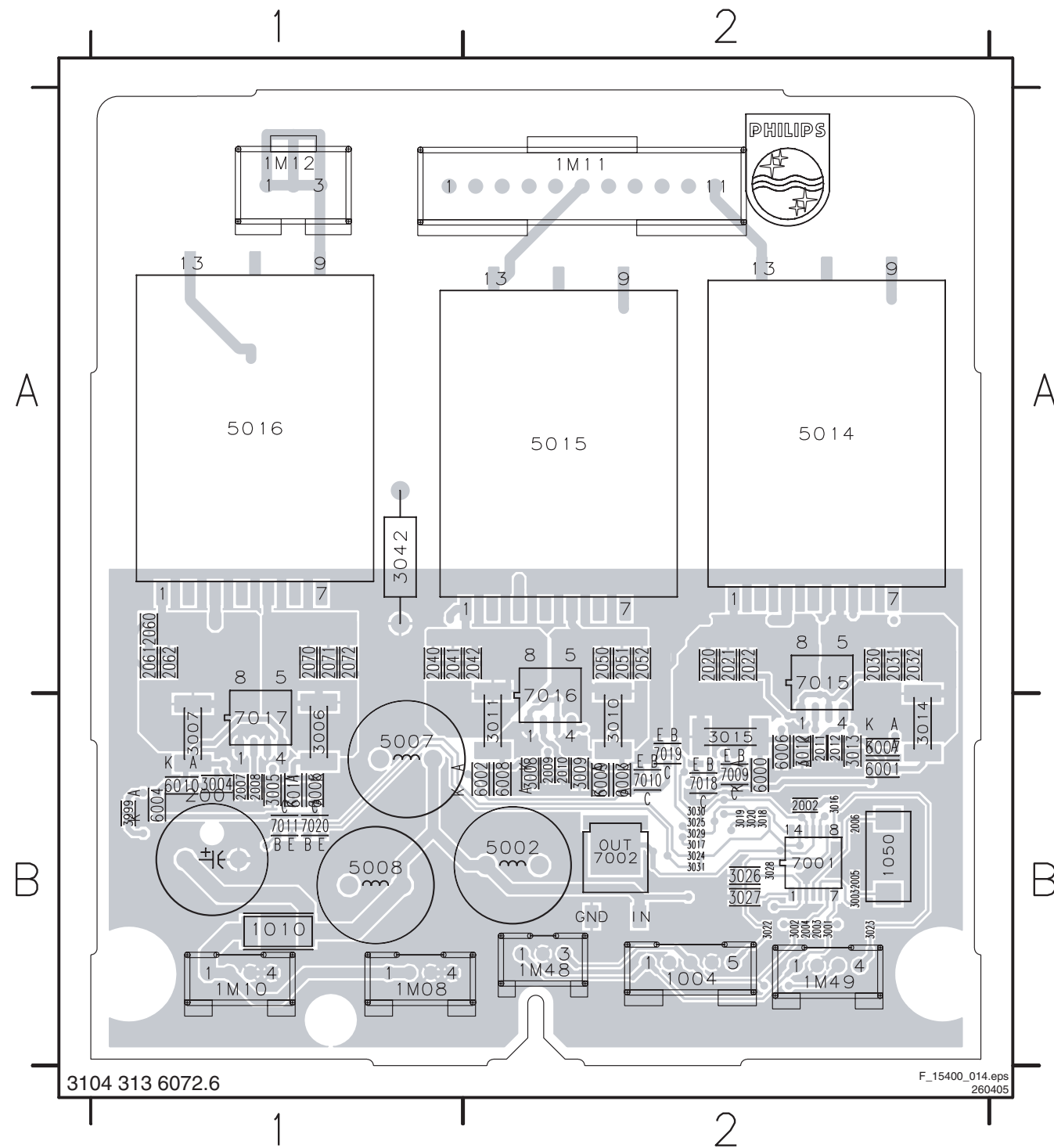
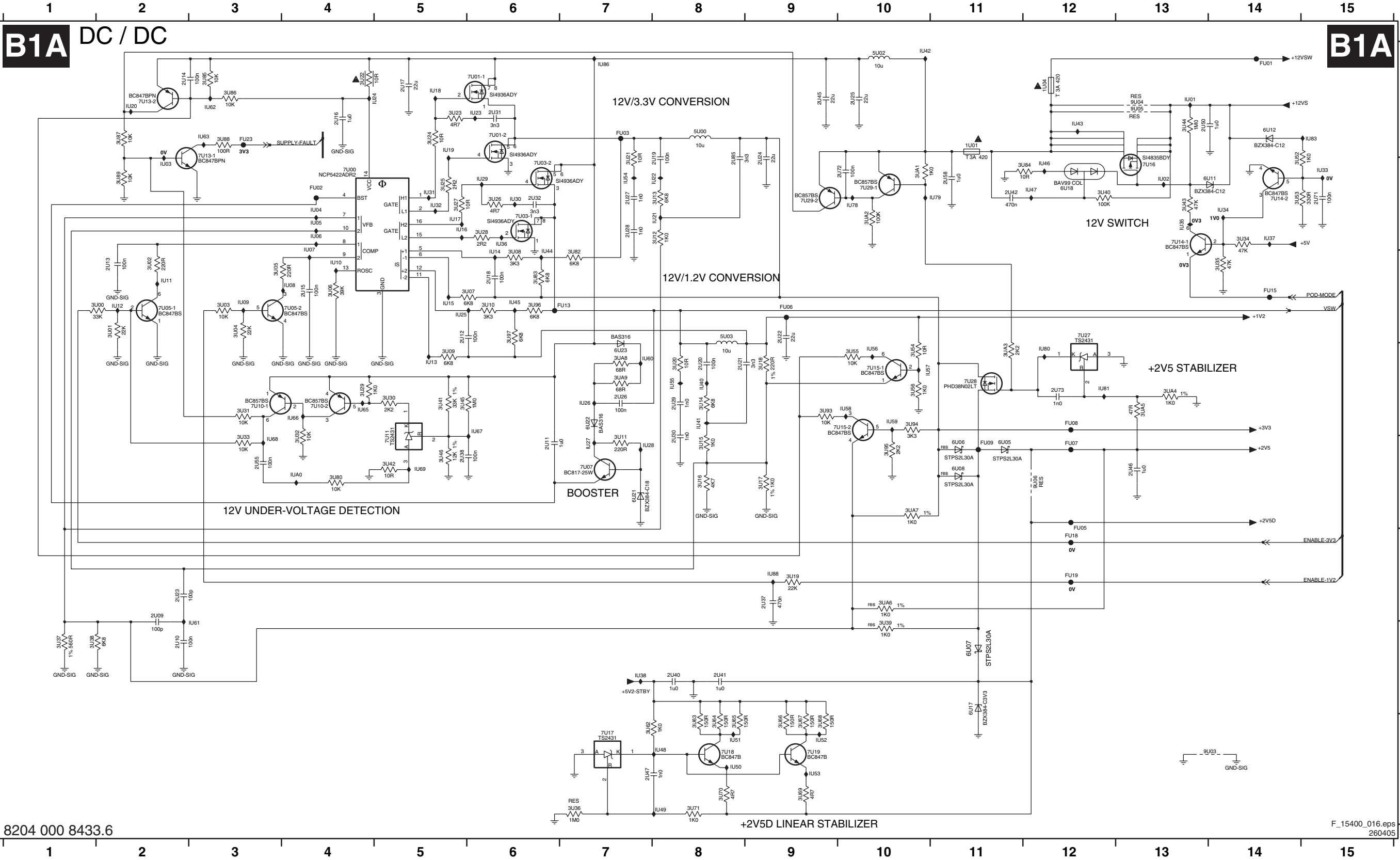


Figure 1: Schematic diagram of the experimental setup. (A) Top view of the microfluidic chip showing the main channel and the inlet/outlet ports. (B) Bottom view of the chip showing the internal network of channels and the location of the two large circular reservoirs. The chip is labeled with '1' and '2' at the top and bottom, and 'A' and 'B' on the left and right sides.

SSB: DC/DC

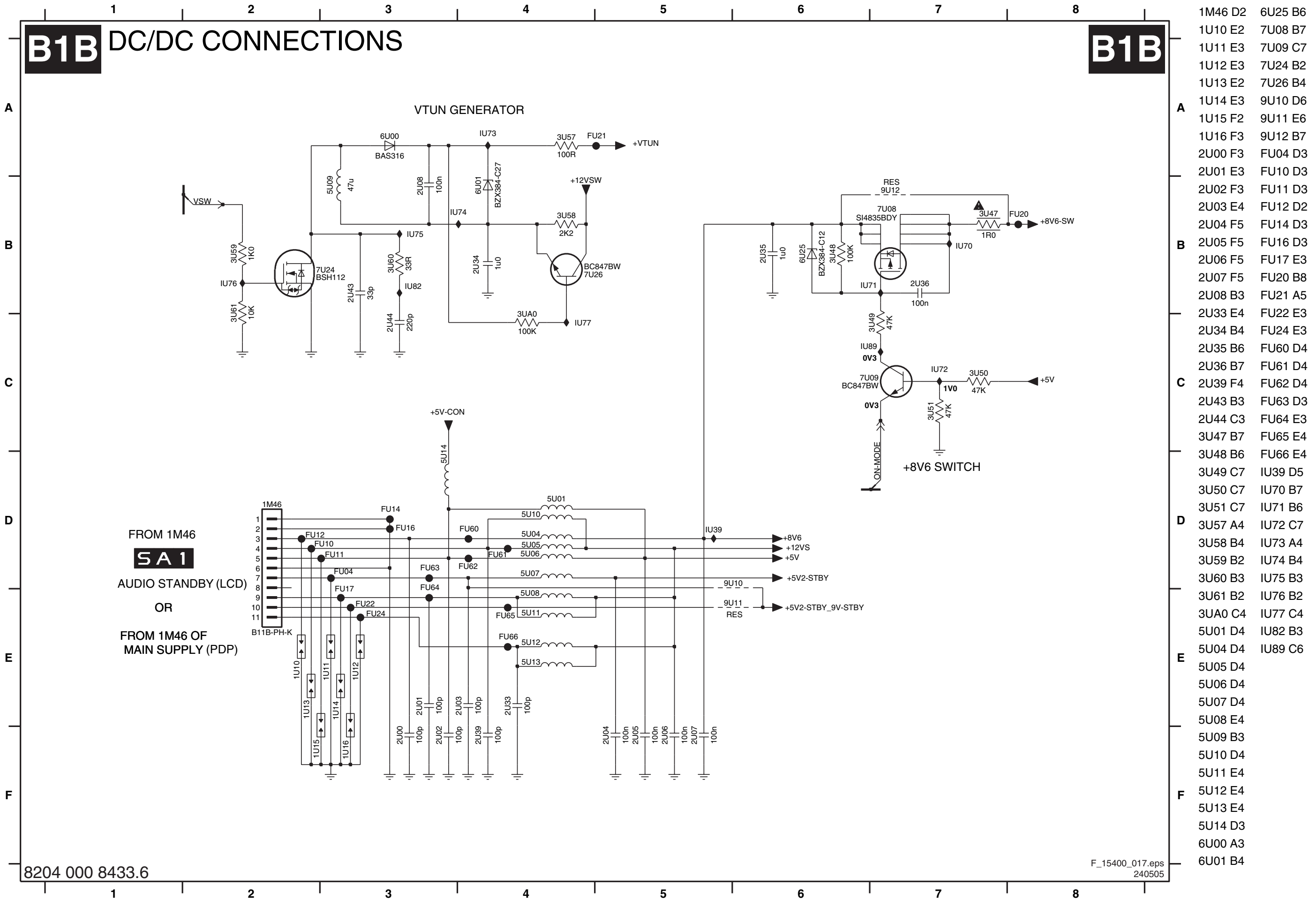
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1U04 A12	2U18 C6	2U28 B7	2U45 A9	3U00 C2	3U10 C6	3U20 D8	3U30 D5	3U40 B12	3U55 D10	3U70 H8	3U89 B2	3U4A D13	6U07 G11	7U01-1 A6	7U13-1 B3	7U27 C12	FU03 A7	FU23 A3	IU10 C4	IU20 A2	IU30 B6	IU41 D8	IU51 H8	IU61 G3	IU80 D12
2U09 F2	2U19 B8	2U29 D8	2U46 E13	3U01 C2	3U11 E7	3U21 B7	3U31 D3	3U41 D5	3U56 D10	3U71 H8	3U93 D9	3U4A D13	6U08 E11	7U01-2 A6	7U13-2 A2	7U28 D11	FU05 F12	IU01 A13	IU11 C2	IU21 B8	IU31 B5	IU42 A10	IU52 H9	IU62 A3	IU81 D12
2U10 G2	2U20 D8	2U30 E8	2U47 H7	3U02 C2	3U12 B8	3U22 A4	3U32 E3	3U42 E5	3U57 H7	3U80 E4	3U94 D10	3U4A D13	6U11 B14	7U03-1 B6	7U14-1 B13	7U29-1 B10	FU06 C9	IU02 B13	IU12 C2	IU22 B8	IU32 B5	IU43 A12	IU53 H9	IU63 A3	IU83 A15
2U11 E6	2U21 D8	2U31 A6	2U50 A13	3U03 C3	3U13 B8	3U23 A5	3U33 E3	3U43 B13	3U58 H8	3U82 C7	3U95 E10	3U4A D13	6U12 A14	7U03-2 B6	7U14-2 B14	7U29-2 B9	FU07 E12	IU03 B2	IU13 D5	IU23 A6	IU33 B15	IU44 C6	IU54 B7	IU65 D4	IU86 A7
2U12 C5	2U22 C9	2U32 B6	2U55 E3	3U04 C3	3U14 D8	3U24 A5	3U34 B14	3U44 A13	3U59 H8	3U83 C6	3U96 C6	3U4A D13	6U17 G11	7U05-1 C2	7U15-1 D10	9U03 H14	FU08 D12	IU04 B4	IU14 C6	IU24 A5	IU34 B14	IU45 C6	IU55 D8	IU66 D4	IU88 F9
2U13 C2	2U23 F2	2U37 F9	2U58 B11	3U05 C3	3U15 E8	3U25 B5	3U35 C14	3U45 D5	3U65 H8	3U84 B12	3U97 C6	3U4A D13	6U18 B12	7U05-2 C4	7U15-2 D10	9U04 A13	FU09 E11	IU05 B4	IU15 C5	IU25 C5	IU35 B13	IU46 B12	IU56 D10	IU67 D6	IU89 E4
2U14 A2	2U24 B9	2U38 E5	2U71 B15	3U06 C4	3U16 E8	3U26 B6	3U36 H7	3U46 E5	3U66 H9	3U85 A3	3U9A B10	3U4A D13	6U21 E7	7U07 E7	7U16 B13	9U05 A13	FU13 C7	IU06 B4	IU16 B5	IU26 D7	IU36 B6	IU47 B12	IU57 D10	IU68 E3	IU90 F9
2U15 C4	2U25 A10	2U40 G8	2U72 B10	3U07 C6	3U17 E9	3U27 B5	3U37 G1	3U47 B14	3U67 H9	3U86 A3	3U9B B10	3U4A D13	6U22 D7	7U10-1 D3	7U17 H7	9U06 E12	FU15 C14	IU07 B4	IU17 B5	IU27 E7	IU37 B14	IU48 H8	IU58 D10	IU69 E5	IU91 F9
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SSB: DC/DC Connections



SSB: RS232 Interface

B1C RS232 INTERFACE

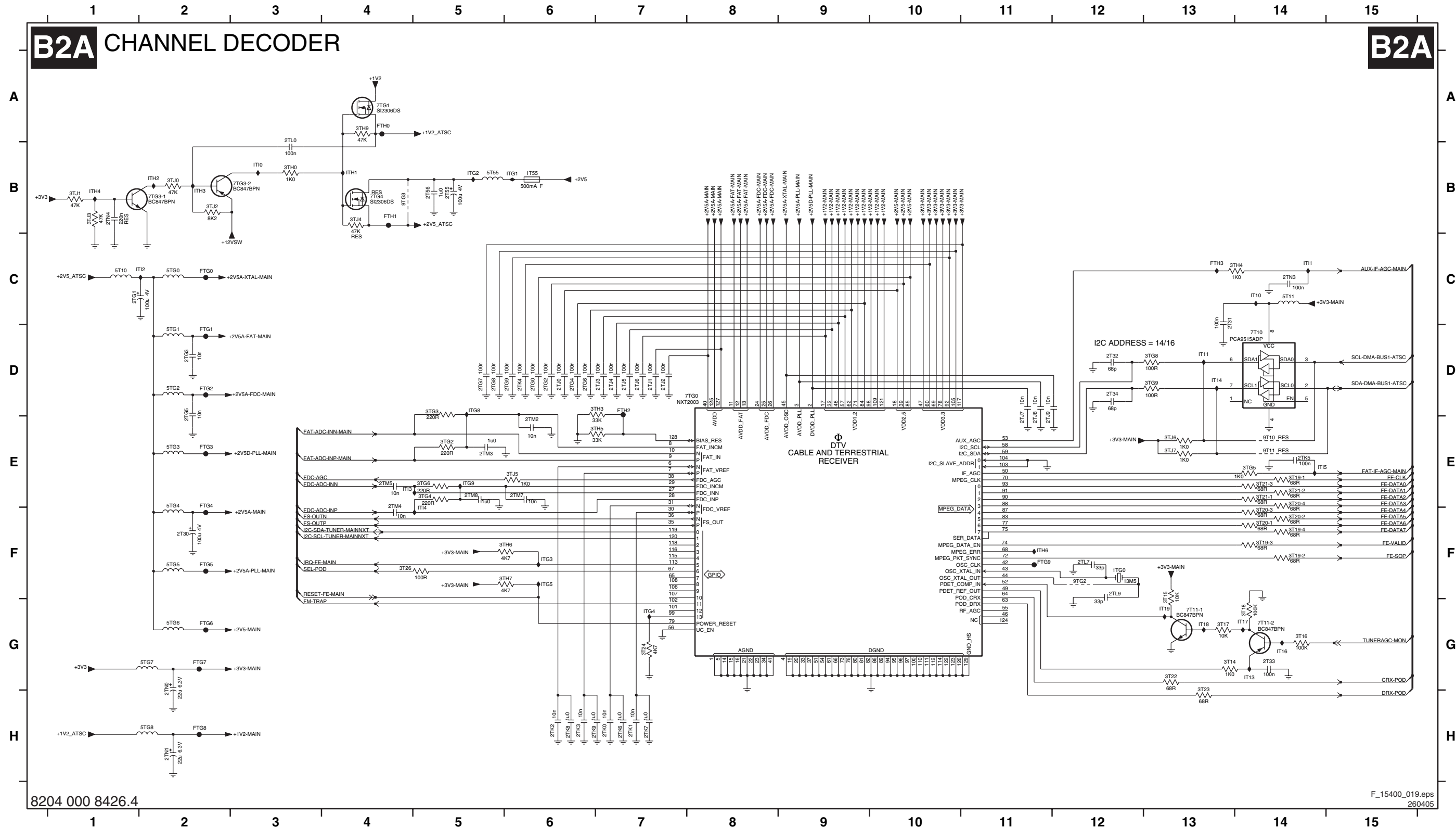
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- 1H07 D1
- 1U02 D8
- 1U03 D8
- 2U60 B3
- 2U61 B3
- 2U63 C5
- 2U64 C6
- 2U65 C6
- 2U66 D5
- 3U72 A3
- 3U73 A4
- 3U74 A2
- 3U75 B3
- 3U76 B3
- 3U77 B3
- 3U79 D7
- 3U81 E7
- 3U90 D3
- 3U91 D2
- 3U92 E3
- 3U98 D7
- 3U99 D7
- 7U20 B3
- 7U21 B2
- 7U22 C5
- 9U01 E5
- 9U02 E5
- 9U07 E2
- 9U13 B5
- 9U14 E5
- 9U15 D4
- 9U16 E4
- FU30 C6
- FU31 D7
- FU32 E7
- FU40 D2
- FU41 D2
- FU42 D2
- FU43 D2
- FU44 D2
- FU45 D2
- FU46 E2
- FU47 E2
- FU48 E2
- FU49 E2
- FU50 E2
- FU51 D8
- FU52 D8
- IU00 D7
- IU64 D7
- IU84 C6
- IU85 D6
- IU87 D5
- IU90 A3
- IU91 B3
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- IU93 C5
- IU94 C5
- IU95 C5
- IU96 D5
- IU97 D7
- IU98 D6
- IU99 E4

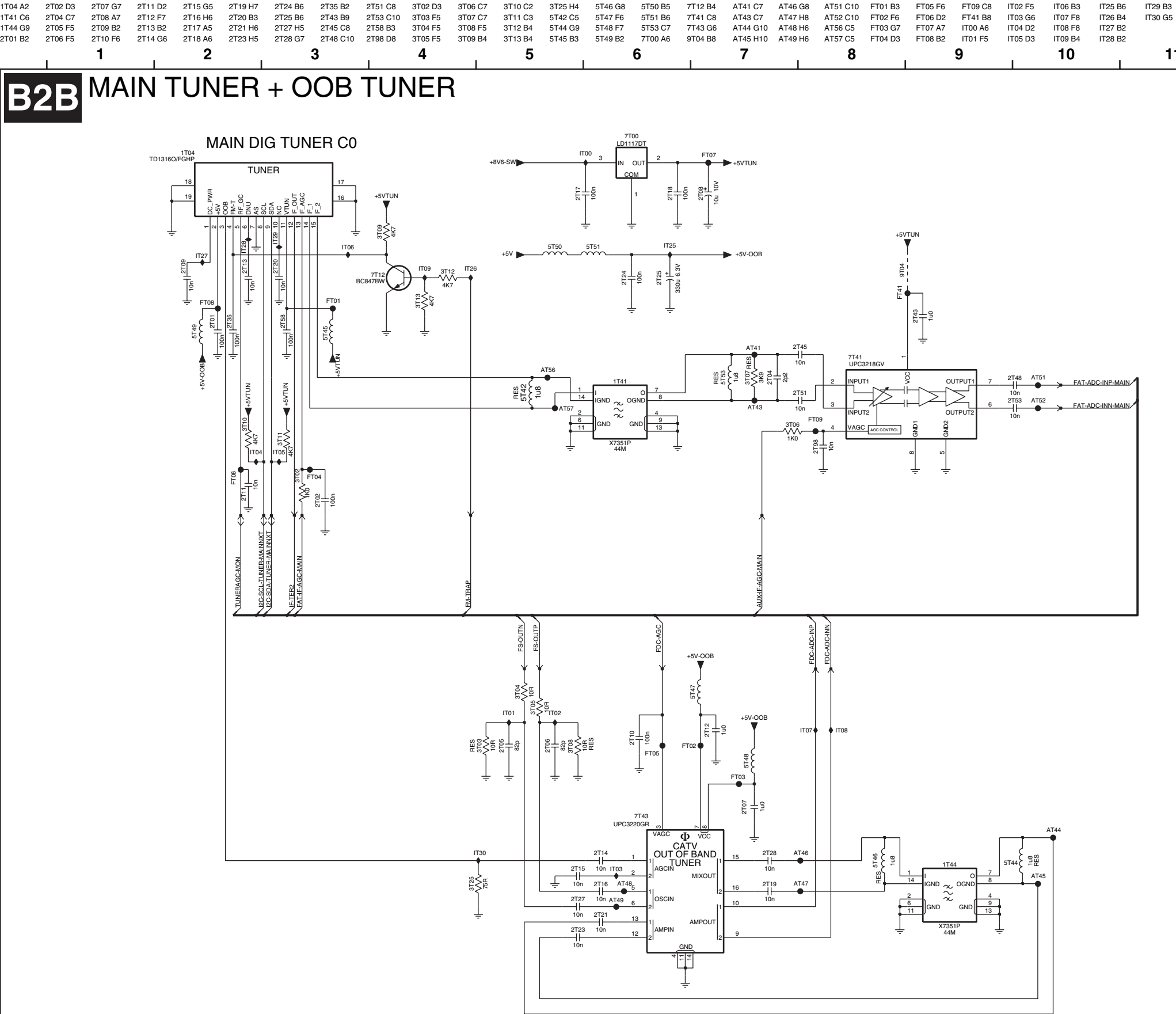
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1TGO F12	2T55 B5	2TG4 D6	2TJ0 D6	2TJ6 D7	2TK2 H6	2TK8 H6	2TM3 E5	2TN1 H2	3T17 G13	3T20-1 F14	3T21-3 E14	3TG3 D5	3TH0 B3	3TH9 A4	3TJ5 E6	5TG0 C2	5TG6 G2	7TG0 D8	9T11 E14	FTG3 E2	FTG9 F11	IT11 D13	IT19 G13	ITG8 D5	ITH6 F11	IT5 E14
2T30 F2	2T56 B5	2TG5 D2	2TJ1 D7	2TJ7 E11	2TK3 H6	2TK9 H7	2TM4 F4	2TN3 C14	3T18 G14	3T20-2 F14	3T22 G13	3TG4 E5	3TH3 D7	3TJ0 B2	3TJ6 E13	5TG1 D2	5TG7 G2	7TG1 A4	9TG2 F12	FTG4 F2	FTH0 A4	IT13 G14	ITG1 B6	ITG9 E5	ITH0 B3	
2T31 C13	2TGO D6	2TG6 D6	2TJ2 D7	2TJ8 E11	2TK4 D6	2TL0 B3	2TM5 E4	2TN4 B1	3T19-1 E14	3T20-3 F14	3T23 H13	3TG5 E14	3TH4 C14	3TJ1 B1	3TJ7 E13	5TG2 D2	5TG8 H2	7TG3-1 B2	9TG3 B4	FTG5 F2	FTH1 B4	IT14 D13	ITG2 B5	ITH1 B4	IT11 C14	
2T32 D12	2TG1 C1	2TG7 D5	2TJ3 D7	2TJ9 E11	2TK5 E14	2TL7 F12	2TM7 E6	3T14 G13	3T19-2 F14	3T20-4 E14	3T24 G7	3TG6 E5	3TH5 E7	3TJ2 B2	5T10 C1	5TG3 E2	7T10 D14	7TG3-2 B3	FTG0 C2	FTG6 G2	FTH2 D7	IT16 G14	ITG3 F6	ITH2 B2	IT12 C2	
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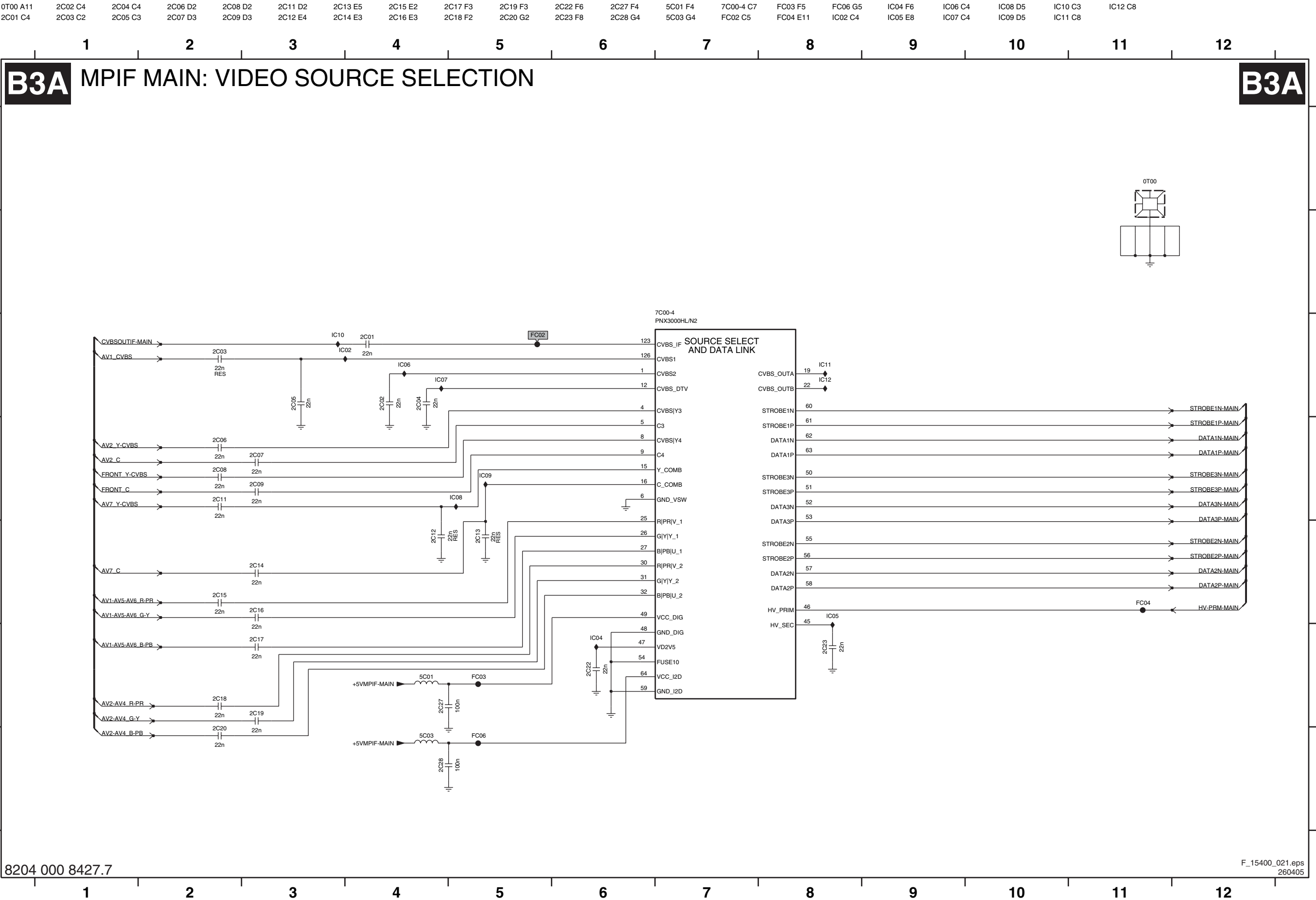
SSB: Main Tuner & OOB Tuner



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SSB: MPIF Main: Video Source Selection



SSB: MPIF Main: Supply



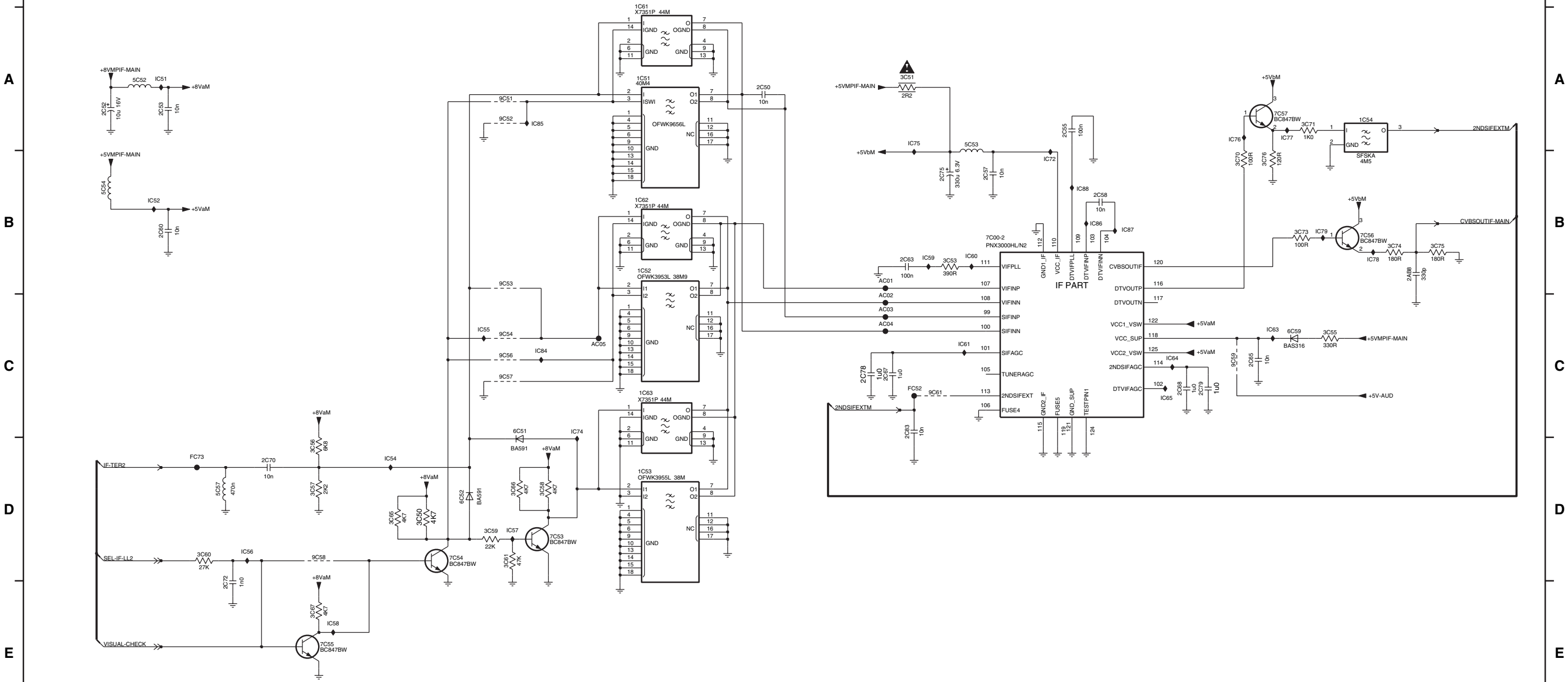
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2C34 H4
2C35 C4
2C36 C5
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2C40 D6
2C41 B5
2C42 C5
2C43 A7
2C44 E5
2C45 D7
2C46 C5
3C30 A6
3C31 I7
3C32 B6
3C33 E4
3C34 B6
3C35 H3
3C36 H4
3C37 H3
3C38 I3
3C39 E5
3C40 F5
3C41 F6
3C42 I3
3C43 C6
3C44 D6
3C45 C5
3C46 H3
3C47 I4
5C33 D7
5C34 D6
5C35 A7
5C36 D5
5C37 G2
7C00-3 A3
7C31-1 A6
7C31-2 C6
7C32-1 H3
7C32-2 H3
9C46 G10
9C47 G10
9C48 G10
9C49 F6
9C50 A7
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FC32 A7
FC36 D6
FC37 D6
FC38 D4
FC40 F7
FC41 F7
IC01 H3
IC32 C5
IC33 H2
IC34 H3
IC35 F7
IC36 A5
IC37 B6
IC38 B6
IC39 H4
IC40 I3
IC41 G3
IC44 E4
IC45 F4
IC46 E4
IC47 C4
IC81 C6
IC82 C6
IC83 A6
IC89 E4

SSB: MPIF Main: IF & SAW Filter

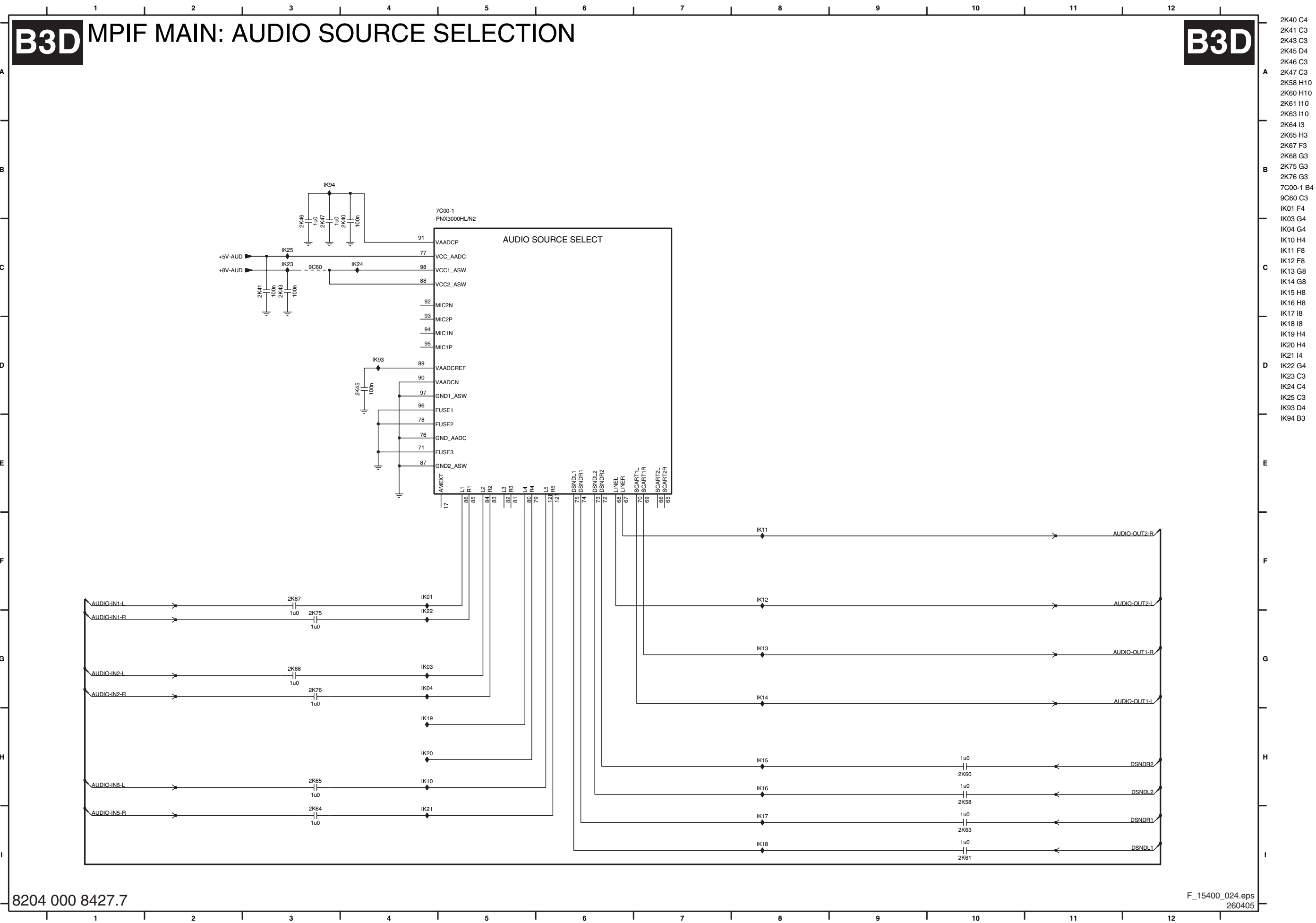
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1C52 B4	1C62 B5	2C52 A1	2C58 B8	2C67 C6	2C75 B7	3C50 D3	3C56 D2	3C60 D1	3C67 E2	3C74 B10	5C53 A7	6C52 D3	7C54 D3	9C51 A4	9C56 C4	9C61 C7	AC04 C6	IC51 A1	IC56 D2	IC60 B7	IC65 C8	IC76 A9	IC84 C4	IC88 B8
1C53 D4	1C63 C5	2C53 A1	2C60 B1	2C68 C8	2C78 C6	3C51 A6	3C57 D2	3C61 D4	3C70 B9	3C75 B10	5C54 B1	6C59 C9	7C55 E2	9C52 A4	9C57 C4	AC01 B6	AC05 C4	IC52 B1	IC57 D4	IC61 C7	IC72 B7	IC77 A9	IC85 A4	
1C54 A10	2AB8 B10	2C55 A7	2C63 B6	2C70 D2	2C79 C8	3C53 B7	3C58 D4	3C65 D3	3C71 A9	3C76 B9	5C57 D2	7C00-2 B7	7C56 B10	9C53 B4	9C58 D2	AC02 C6	FC52 C6	IC54 D3	IC58 E2	IC63 C9	IC74 C4	IC78 B10	IC86 B8	

B3C MPIF MAIN: IF + SAW FILTER

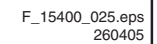
B3C



SSB: MPIF Main: Audio Source Selection

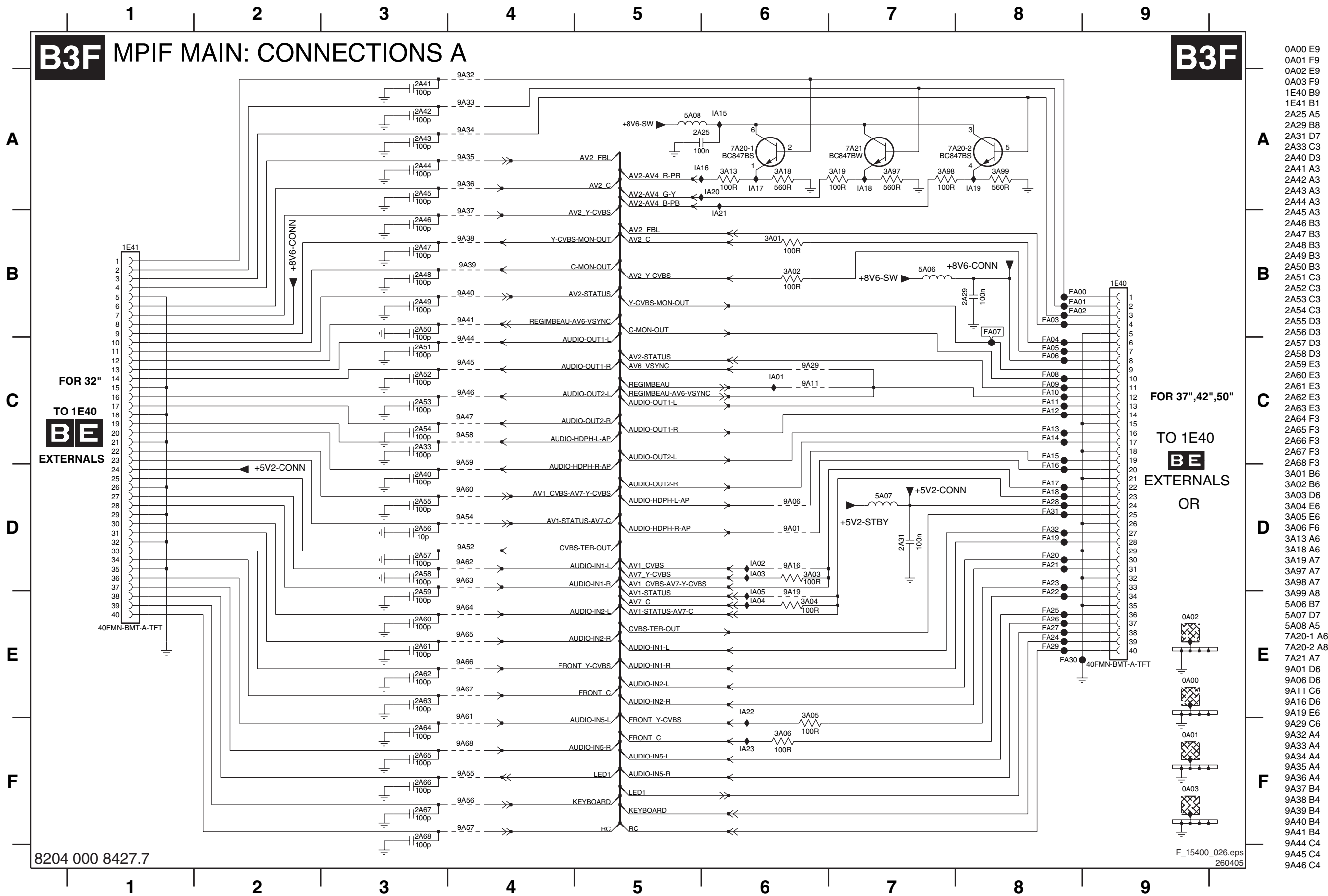


B3E MPIF MAIN: AUDIO AMPLIFIER



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2A22 C8	6A02 A3
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2A24 I12	7A0A2 C9
2A32 B7	7A05-1 F6
2A79 F8	7A05-2 E5
2A81 F7	7A05-3 F2
2A83 E9	7A05-4 H2
2A85 B6	7A06-1 B0
2A85 D9	7A07 E7
2A86 C9	7A08-1 A4
2A87 B6	7A08-2 A5
2A88 B5	7A09 A8
2A89 G3	7A10-1 C8
2A90 I3	7A10-2 B9
2A91 B3	7A11 C11
2A93 C10	7A12-1 D11
2A96 H3	7A12-2 D12
2A97 D10	7A13-1 H10
2A99 B7	7A13-2 H12
2A00 B8	7A13-3 I10
2A01 D10	7A13-4 I12
2A02 C12	7A13-5 H10
2A03 G9	7A13-6 H11
2A04 G9	7A14-1 E3
2A05 E2	7A14-2 E4
2A06 E3	7A15 A11
2A07 B7	7A16-1 B10
2A08 B6	7A16-2 C13
2A08 E4	7A16-1 F9
2A07 F8	7A18-2 E8
3A14 F2	9A80 I3
3A15 H9	9A81 H3
3A16 I3	9A82 B6
3A17 I3	9A83 D9
3A20 E9	9A86 D4
3A21 E10	9A88 H10
3A22 B6	9A90 F3
3A23 B7	9A92 B7
3A24 I2	FK01 B8
3A25 I3	FK02 B9
3A26 E2	FK03 E7
3A27 G3	FK06 C7
3A28 B3	FK07 C9
3A29 D10	FK09 C10
3A30 B7	FK11 C12
3A31 A5	FK17 D11
3A32 B5	FK17 G9
3A33 B7	FK19 I13
3A34 C9	K02 F8
3A35 C9	K05 D11
3A36 D9	K30 A10
3A37 D10	K31 D4
3A38 B7	K32 A11
3A39 I3	K33 B11
3A40 G3	K35 E7
3A41 F7	K36 E8
3A42 B7	K37 B6
3A43 G8	K47 I13
3A44 G8	K48 G3
3A45 G8	K49 E10
3A46 E6	K50 C6
3A47 E6	K51 A3
3A48 F7	K52 A3
3A49 F7	K53 A4
3A50 F7	K54 A4
3A51 A3	K55 B9
3A52 A4	K56 H12
3A53 A4	K57 G9
3A54 B5	K58 I12
3A55 A8	K59 H11
3A56 B7	K60 I12
3A57 B8	K62 B8
3A58 B8	K63 B7
3A59 B8	K64 B8
3A60 A9	K65 B8
3A61 B9	K66 C8
3A62 B9	K67 B6
3A63 C8	K68 A6
3A64 B9	K69 B6
3A65 C8	K70 G2
3A66 C11	K71 F4
3A67 C12	K72 H9
3A68 C12	K73 H4
3A69 C12	K74 F7
3A70 C11	K75 F7
3A71 D11	K76 G7
3A72 D11	K77 G7
3A73 D10	K78 E7
3A74 D11	K79 F7
3A75 D12	K80 C11
3A76 D11	K81 C11
3A77 G9	K82 D11
3A78 G9	K83 D10
3A79 H11	K84 D12
3A80 E11	K85 C12
3A81 E2	K86 C9
3A82 E2	K87 D9
3A83 D3	K88 D9
3A84 E4	K89 E3
3A85 F3	K90 E3
3A86 H12	K91 E2
3A87 A10	K92 F3
3A88 B11	K95 F2
3A89 D13	K96 C8
3A90 F8	K97 E4
3A91 F8	K98 G3
3A92 E7	K99 I3
3A93 E8	
3A94 F8	
3A95 D7	
3A96 F8	
3A01 G3	
3A02 H3	

SSB: MPIF Main: Connections A



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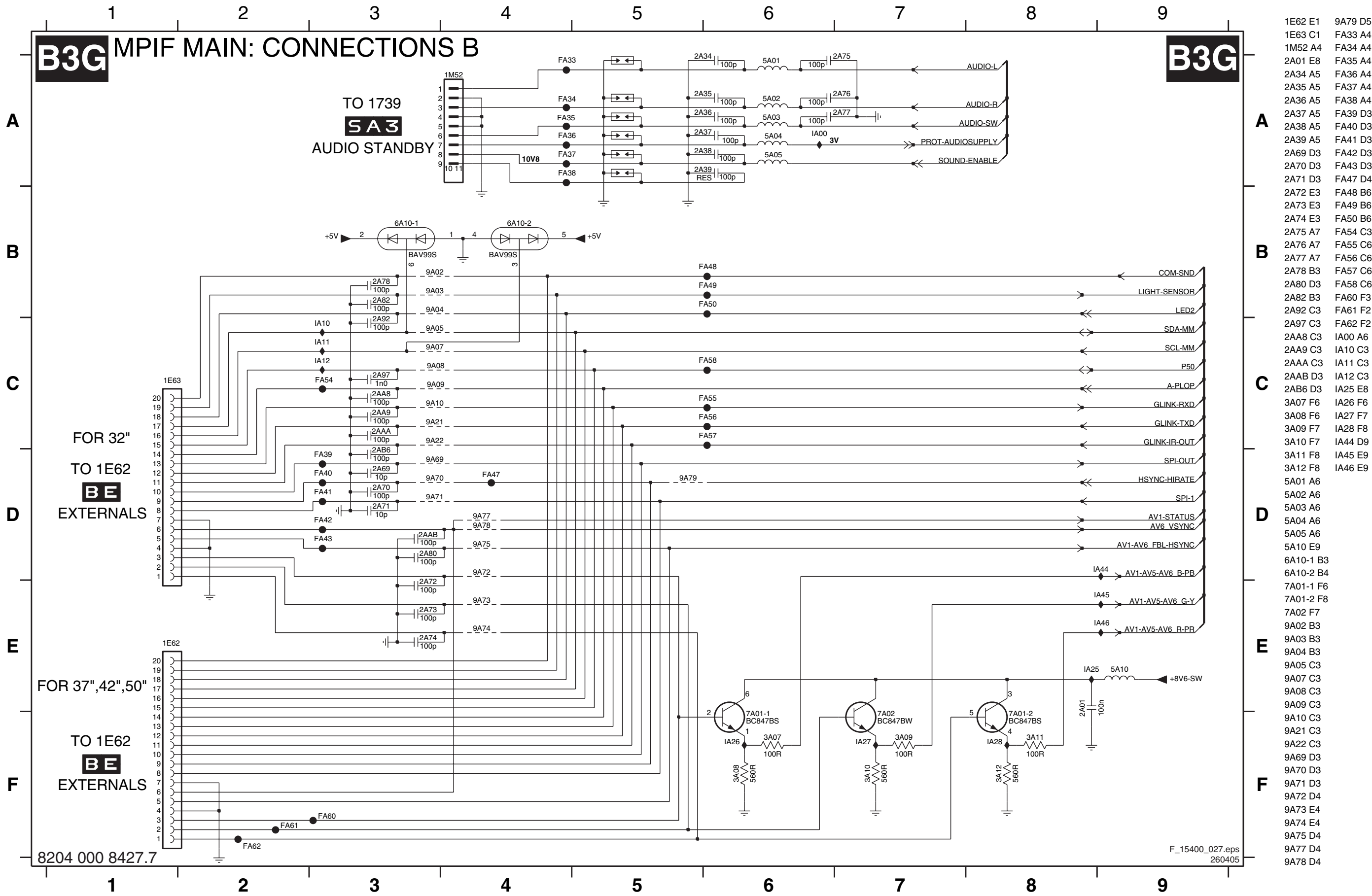
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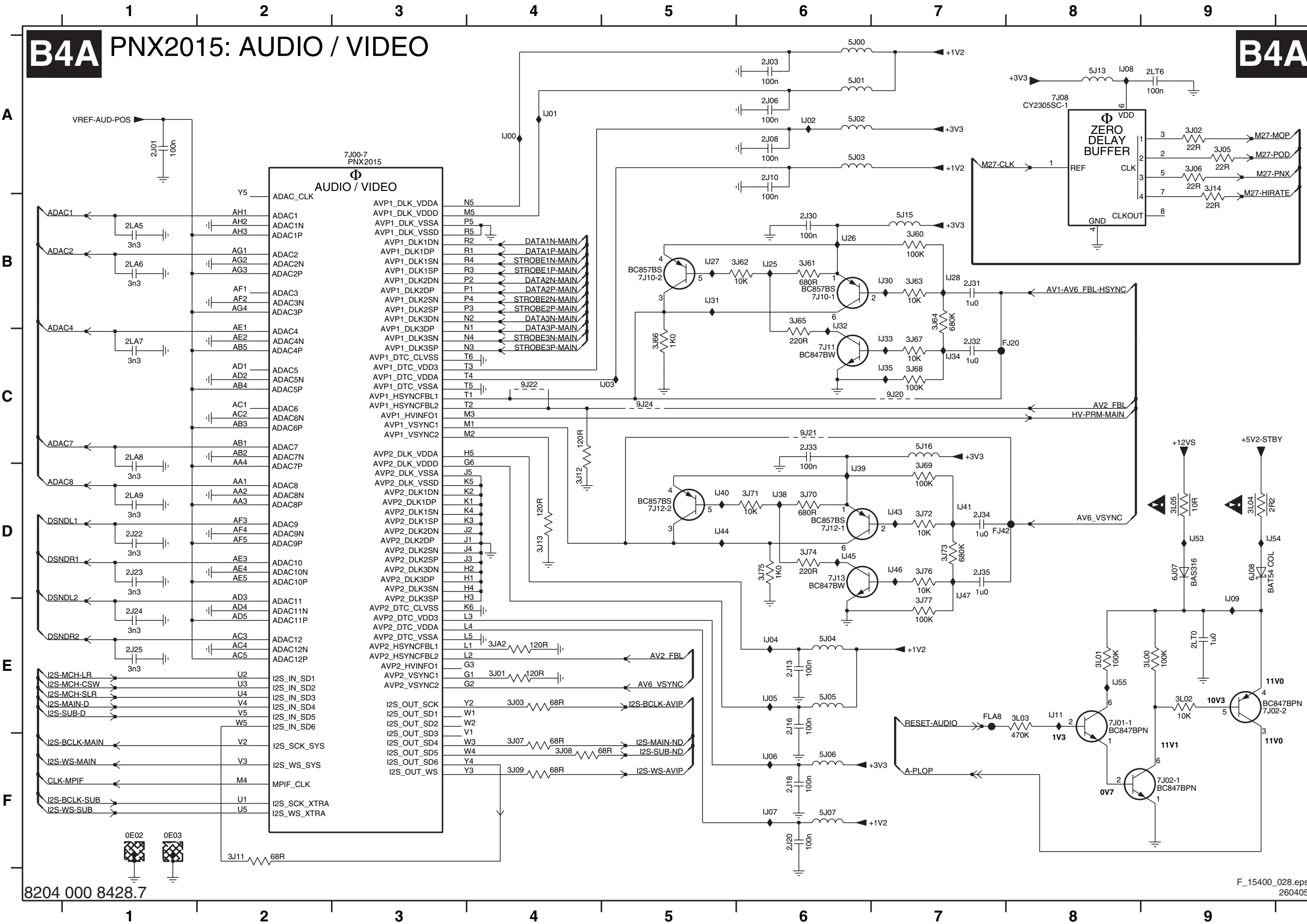
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SSB: MPIF Main: Connections B



SSB: PNX2015: Audio/Video

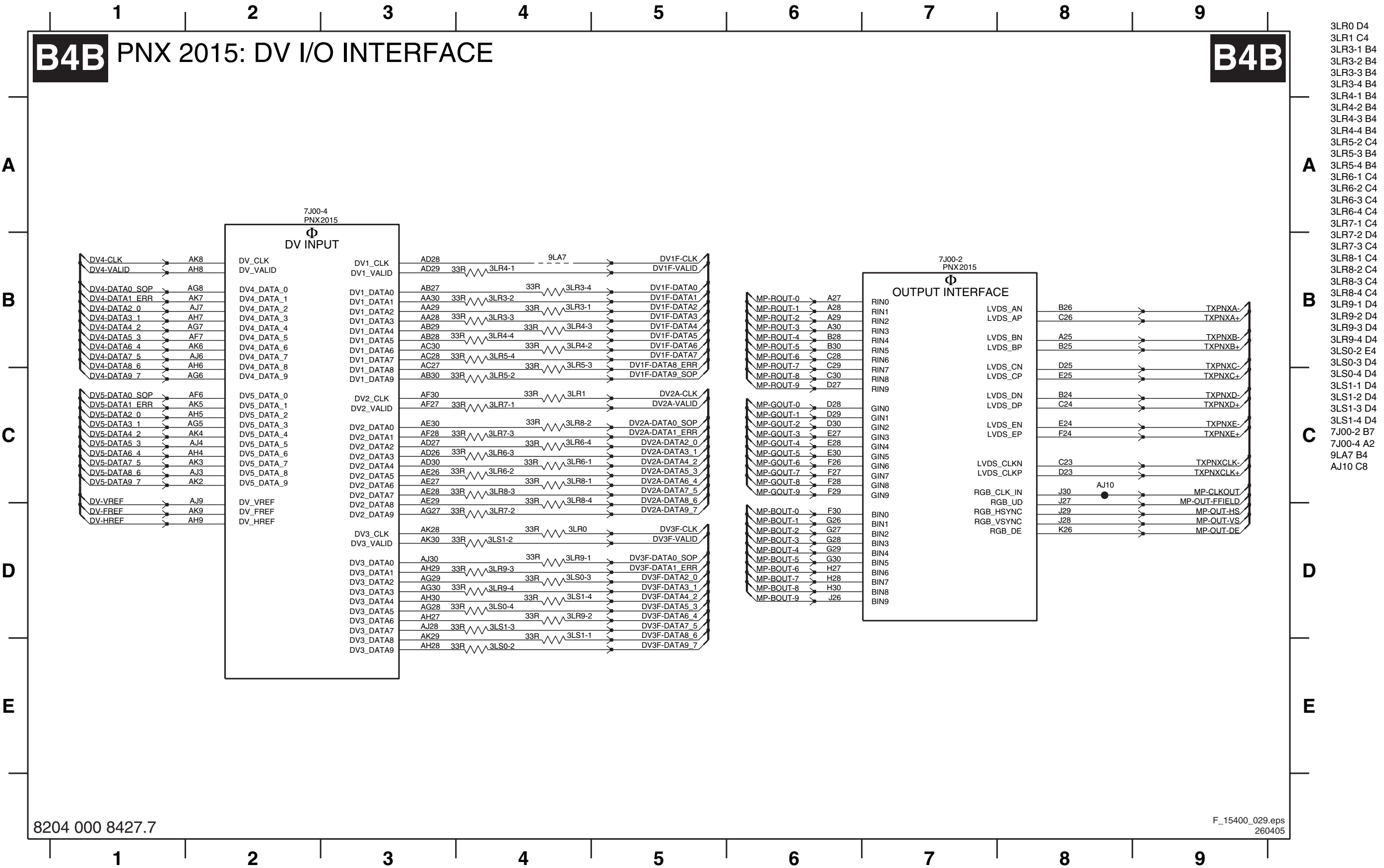


0E02 F1	5J01 A6
0E03 F1	5J02 A6
2J01 A1	5J03 A6
2J03 A6	5J04 E6
2J06 A6	5J05 E6
2J08 A6	5J06 F6
2J10 A6	5J07 F6
2J13 E6	5J13 A8
2J16 E6	5J15 B7
2J18 F6	5J16 C7
2J20 F6	6J07 D9
2J22 D1	6J08 D9
2J23 D1	7J00-7 A3
2J24 E1	7J01-1 E8
2J25 E1	7J02-1 F9
2J30 B6	7J02-2 E9
2J31 B7	7J08 A8
2J32 C7	7J10-1 B6
2J33 C6	7J10-2 B5
2J34 D7	7J11 C6
2J35 D7	7J12-1 D6
2LA5 B1	7J12-2 D5
2LA6 B1	7J13 D6
2LA7 C1	9J20 C7
2LA8 C1	9J21 C6
2LA9 D1	9J22 C4
2LT0 E9	9J24 C5
2LT6 A9	FJ20 C8
3J01 E4	FJ42 D7
3J02 A9	FLA8 E7
3J03 E4	IJ00 A4
3J05 A9	IJ01 A4
3J06 A9	IJ02 A6
3J07 F4	IJ03 C5
3J08 F4	IJ04 E6
3J09 F4	IJ05 E6
3J11 F2	IJ06 F6
3J12 D4	IJ07 F6
3J13 D4	IJ08 A8
3J14 A9	IJ09 E9
3J60 B7	IJ11 E8
3J61 B6	IJ25 B6
3J62 B6	IJ26 B6
3J63 B7	IJ27 B5
3J64 B7	IJ28 B7
3J65 B6	IJ30 B7
3J66 C5	IJ31 B5
3J67 C7	IJ32 B6
3J68 C7	IJ33 C7
3J69 C7	IJ34 C7
3J70 D6	IJ35 C7
3J71 D6	IJ38 D6
3J72 D7	IJ39 D6
3J73 D7	IJ40 D5
3J74 D6	IJ41 D7
3J75 D6	IJ43 D7
3J76 D7	IJ44 D5
3J77 D7	IJ45 D6
3JA2 E4	IJ46 D7
3L00 E9	IJ47 D7
3L01 E8	IJ53 D9
3L02 E9	IJ54 D9
3L03 E8	IJ55 E8
3L04 D9	
3L05 D9	
5J00 A6	

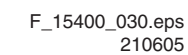
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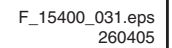
SSB: PN2015: DV I/O Interface



PNX 2015: TUNNEL BUS



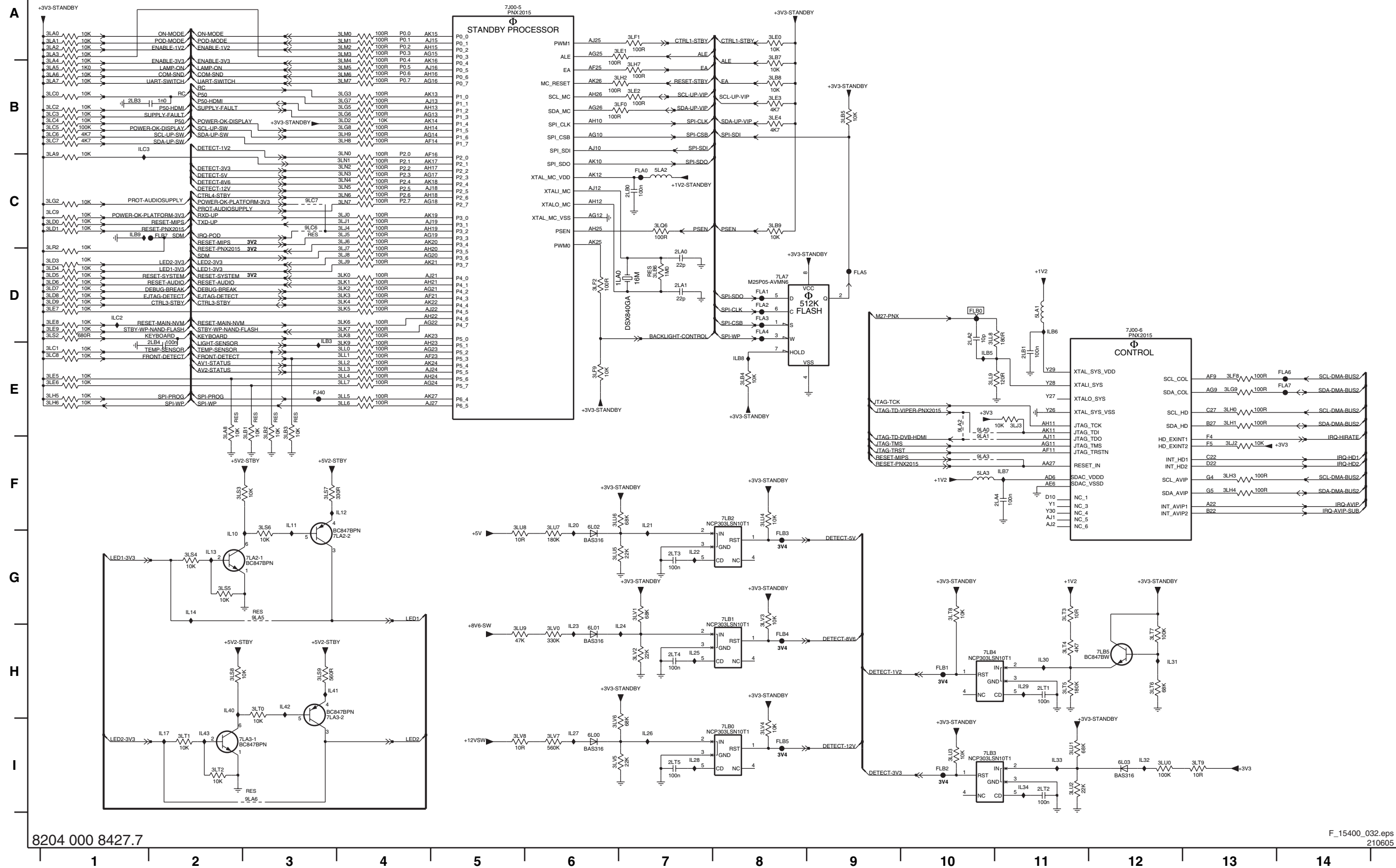
B4D PNX 2015: DDR INTERFACE



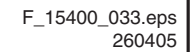
SSB: PN2015: Standby & Control

B4E PN2015: STANDBY + CONTROL

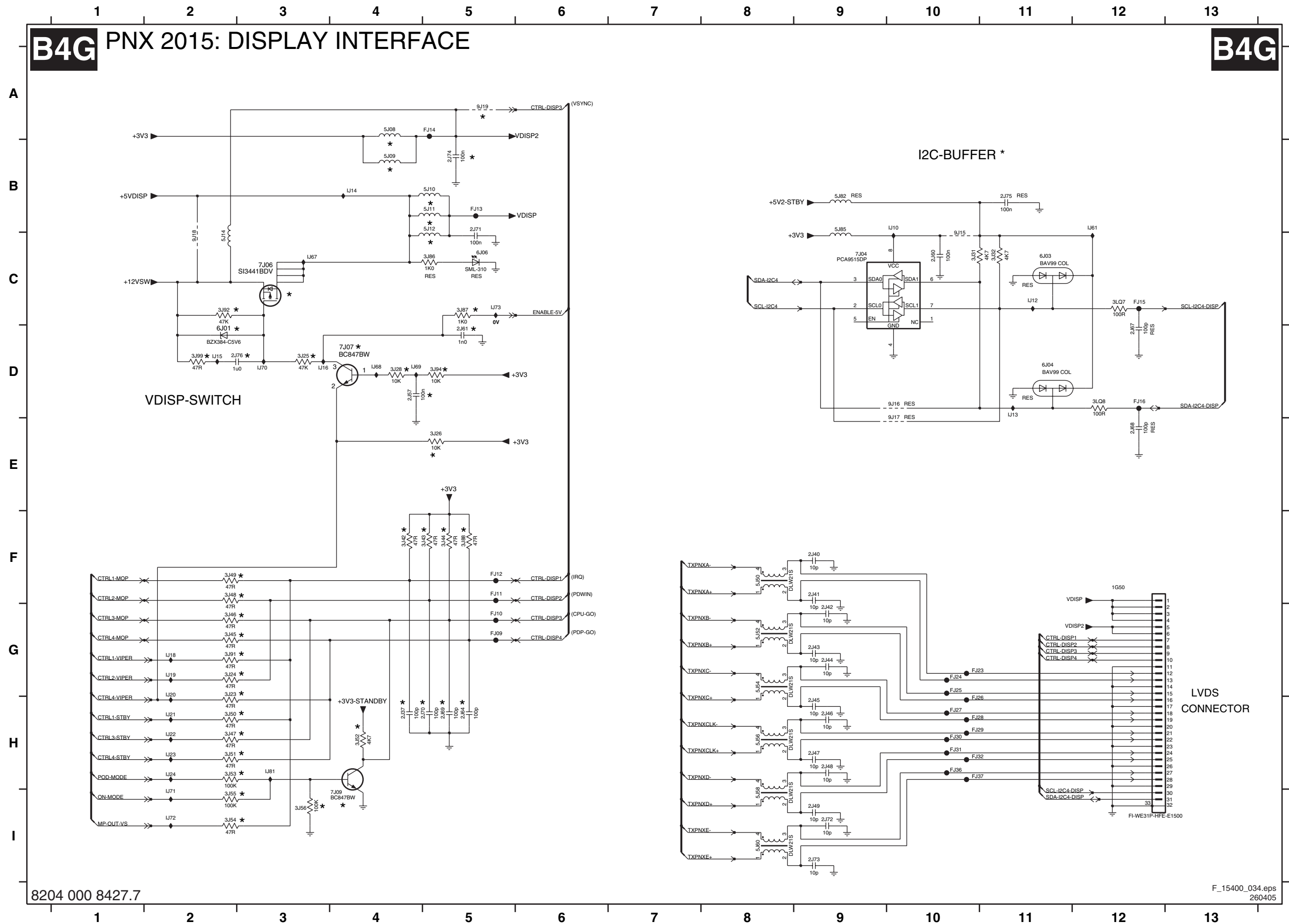
B4E



B4F PNx 2015: SUPPLY



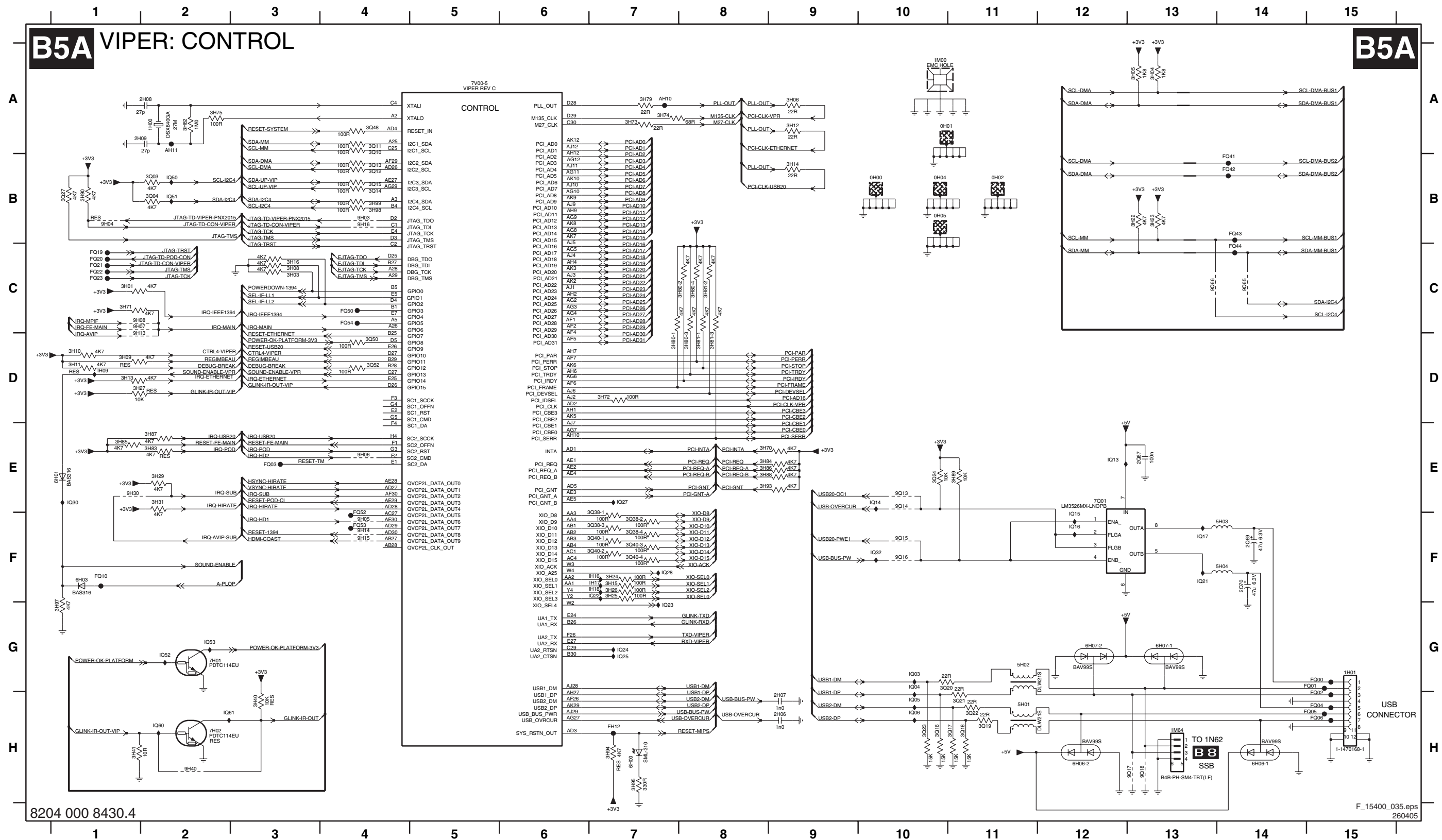
SSB: PNX2015: Display Interface



F250 F12	FJ28 H10
2J37 H4	FJ29 H10
2J40 F9	FJ30 H10
2J41 F9	FJ31 H10
2J42 G9	FJ32 H10
2J43 G9	FJ36 H10
2J44 G9	FJ37 H10
2J45 H9	IJ10 B10
2J46 H9	IJ12 C11
2J47 H9	IJ13 D11
2J48 H9	IJ14 B4
2J49 I9	IJ15 D2
2J57 D4	IJ16 D3
2J60 C10	IJ18 G2
2J61 D5	IJ19 G2
2J64 H5	IJ20 G2
2J67 D12	IJ21 H2
2J68 E12	IJ22 H2
2J69 H5	IJ23 H2
2J70 H5	IJ24 H2
2J71 B5	IJ61 B12
2J72 I9	IJ67 C3
2J73 I9	IJ68 D4
2J74 B5	IJ69 D4
2J75 B11	IJ70 D3
2J76 D3	IJ71 I2
3J23 G2	IJ72 I2
3J24 G2	IJ73 C5
3J25 D3	IJ81 H3
3J26 E5	
3J28 D4	
3J31 C10	
3J32 C11	
3J42 F4	
3J43 F5	
3J44 F5	
3J45 G2	
3J46 G2	
3J47 H2	
3J48 F2	
3J49 F2	
3J50 H2	
3J51 H2	
3J52 H4	
3J53 H2	
3J54 I2	
3J55 I2	
3J56 I3	
3J86 C5	
3J87 C5	
3J88 F5	
3J91 G2	
3J92 C2	
3J94 D5	
3J99 D2	
3LQ7 C12	
3LQ8 D12	
5J08 A4	
5J09 B4	
5J10 B5	
5J11 B5	
5J12 B5	
5J14 C2	
5J50 F8	
5J52 H8	
5J54 G8	
5J56 H8	
5J58 I8	
5J60 I8	
5J82 B9	
5J85 B9	
6J01 D2	
6J03 C11	
6J04 D11	
6J06 C5	
7J04 C9	
7J06 C3	
7J07 D4	
7J09 I4	
9J15 C10	
9J16 D10	
9J17 E10	
9J18 C2	
9J19 A5	
FJ09 G5	
FJ10 G5	
FJ11 F5	
FJ12 F5	
FJ13 B5	
FJ14 A5	
FJ15 C12	
FJ16 D12	
FJ23 G10	
FJ24 G10	
FJ25 G10	
FJ26 H10	
FJ27 H10	

SSB: Viper: Control

0H00 B10	1M00 A10	2Q69 F14	3H08 C3	3H15 F7	3H27 D1	3H72 D7	3H80-3 D8	3H84 E8	3H93 E8	3Q04 B2	3Q16 H10	3Q23 H10	3Q40-1 F7	5H01 H11	6H06-1 H14	7V00-5 A5	9H13 C1	9Q14 E10	AH10 A7	FQ04 H15	FQ22 C1	FQ52 F4	IQ03 G10	IQ16 F12	IQ27 E7	IQ53 G2
0H01 A10	1M64 H13	2Q70 F14	3H09 D1	3H16 C3	3H29 E2	3H73 A7	3H80-4 C8	3H85 E1	3H94 H7	3Q10 A4	3Q17 H11	3Q24 E10	3Q40-2 F7	5H02 G11	6H06-2 H12	9H03 B4	9H14 F4	9Q15 F10	AH11 A2	FQ05 H15	FQ23 C1	FQ53 F4	IQ04 G10	IQ17 F13	IQ28 F7	IQ60 H2
0H02 B11	2H06 H9	3H01 C1	3H10 D1	3H22 B13	3H31 E2	3H74 B1	3H81-1 D8	3H86 E8	3H95 H7	3Q11 A4	3Q18 H11	3Q27 B1	3Q40-3 F7	5H03 F14	6H07-1 G13	9H04 B1	9H15 F4	9Q16 F10	FH12 H7	FQ06 H15	FQ24 C1	FQ54 F4	IQ05 H10	IQ21 F13	IQ30 E1	IQ61 H2
0H04 B10	2H07 H9	3H03 C3	3H11 D1	3H23 B13	3H40 H3	3H75 A2	3H81-2 C8	3H87 E2	3H97 G1	3Q12 B4	3Q19 H11	3Q38-1 F7	3Q40-4 F7	5H04 F14	6H07-2 G12	9H05 F4	9H16 B4	9Q17 H13	FQ00 G15	FQ10 F1	FQ42 B14	IH09 D1	IQ06 H10	IQ22 F7	IQ32 F10	
0H05 B10	2H08 A2	3H04 A13	3H12 A9	3H24 F7	3H41 H1	3H79 A7	3H81-3 D8	3H88 E8	3H98 B4	3Q13 B4	3Q20 G10	3Q38-2 F7	3Q48 A4	6H00 H7	7H01 G2	9H06 E4	9H30 E1	9Q18 H13	FQ01 G15	FQ19 C1	FQ43 B14	IH16 F7	IQ13 E12	IQ23 G7	IQ50 B2	
1H00 A2	2H09 A1	3H05 A13	3H13 D1	3H25 F7	3H70 E8	3H82 A2	3H80-1 D7	3H89 E1	3H99 B4	3Q14 B4	3Q21 H11	3Q38-3 F7	3Q50 D4	6H01 E1	7H02 H2	9H07 C1	9H40 H2	9Q65 C14	FQ02 H15	FQ20 C1	FQ44 C14	IH17 F7	IQ14 E10	IQ24 G7	IQ51 B2	
1H01 G15	2Q67 E13	3H06 A9	3H14 B9	3H26 F7	3H71 C1	3H80-2 C7	3H83 E2	3H90 B1	3Q03 B2	3Q15 B4	3Q22 H11	3Q38-4 F7	3Q52 D4	6H03 F1	7H03 E12	9H08 C1	9Q13 E10	9Q66 C13	FQ03 E3	FQ21 C1	FQ50 C4	IH18 F7	IQ15 F12	IQ25 G7	IQ52 G2	



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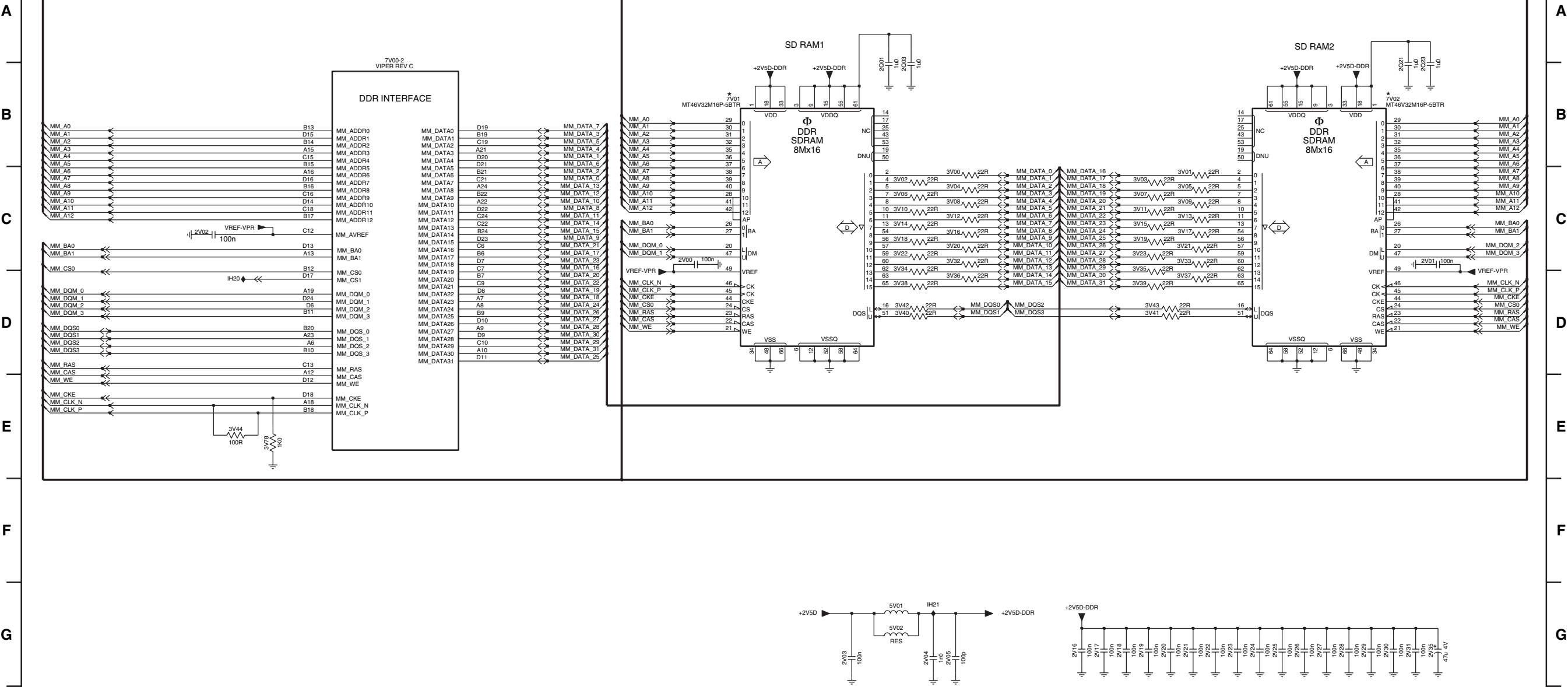
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SSB: Viper: Main Memory

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VIPER: MAIN MEMORY

B5B



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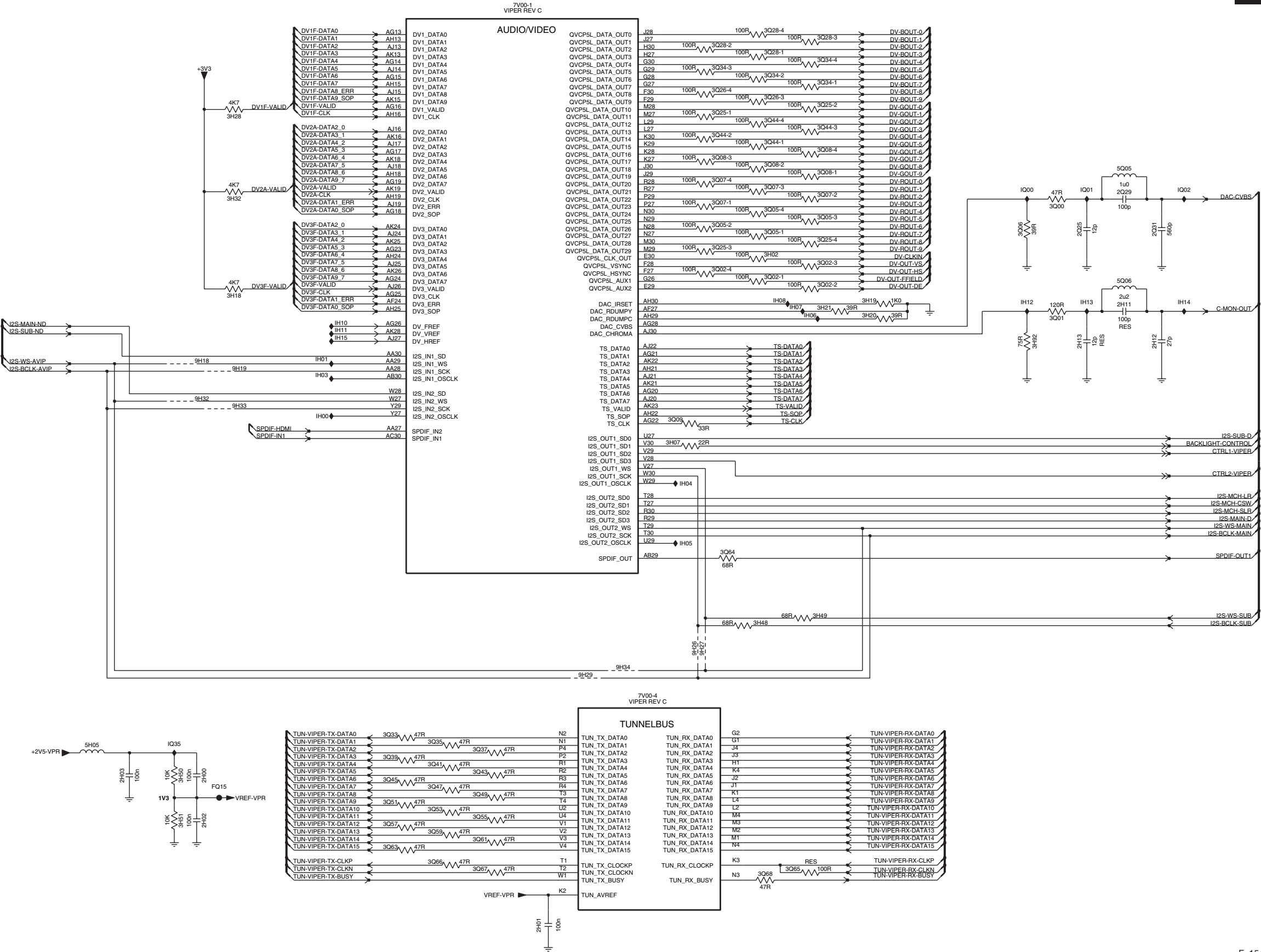
2Q01 B8
2Q03 B9
2Q01 B13
2Q03 B14
2V00 C7
2V01 C14
2V02 C2
2V03 G8
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2V05 G9
2V16 G10
2V17 G11
2V18 G11
2V19 G11
2V20 G11
2V21 G11
2V22 G12
2V23 G12
2V24 G12
2V25 G12
2V26 G12
2V27 G13
2V28 G13
2V29 G13
2V30 G13
2V31 G14
2V35 G14
3V00 C9
3V01 C11
3V02 C9
3V03 C11
3V04 C9
3V05 C11
3V06 C9
3V07 C11
3V08 C9
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3V18 C9
3V19 C11
3V20 C9
3V21 C11
3V22 C9
3V23 C11
3V24 C9
3V25 C11
3V26 C9
3V27 C11
3V28 C9
3V29 C11
3V30 C9
3V31 C11
3V32 C9
3V33 C11
3V34 C9
3V35 C11
3V36 C9
3V37 D11
3V38 D9
3V39 D11
3V40 D9
3V41 D11
3V42 D9
3V43 D11
3V44 E3
3V78 E3
5V01 G9
5V02 G9
7V00-2 A4
7V01 B7
7V02 B13
IH20 D3
IH21 G9

SSB: Viper: A/V & Tunnel Bus

B5C

VIPER: A/V + TUNNEL BUS

B5C

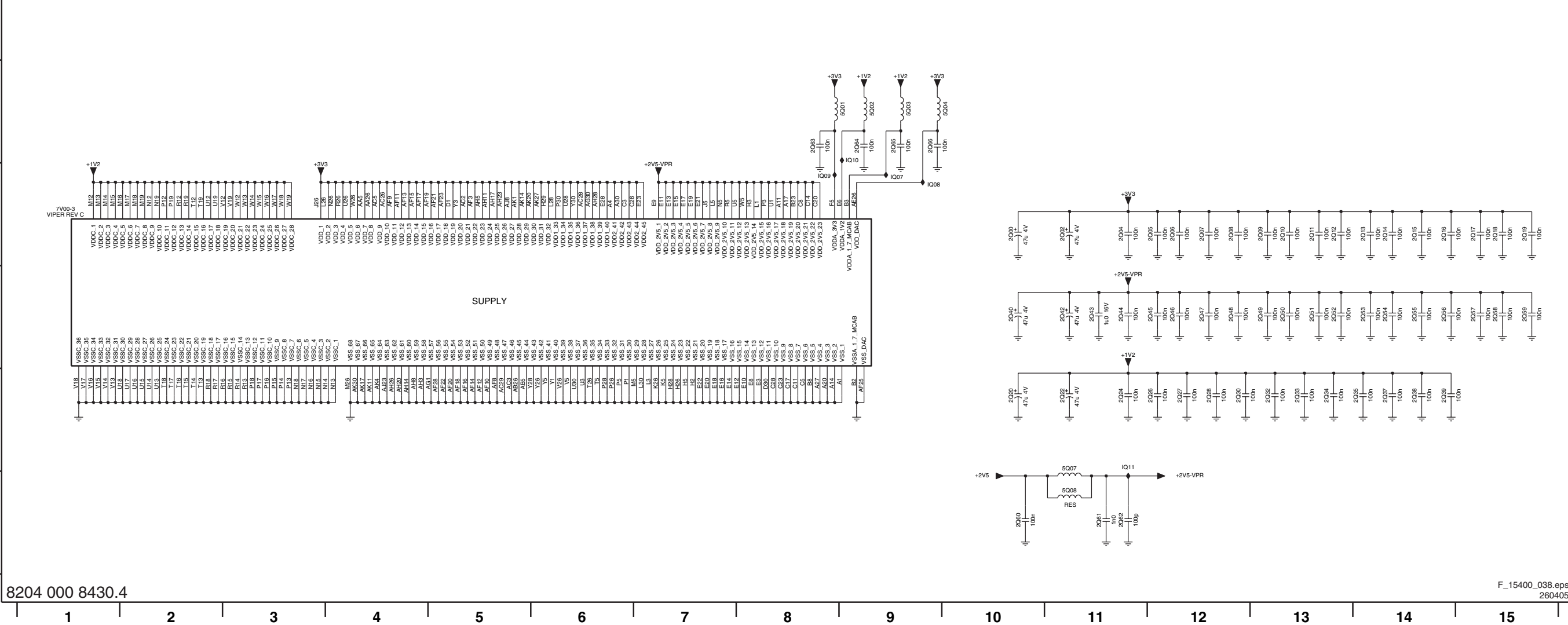


SSB: Viper: Supply

2Q00 C10	2Q05 C12	2Q08 C12	2Q11 C13	2Q14 C14	2Q17 C15	2Q20 E10	2Q26 E12	2Q30 E12	2Q34 E13	2Q38 E14	2Q42 D11	2Q45 D12	2Q46 D12	2Q48 D12	2Q51 D13	2Q54 D14	2Q57 D15	2Q60 F10	2Q63 B8	2Q66 B9	5Q03 B9	5Q08 F11	IQ08 C9	IQ11 E11
2Q02 C11	2Q06 C12	2Q09 C13	2Q12 C13	2Q15 C14	2Q18 C15	2Q22 E11	2Q27 E12	2Q32 E13	2Q35 E14	2Q39 E14	2Q43 D11	2Q46 D12	2Q49 D13	2Q50 D13	2Q52 D13	2Q55 D14	2Q58 D15	2Q61 F11	2Q64 B9	5Q01 B9	5Q04 B10	7V00-3 C1	IQ09 C8	
2Q04 C11	2Q07 C12	2Q10 C13	2Q13 C14	2Q16 C14	2Q19 C15	2Q24 E11	2Q28 E12	2Q33 E13	2Q37 E14	2Q40 D10	2Q44 D11	2Q47 D12	2Q50 D13		2Q53 D14	2Q56 D14	2Q59 D15	2Q62 F11	2Q65 B9	5Q02 B9	5Q07 E11	IQ07 C9	IQ10 B9	

B5D VIPER: SUPPLY

B5D



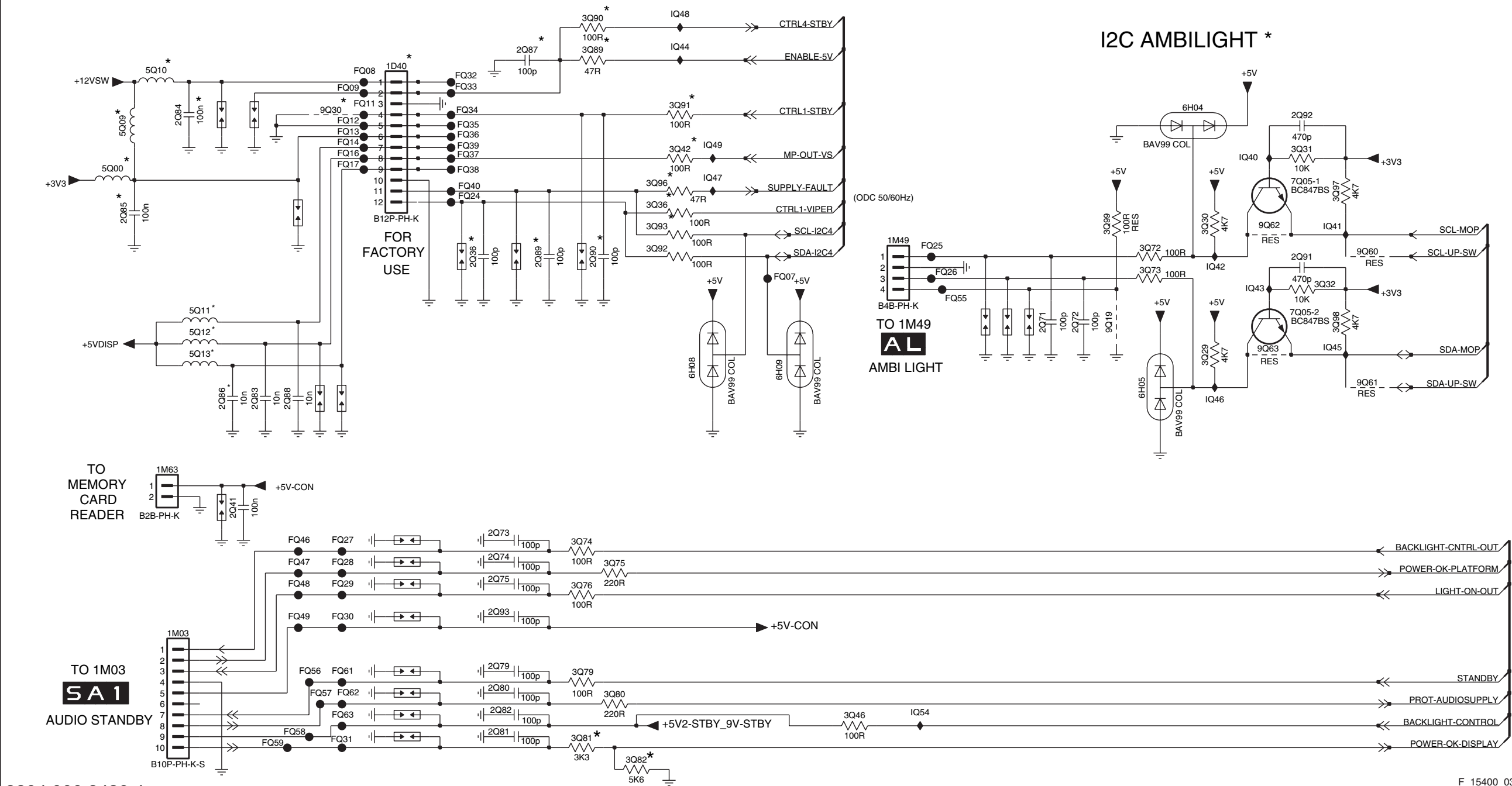
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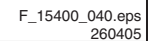
SSB: Viper: Display Diversity & Ambilight

1D40 A3	2Q71 C7	2Q80 E4	2Q86 C2	2Q92 A9	3Q36 B5	3Q75 D4	3Q89 A4	3Q97 B9	5Q11 C2	6H09 C6	9Q61 C9	FQ11 A3	FQ24 B4	FQ30 E3	FQ36 A3	FQ47 D2	FQ58 E2	IQ41 B9	IQ47 B5
1M03 E2	2Q72 C7	2Q81 E4	2Q87 A4	2Q93 E4	3Q42 B5	3Q76 D4	3Q90 A4	3Q98 C9	5Q12 C2	7Q05-1 B9	9Q62 B9	FQ12 A3	FQ25 B7	FQ31 E3	FQ37 B3	FQ48 D2	FQ59 E2	IQ42 B8	IQ48 A5
1M49 B6	2Q73 D4	2Q82 E4	2Q88 C2	3Q29 C8	3Q46 E6	3Q79 E4	3Q91 A5	3Q99 B8	5Q13 C2	7Q05-2 C9	9Q63 C9	FQ13 A3	FQ26 B7	FQ32 A3	FQ38 B3	FQ49 E2	FQ61 E3	IQ43 B9	IQ49 B5
1M63 D2	2Q74 D4	2Q83 C2	2Q89 B4	3Q30 B8	3Q72 B8	3Q80 E4	3Q92 B5	5Q00 B1	6H04 A8	9Q19 C8	FQ07 B6	FQ14 B3	FQ27 D3	FQ33 A3	FQ39 B3	FQ55 C7	FQ62 E3	IQ44 A5	IQ54 E6
2Q36 B4	2Q75 D4	2Q84 A2	2Q90 B4	3Q31 B9	3Q73 B8	3Q81 E4	3Q93 B5	5Q09 A1	6H05 C8	9Q30 A3	FQ08 A3	FQ16 B3	FQ28 D3	FQ34 A3	FQ40 B4	FQ56 E2	FQ63 E3	IQ45 C9	
2Q41 D2	2Q79 E4	2Q85 B1	2Q91 B9	3Q32 B9	3Q74 D4	3Q82 E5	3Q96 B5	5Q10 A1	6H08 C5	9Q60 B9	FQ09 A3	FQ17 B3	FQ29 D3	FQ35 A3	FQ46 D2	FQ57 E3	IQ40 B9	IQ46 C8	

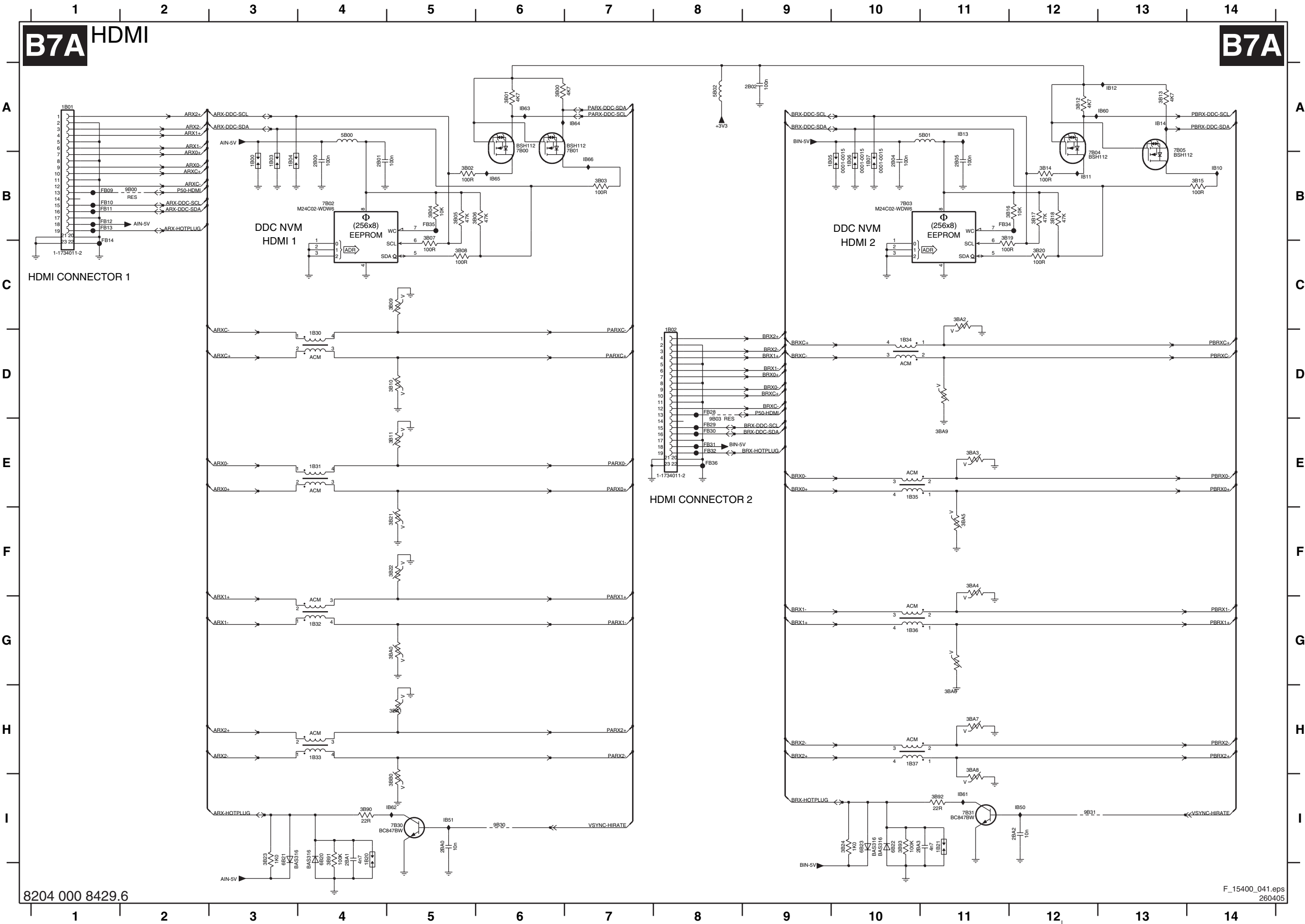
B5E VIPER: DISPLAY DIVERSITY + AMBILIGHT



B6 DISPLAY INTERFACE: MOP

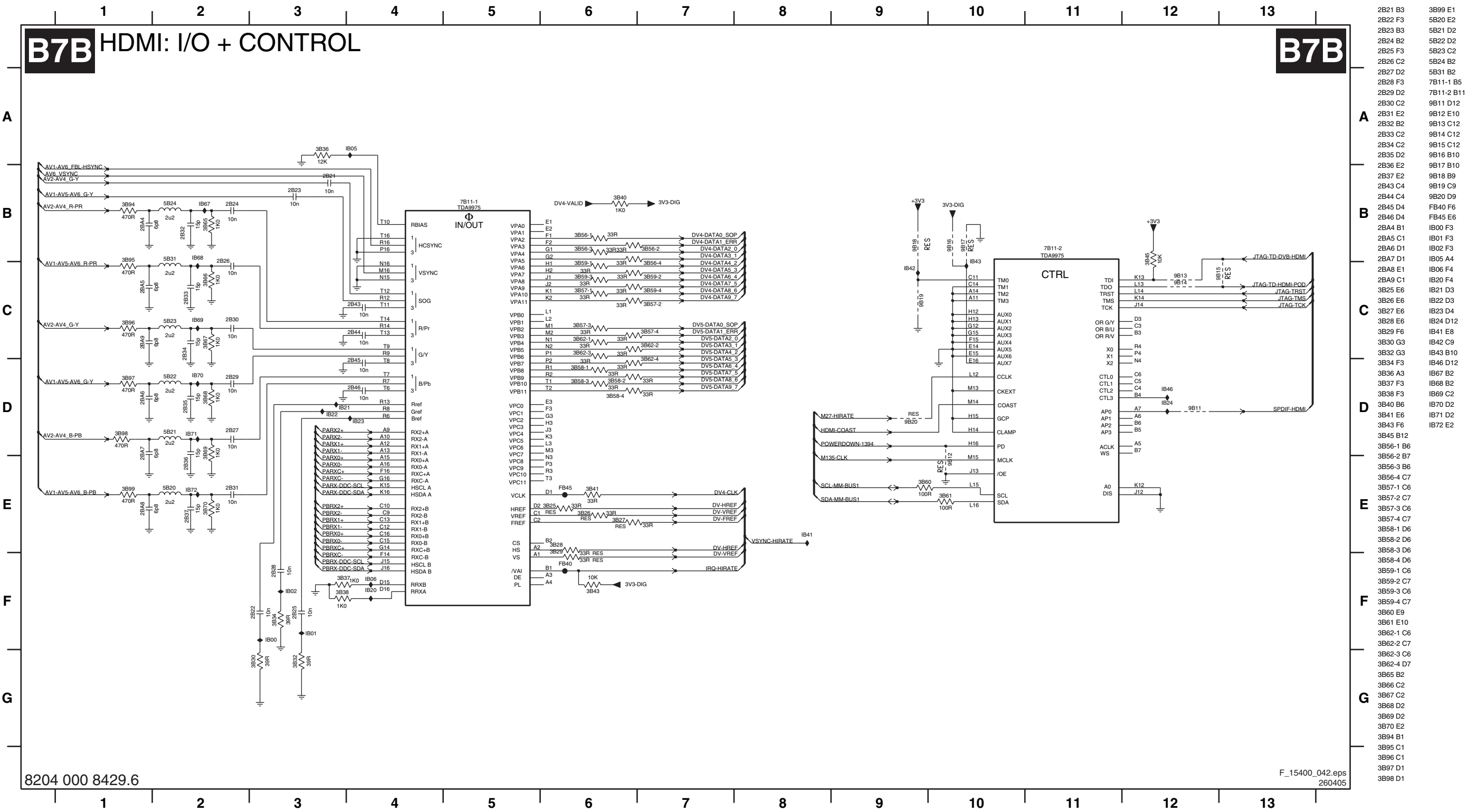


SSB: HDMI

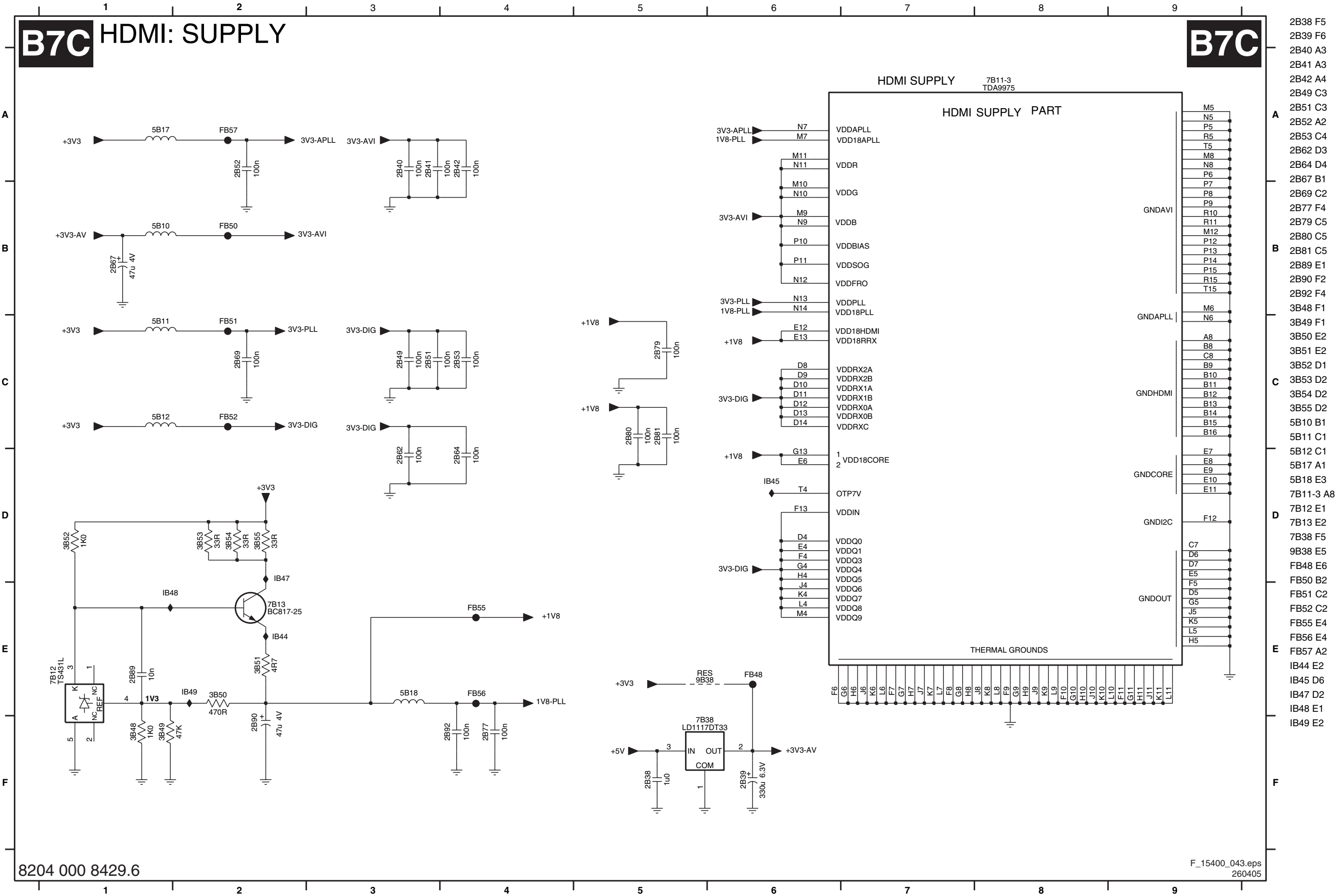


- 1B00 B3
- 1B01 A1
- 1B02 D8
- 1B03 B3
- 1B04 B3
- 1B05 B10
- 1B06 B10
- 1B07 B10
- 1B08 I4
- 1B09 I11
- 1B10 D4
- 1B11 E4
- 1B12 G4
- 1B13 H4
- 1B14 D10
- 1B15 E10
- 1B16 G10
- 1B17 H10
- 1B18 B4
- 1B19 B4
- 1B20 A9
- 1B21 B10
- 1B22 B11
- 1B23 I4
- 1B24 I10
- 1B25 I10
- 1B26 A6
- 1B27 A6
- 1B28 B5
- 1B29 B7
- 1B30 B5
- 1B31 B6
- 1B32 B5
- 1B33 B5
- 1B34 B5
- 1B35 B5
- 1B36 B5
- 1B37 B5
- 1B38 B5
- 1B39 B5
- 1B40 B5
- 1B41 B5
- 1B42 B5
- 1B43 B5
- 1B44 B5
- 1B45 B5
- 1B46 B5
- 1B47 B5
- 1B48 B5
- 1B49 B5
- 1B50 B5
- 1B51 B5
- 1B52 B5
- 1B53 B5
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- 1B67 B5
- 1B68 B5
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- 1B73 B5
- 1B74 B5
- 1B75 B5
- 1B76 B5
- 1B77 B5
- 1B78 B5
- 1B79 B5
- 1B80 B5
- 1B81 B5
- 1B82 B5
- 1B83 B5
- 1B84 B5
- 1B85 B5
- 1B86 B5
- 1B87 B5
- 1B88 B5
- 1B89 B5
- 1B90 B5
- 1B91 B5
- 1B92 B5
- 1B93 B5
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- 1B96 B5
- 1B97 B5
- 1B98 B5
- 1B99 B5
- 1B100 B5

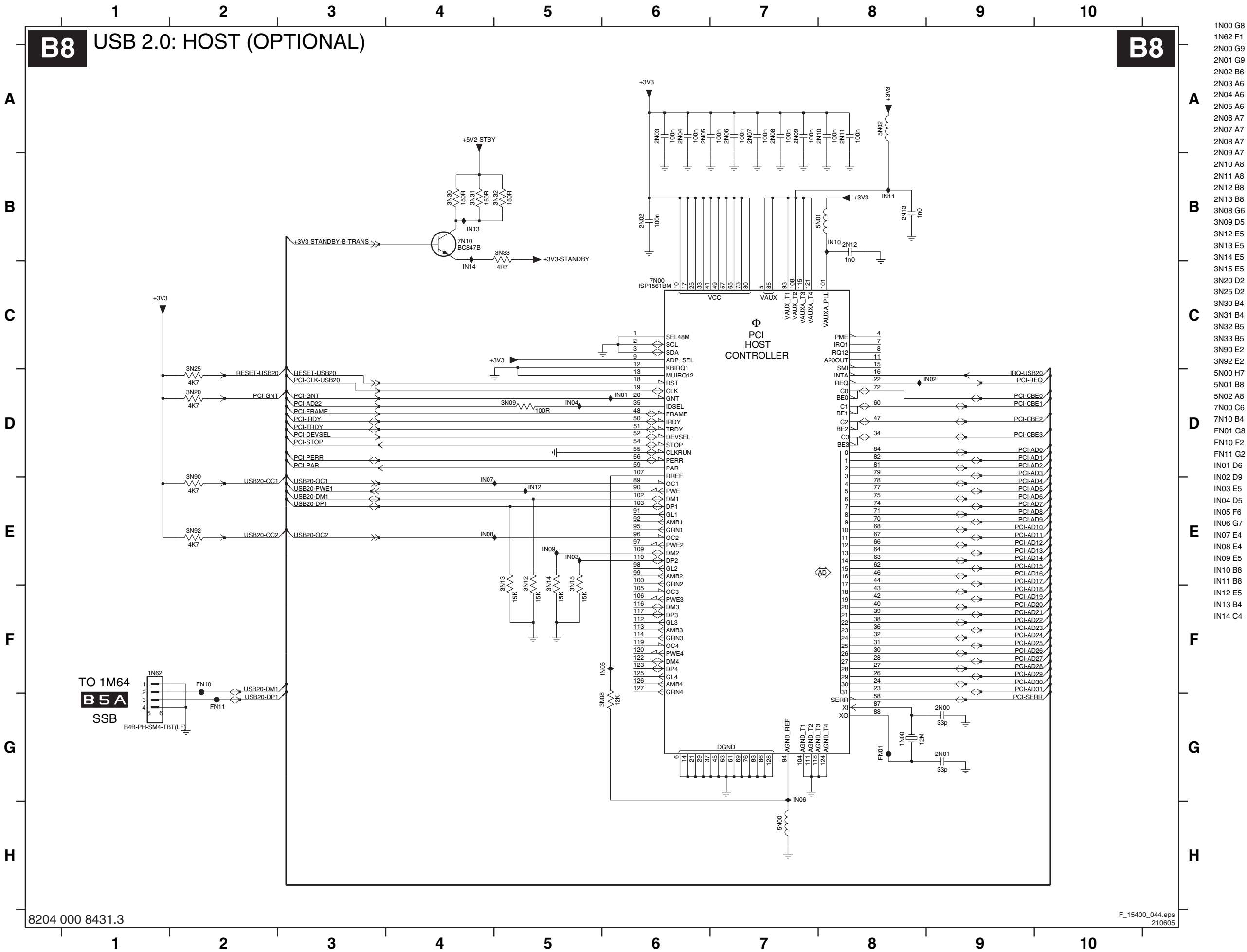
SSB: HDMI: I/O & Control



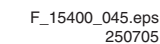
SSB: HDMI: Supply



SSB: USB2.0: Host (Optional)

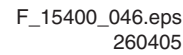


1000 C8	2002 H4	2006 D12	2012 G10	2016 C8	2020 G11	2024 G11	2028 G10	3003 C7	3007 D1	3011 D8	3021 A8	3025 C9	5000 G9	7000-1 B3	FO01 A10	FO05 C10	FO12 H9	IO04 G10	IO08 A12	IO13 F7
1010 A10	2003 H3	2007 D11	2013 B9	2017 H9	2021 G11	2025 G10	3000 C8	3004 E8	3008 E1	3012 D9	3022 A9	3026 C9	5001 H9	7000-2 H7	FO02 B10	FO06 F9	IO01 E7	IO05 A9	IO10 C8	IO14 F8
2000 D8	2004 A11	2010 E3	2014 B9	2018 H10	2022 G11	2026 G10	3001 C7	3005 F8	3009 A11	3013 D9	3023 A9	3027 C9	6000 F8	9016 C9	FO03 C10	FO07 F9	IO02 C7	IO06 C9	IO11 F7	
2001 D8	2005 A12	2011 G9	2015 B10	2019 G12	2023 G11	2027 G10	3002 D3	3006 F8	3010 C11	3014 D9	3024 A9	3028 C9	6001 F8	AO01 C8	FO04 C10	FO08 E3	IO03 H3	IO07 D12	IO12 F7	



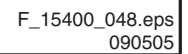
M15 B6 1002

FO11 C4



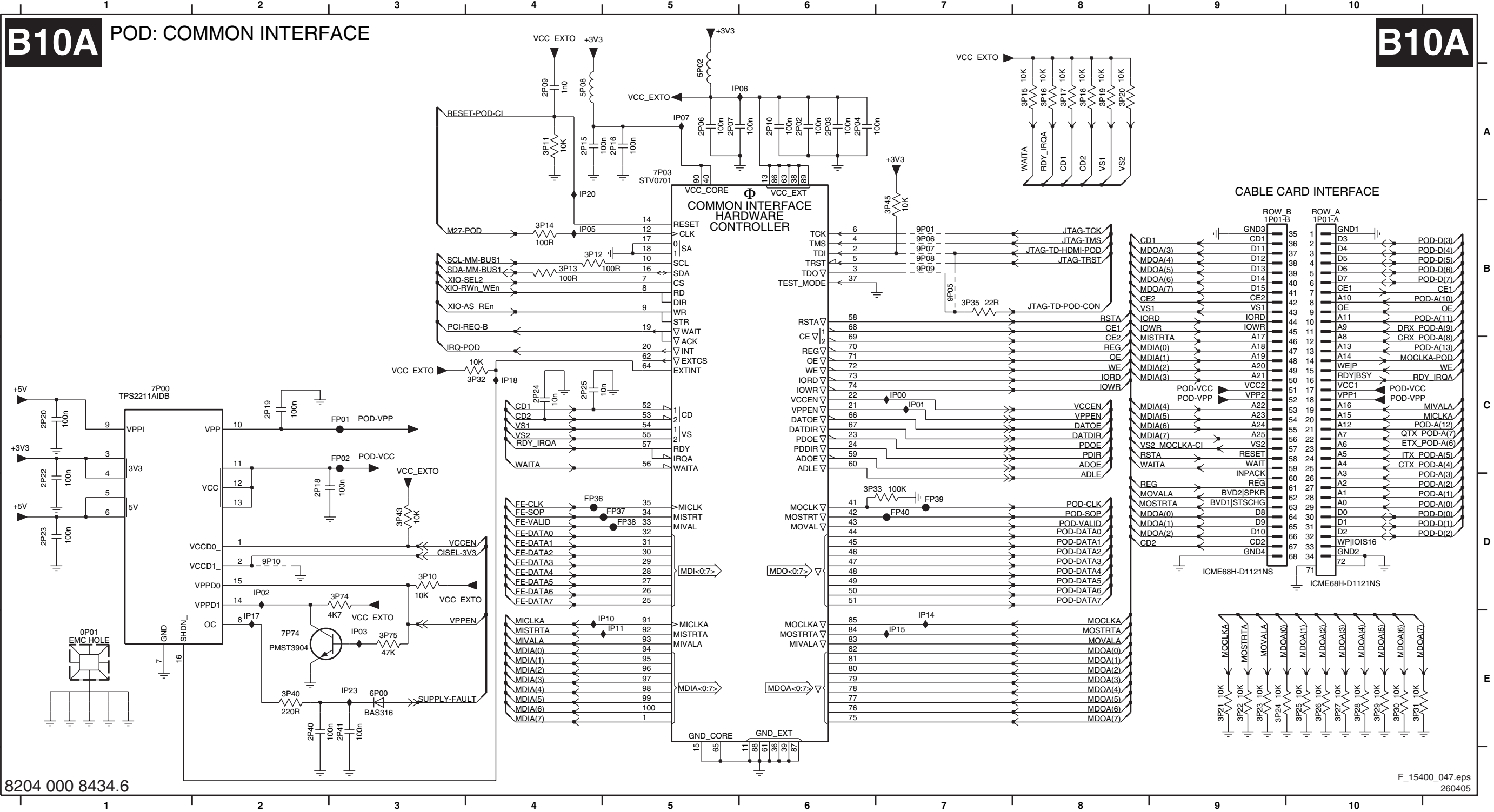
1 |

2P50 B1
2P51 E1
3P50 F3
3P51 F3
3P52 F3
3P53 F4
7P10-1 D2
7P10-2 E2
7P13 C2
9P30 A2
9P31 A2
9P32 A2
9P33 B2
9P34 B2
9P35 B2
9P36 B3
9P37 B3
9P38 B3

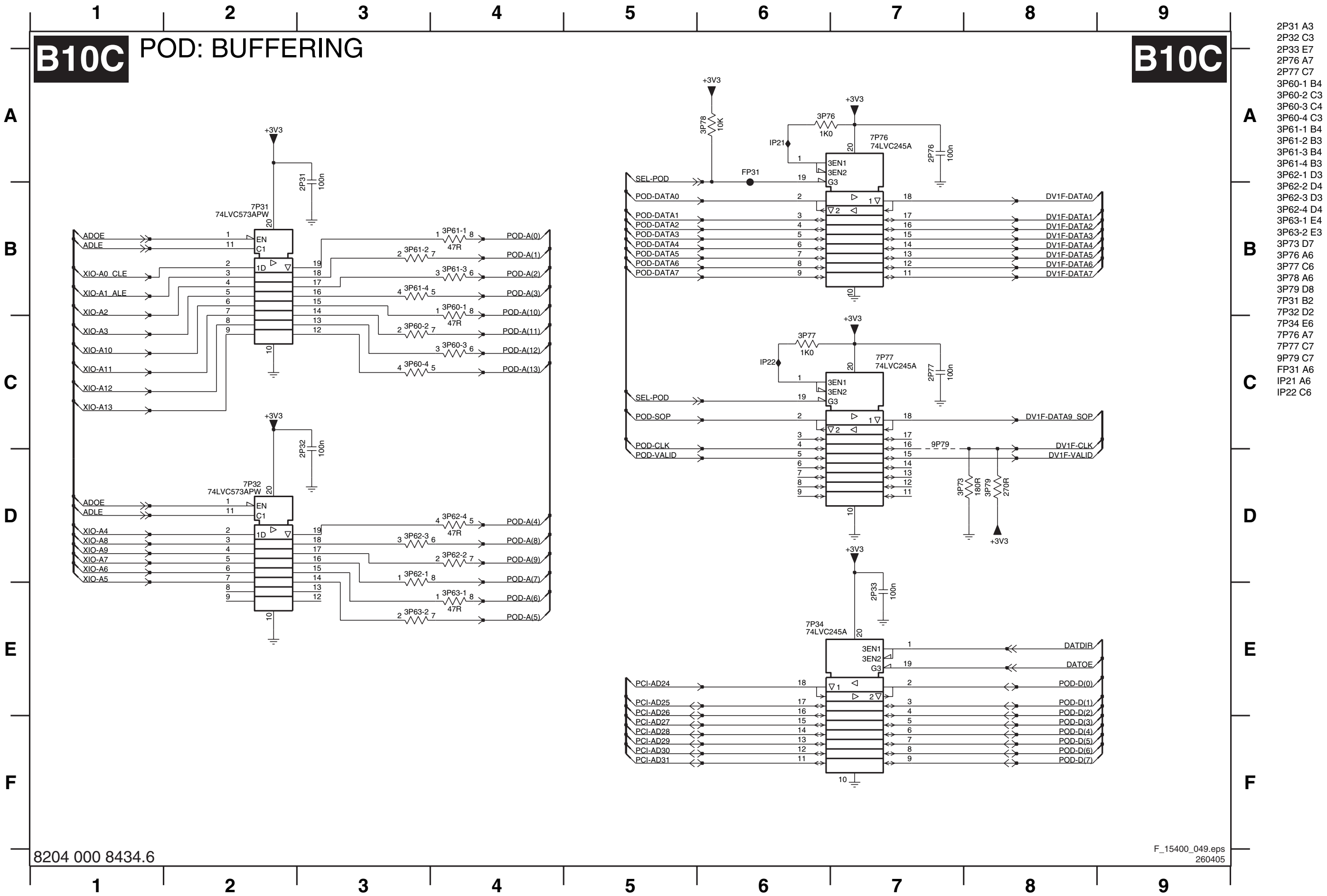


SSB: POD: Common Interface

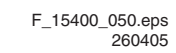
1P01-A B10	2P06 A5	2P16 A5	2P23 D1	3P10 D3	3P15 A8	3P20 A8	3P25 E10	3P30 E10	3P40 E2	5P02 A5	7P74 E2	9P08 B7	FP36 D4	IP00 C7	IP06 A6	IP15 E7
1P01-B B9	2P07 A5	2P18 D2	2P24 C4	3P11 A4	3P16 A8	3P21 E9	3P26 E10	3P31 E10	3P43 D3	5P08 A4	9P01 B7	9P09 B7	FP37 D5	IP01 C7	IP07 A5	IP17 E2
2P02 A6	2P09 A4	2P19 C2	2P25 C4	3P12 B4	3P17 A8	3P22 E9	3P27 E10	3P32 C4	3P45 B7	6P00 E3	9P05 B7	9P10 D2	FP38 D5	IP02 D2	IP10 E5	IP18 C4
2P03 A6	2P10 A6	2P20 C1	2P40 E2	3P13 B4	3P18 A8	3P23 E9	3P28 E10	3P33 D6	3P74 D3	7P00 C1	9P06 B7	FP01 C3	FP39 D7	IP03 E3	IP11 E5	IP20 A4
2P04 A6	2P15 A4	2P22 D1	2P41 E3	3P14 B4	3P19 A8	3P24 E9	3P29 E10	3P35 B7	3P75 E3	7P03 A5	9P07 B7	FP02 C3	FP40 D7	IP05 B4	IP14 E7	IP23 E3



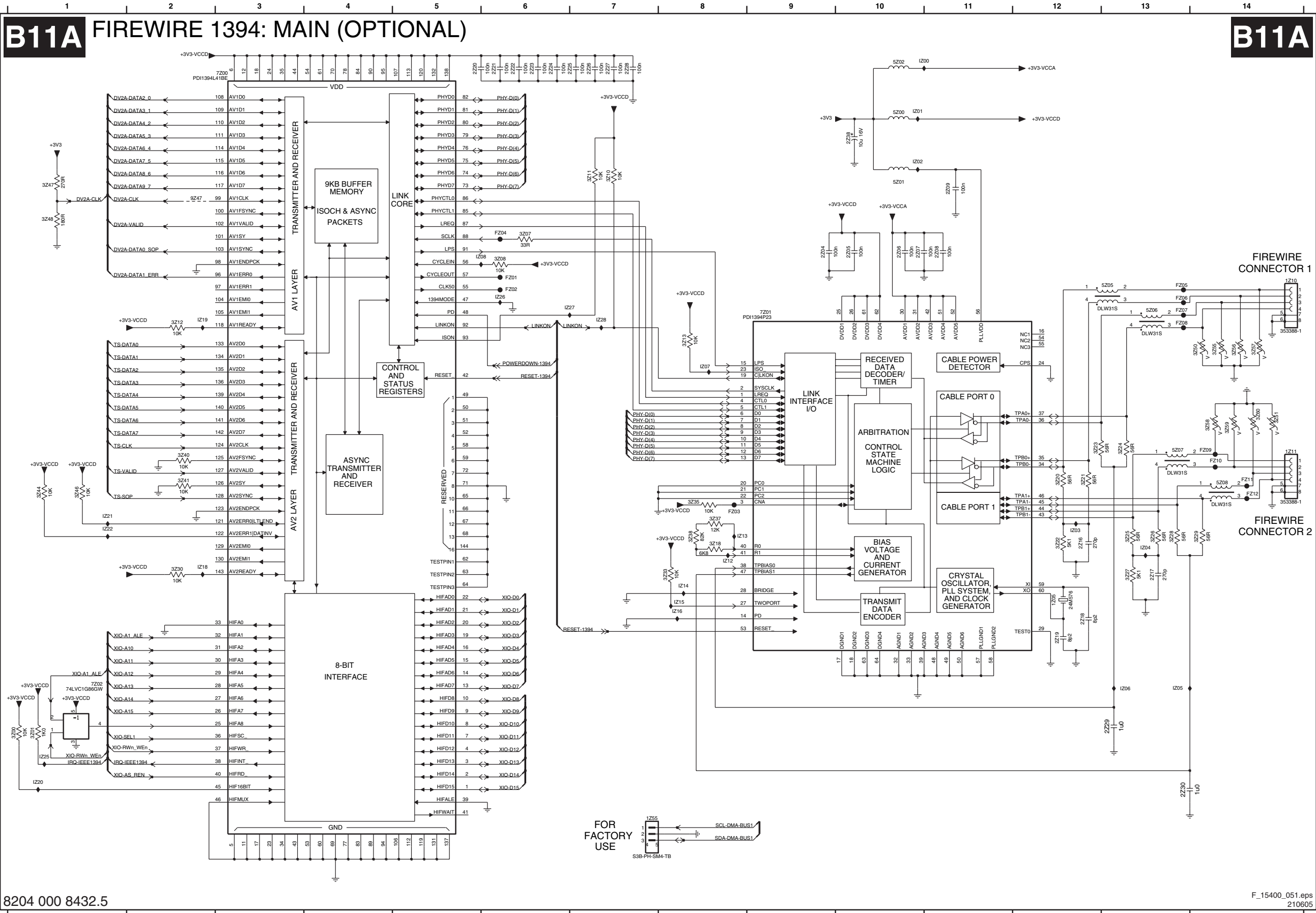
SSB: POD: Buffering



B10D POD: TS BUFFERING

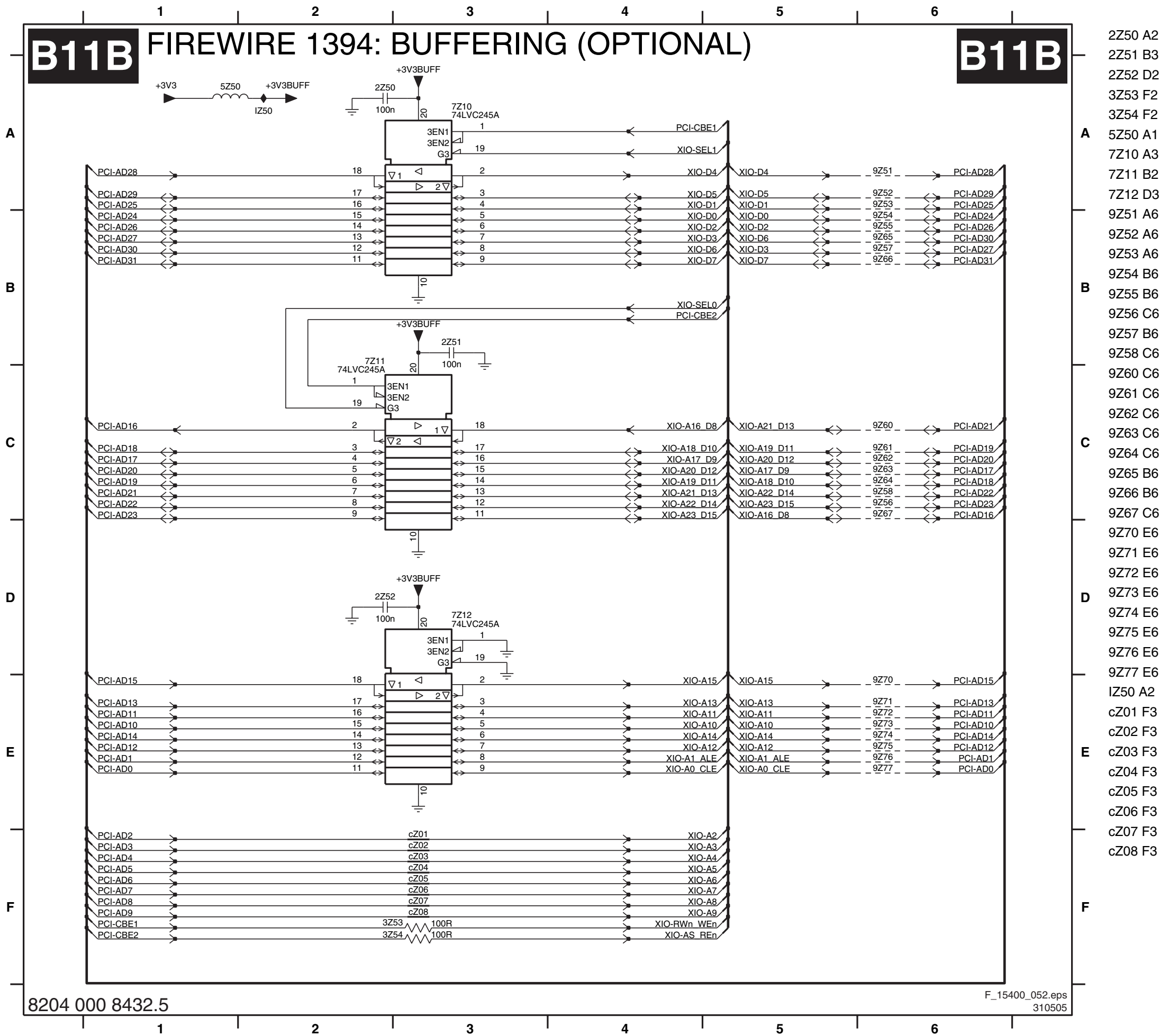


SSB: Firewire 1394: Main (Optional)



- 1205 F12
- 1210 C14
- 1211 E14
- 1255 I7
- 2204 B9
- 2205 B10
- 2206 B10
- 2207 B10
- 2208 B11
- 2209 B11
- 2216 F12
- 2217 F13
- 2218 G12
- 2219 G12
- 2220 A5
- 2221 A6
- 2222 A6
- 2223 A6
- 2224 A6
- 2225 A7
- 2226 A7
- 2227 A7
- 2228 A7
- 2229 H13
- 2230 H13
- 2238 A10
- 2200 H1
- 3201 H1
- 3207 B6
- 3208 C6
- 3210 B7
- 3211 B7
- 3212 C2
- 3213 C8
- 3218 F8
- 3220 E12
- 3221 E12
- 3222 F12
- 3223 E12
- 3224 E13
- 3225 F13
- 3226 F13
- 3227 F13
- 3228 F13
- 3229 F14
- 3230 F2
- 3233 F8
- 3235 E8
- 3237 E8
- 3238 F8
- 3240 E2
- 3241 E2
- 3244 E1
- 3246 E1
- 3247 B1
- 3248 B1
- 3250 D14
- 3251 D14
- 3255 D14
- 3256 D14
- 3257 D14
- 3258 D14
- 3259 D14
- 3260 D14
- 5200 A10
- 5201 B10
- 5202 A10
- 5205 C13
- 5206 C13
- 5207 E13
- 5208 E14
- 7200 A3
- 7201 C9
- 7202 G1
- 9247 B2
- F201 C6
- F202 C6
- F203 E8
- F204 B6
- F205 C13
- F206 C13
- F207 C13
- F208 C13
- F209 E14
- F210 E14
- F211 E14
- F212 E14
- I200 A10
- I201 A10
- I202 A10
- I203 F12
- I204 F13
- I205 G1
- I206 G1
- I207 D8
- I208 B5
- I212 F8
- I213 F8
- I214 F8
- I215 F8
- I216 F8
- I219 C2
- I220 H1
- I221 E1
- I222 F1
- I225 H1
- I226 C6
- I227 C6
- I228 C7

SSB: Firewire 1394: Buffering (Optional)



B12 MISCELLANEOUS



1TG1 E4	IM13 C5
2M90 B2	IM14 C2
2M91 C2	IM15 C2
2M92 D3	IM16 C4
2M93 C4	IM17 D2
2M94 D5	
3M00 E1	
3M01 E1	
3M02 E2	
3M03 E1	
3M04 E2	
3M05 F2	
3M09 A4	
3M14 C3	
3M70 A1	
3M71 B1	
3M72 A3	
3M73 B1	
3M74 B3	
3M75 B3	
3M76 D2	
3M77 D2	
3M78 D2	
3M79 C4	
3M80 C5	
3M81 C5	
3M82 B3	
3M85 E4	
3M86 E4	
6M10 E3	
6M11 F3	
7M01 A4	
7M03 A3	
7M04 C3	
7M05 D1	
7M06 C4	
7M07 C5	
7M10 E1	
7M11 E1	
7M12 E2	
9M00 F1	
9M01 E5	
9M02 E5	
9M04 E4	
9M05 E5	
9M06 A3	
FM07 F1	
FM10 A3	
FM70 A1	
FM71 C5	
FM72 D3	
IM00 D2	
IM01 E2	
IM02 E3	
IM03 F3	
IM04 E1	
IM05 E1	
IM06 E1	
IM08 F2	
IM11 A3	
IM12 A2	

SRP Overview SSB

+12VS	B1a	+5VbM	B3c	AV1-STATUS	B3f	DATOE	B10a	DV3F-DATA8_6	B4b	DV-ROUT-3	B6	I2S-MCH-CSW	B5c	MDOA(4)	B10a	MP-G1	B6	PBRX2+	B7a
+12VS	B1b	+5V-CON	B1b	AV1-STATUS	B3g	DATOE	B10c	DV3F-DATA8_6	B5c	DV-ROUT-4	B5c	I2S-MCH-LR	B4a	MDOA(5)	B10a	MP-G2	B6	PBRX2+	B7b
+12VS	B4a	+5V-CON	B5e	AV1-STATUS	B4e	DEBUG-BREAK	B4e	DV3F-DATA9_7	B4b	DV-ROUT-5	B5c	I2S-MCH-SLR	B4a	MDOA(6)	B10a	MP-G3	B6	PBRXC-	B7a
+12VSW	B1a	+5VDISP	B4g	AV1-STATUS-AV7-C	B3f	DEBUG-BREAK	B5a	DV3F-DATA9_7	B5c	DV-ROUT-6	B5c	I2S-SUB-D	B4a	MDOA(7)	B10a	MP-G4	B6	PBRXC-	B7b
+12VSW	B1b	+5VDISP	B5e	AV2_C	B3f	DETECT-12V	B4e	DV3F-VALID	B4b	DV-ROUT-7	B5c	I2S-SUB-ND	B4a	MICLKA	B10a	MP-G5	B6	PBRXC+	B7a
+12VSW	B2a	+5VMPIF-MAIN	B3a	AV2_C	B3f	DETECT-1V2	B4e	DV3F-VALID	B5c	DV-ROUT-8	B5c	I2S-SUB-ND	B4a	MISTRTA	B10a	MP-G6	B6	PBRXC+	B7b
+12VSW	B3e	+5VMPIF-MAIN	B3b	AV2_FBL	B3f	DETECT-3V3	B4e	DV4-CLK	B4b	DV-ROUT-9	B6	I2S-SUB-ND	B5c	MIVALA	B10a	MP-G7	B6	PBRX-DDC-SCL	B7a
+12VSW	B4e	+5VMPIF-MAIN	B3c	AV2_FBL	B4a	DETECT-5V	B4e	DV4-CLK	B7b	DV-ROUT-10	B5c	I2S-SUB-ND	B4a	MM_A0	B5b	MP-G8	B6	PBRX-DDC-SCL	B7b
+12VSW	B4g	+5V-OOB	B2b	AV2_Y-CVBS	B3a	DETECT-8V6	B4e	DV4-DATA0_SOP	B4b	DV-ROUT-11	B6	I2S-SUB-ND	B5c	MM_A1	B5b	MP-G9	B6	PBRX-DDC-SDA	B7a
+12VSW	B5e	+5VTUN	B2b	AV2_Y-CVBS	B3f	DIN	B6	DV4-DATA0_SOP	B7b	DV-ROUT-12	B5c	I2S-W5-AVIP	B4a	MM_A10	B5b	MP-GOUT-0	B4b	PBRX-DDC-SDA	B7b
+1V2	B1a	+8V6	B1b	AV2-AV4_B-PB	B3a	DRX_POD-A(9)	B10a	DV4-DATA1_ERR	B4b	DV-ROUT-13	B6	I2S-W5-AVIP	B5c	MM_A11	B5b	MP-GOUT-0	B6	PCI-AD0	B11b
+1V2	B2a	+8V6-CONN	B3f	AV2-AV4_B-PB	B3f	DRX_POD-A(9)	B10b	DV4-DATA1_ERR	B7b	DV-ROUT-14	B5c	I2S-W5-MAIN	B4a	MM_A12	B5b	MP-GOUT-1	B4b	PCI-AD0	B5a
+1V2	B4e	+8V6-SW	B1b	AV2-AV4_G-Y	B7b	DRX-POD	B10b	DV4-DATA2_0	B4b	DV-ROUT-15	B6	I2S-W5-MAIN	B5c	MM_A2	B5b	MP-GOUT-1	B6	PCI-AD0	B8
+1V2	B5d	+8V6-SW	B2b	AV2-AV4_G-Y	B3a	DRX-POD	B2a	DV4-DATA2_0	B7b	DV-VREF	B4b	I2S-W5-SUB	B4a	MM_A3	B5b	MP-GOUT-2	B4b	PCI-AD0	B9a
+1V2_ATSC	B2a	+8V6-SW	B3b	AV2-AV4_G-Y	B3f	DSNDL1	B3d	DV4-DATA3_1	B4b	DV-VREF	B7b	I2S-W5-SUB	B5c	MM_A4	B5b	MP-GOUT-2	B6	PCI-AD1	B11b
+1V2M	B6	+8V6-SW	B3e	AV2-AV4_G-Y	B7b	DSNDL1	B4a	DV4-DATA3_1	B7b	EA	B4e	IF-TER2	B2b	MM_A5	B5b	MP-GOUT-3	B4b	PCI-AD1	B5a
+1V2-MAIN	B2a	+8V6-SW	B3f	AV2-AV4_R-PR	B3a	DSNDL2	B3d	DV4-DATA4_2	B4b	EJTAG-DETECT	B1c	IF-TER2	B3c	MM_A6	B5b	MP-GOUT-3	B6	PCI-AD1	B8
+1V2-STANDBY	B12	+8V6-SW	B3g	AV2-AV4_R-PR	B3f	DSNDL2	B4a	DV4-DATA4_2	B7b	EJTAG-DETECT	B4e	INIT	B6	MM_A7	B5b	MP-GOUT-4	B4b	PCI-AD1	B9a
+1V2-STANDBY	B4e	+8V6-SW	B4e	AV2-AV4_R-PR	B7b	DSNDR1	B3d	DV4-DATA5_3	B4b	EJTAG-TCK	B1c	IORD	B10a	MM_A8	B5b	MP-GOUT-4	B6	PCI-AD10	B11b
+1V2-STANDBY	B4f	+8V6-SW	B6	AV2-STATUS	B3f	DSNDR1	B4a	DV4-DATA5_3	B7b	EJTAG-TCK	B5a	IOWR	B10a	MM_A9	B5b	MP-GOUT-5	B4b	PCI-AD10	B5a
+1V8	B7c	+8VaM	B3c	AV2-STATUS	B4e	DSNDR2	B3d	DV4-DATA6_4	B4b	EJTAG-TDI	B1c	IRQ-AVIP	B4e	MM_BA0	B5b	MP-GOUT-5	B6	PCI-AD10	B8
+2V5	B1a	+8V-AUD	B3e	AV6_VSYNC	B3f	DSNDR2	B4a	DV4-DATA6_4	B7b	EJTAG-TDI	B5a	IRQ-AVIP	B5a	MM_BA1	B5b	MP-GOUT-6	B4b	PCI-AD10	B9a
+2V5	B2a	+8VMPIF-MAIN	B3b	AV6_VSYNC	B3g	DV1F-CLK	B10c	DV4-DATA7_5	B4b	EJTAG-TDO	B1c	IRQ-AVIP-SUB	B4e	MM_CAS	B5b	MP-GOUT-6	B6	PCI-AD11	B11b
+2V5	B4d	+8VMPIF-MAIN	B3c	AV6_VSYNC	B4a	DV1F-CLK	B4b	DV4-DATA7_5	B7b	EJTAG-TDO	B5a	IRQ-AVIP-SUB	B5a	MM_CKE	B5b	MP-GOUT-7	B4b	PCI-AD11	B5a
+2V5	B5d	+VTUN	B1b	AV6_VSYNC	B7b	DV1F-CLK	B5c	DV4-DATA8_6	B4b	EJTAG-TMS	B1c	IRQ-ETHERNET	B5a	MM_CLK_N	B5b	MP-GOUT-7	B6	PCI-AD11	B8
+2V5_ATSC	B2a	1V8-PLL	B7c	AV7_C	B3a	EJTAG-TMS	B5a	DV4-DATA8_6	B7b	EJTAG-TMS	B5a	IRQ-ETHERNET	B9a	MM_CLK_P	B5b	MP-GOUT-8	B4b	PCI-AD11	B9a
+2V5A-FAT-MAIN	B2a	2NDSIFEXTM	B3c	AV7_C	B3f	ENABLE-1V2	B1a	DV4-DATA9_7	B4b	ENABLE-1V2	B1a	IRQ-FE-MAIN	B2a	MM_CS0	B5b	MP-GOUT-8	B6	PCI-AD12	B11b
+2V5A-FDC-MAIN	B2a	3V3-APLL	B7c	AV7_Y-CVBS	B3a	ENABLE-1V2	B4e	DV4-DATA9_7	B7b	ENABLE-1V2	B4e	IRQ-FE-MAIN	B5a	MM_DATA_0	B5b	MP-GOUT-9	B4b	PCI-AD12	B5a
+2V5A-MAIN	B2a	3V3-AV1	B7c	BACKLIGHT-CNTRL-OUT	B5e	DV4-VALID	B1a	DV4-VALID	B4b	ENABLE-3V3	B4e	IRQ-HD1	B4e	MM_DATA_1	B5b	MP-GOUT-9	B6	PCI-AD12	B8
+2V5A-PLL-MAIN	B2a	3V3-DIG	B7b	BACKLIGHT-CNTRL-OUT	B6	DV4-VALID	B7b	DV4-DATA0_SOP	B4b	ENABLE-3V3	B4e	IRQ-HD1	B5a	MM_DATA_10	B5b	MP-HS	B6	PCI-AD12	B9a
+2V5A-XTAL-MAIN	B2a	3V3-DIG	B7c	BACKLIGHT-CNTRL-OUT	B6	DV4-VALID	B4e	DV5-DATA0_SOP	B4b	ENABLE-5V	B4g	IRQ-HD2	B4e	MM_DATA_11	B5b	MP-OUT-DE	B4b	PCI-AD13	B11b
+2V5D	B1a	3V3-PLL	B7c	BACKLIGHT-CONTROL	B4e	DV5-DATA0_SOP	B5e	DV5-DATA1_ERR	B7b	ENABLE-5V	B5e	IRQ-HD2	B5a	MM_DATA_12	B5b	MP-OUT-DE	B6	PCI-AD13	B5a
+2V5D	B5b	ADAC1	B3e	BACKLIGHT-CONTROL	B5c	ETX_POD-A(6)	B10a	DV5-DATA1_ERR	B4b	ETX_POD-A(6)	B10a	IRQ-HIRATE	B4e	MM_DATA_13	B5b	MP-OUT-FFIELD	B4b	PCI-AD13	B8
+2V5D-DDR	B5b	ADAC2	B4a	BACKLIGHT-CONTROL	B5e	ETX_POD-A(6)	B10b	DV5-DATA1_ERR	B7b	ETX_POD-A(6)	B10b	IRQ-HIRATE	B5a	MM_DATA_14	B5b	MP-OUT-FFIELD	B6	PCI-AD13	B9a
+2V5-DDRPNX	B4d	ADAC2	B3e	BACKLIGHT-CONTROL	B6	ETX-POD	B10b	DV5-DATA2_0	B4b	ETX-POD	B10b	IRQ-HIRATE	B7b	MM_DATA_15	B5b	MP-OUT-HS	B4b	PCI-AD14	B11b
+2V5D-PLL-MAIN	B2a	ADAC4	B4a	BACKLIGHT-CONTROL	B6	EWV-DRIVE	B3b	DV5-DATA2_0	B7b	EWV-DRIVE	B3b	IRQ-IEEE1394	B11a	MM_DATA_16	B5b	MP-OUT-HS	B6	PCI-AD14	B5a
+2V5M	B6	ADAC4	B3e	BIN-5V	B7a	FAT-ADC-INN-MAIN	B2a	DV5-DATA3_1	B4b	FAT-ADC-INN-MAIN	B2b	IRQ-IEEE1394	B5a	MM_DATA_17	B5b	MP-OUT-VS	B4b	PCI-AD14	B8
+2V5-MAIN	B2a	ADAC7	B3e	BRX0-	B7a	FAT-ADC-INP-MAIN	B2a	DV5-DATA4_2	B7b	FAT-ADC-INP-MAIN	B2b	IRQ-MAIN	B5a	MM_DATA_18	B5b	MP-OUT-VS	B4g	PCI-AD14	B9a
+2V5-VPR	B5c	ADAC7	B4a	BRX1+	B7a	FAT-ADC-INP-MAIN	B2b	DV5-DATA4_2	B7b	FAT-ADC-INP-MAIN	B2b	IRQ-MPIF	B5a	MM_DATA_19	B5b	MP-OUT-VS	B5e	PCI-AD15	B11b
+2V5-VPR	B5d	ADAC8	B3e	BRX2-	B7a	FAT-IF-AGC-MAIN	B2a	DV5-DATA5_3	B4b	FAT-IF-AGC-MAIN	B2b	IRQ-POD	B10a	MM_DATA_2	B5b	MP-OUT-VS	B6	PCI-AD15	B5a
+3V3	B10a	ADAC8	B4a	BRX2+	B7a	FAT-IF-AGC-MAIN	B2b	DV5-DATA5_3	B7b	FAT-IF-AGC-MAIN	B2b	IRQ-POD	B4e	MM_DATA_20	B5b	MP-OUT-VS	B6	PCI-AD15	B8
+3V3	B10b	ADLE	B10a	BRXC-	B7a	FDC-ADC-INN	B2a	DV5-DATA6_4	B4b	FDC-ADC-INN	B2b	IRQ-POD	B5a	MM_DATA_21	B5b	MP-R0	B6	PCI-AD15	B9a
+3V3	B10c	ADLE	B10c	BRXC+	B7a	FDC-ADC-INN	B2b	DV5-DATA6_4	B7b	FDC-ADC-INN	B2b	IRQ-SUB	B5a	MM_DATA_22	B5b	MP-R1	B6	PCI-AD15	B11b
+3V3	B10d	ADOE	B10a	BRX-DDC-SCL	B7a	FDC-ADC-INP	B2a	DV5-DATA7_5	B4b	FDC-ADC-INP	B2b	IRQ-USB20	B5a	MM_DATA_23	B5b	MP-R2	B6	PCI-AD16	B5a
+3V3	B11a	ADOE	B10b	BRX-DDC-SDA	B7a	FDC-ADC-INP	B2b	DV5-DATA7_5	B7b	FDC-ADC-INP	B2b	IRQ-USB20	B8	MM_DATA_24	B5b	MP-R3	B6	PCI-AD16	B8
+3V3	B11b	ADOE	B10c	BRX-HOTPLUG	B7a	FDC-AGC	B2a	DV5-DATA8_6	B4b	FDC-AGC	B2a	ITX_POD-A(5)	B10a	MM_DATA_25	B5b	MP-R4	B6	PCI-AD16	B9a
+3V3	B12	AIN-5V	B7a	CD1	B10a	FDC-AGC	B2b	DV5-DATA8_6	B7b	FDC-AGC	B2b	ITX_POD-A(5)	B10b	MM_DATA_26	B5b	MP-R5	B6	PCI-AD16	B11b
+3V3	B1a	ALE	B4e	CD2	B10a	FE-CLK	B10a	DV5-DATA9_7	B4b	FE-CLK	B10a	ITX_POD-A(5)	B10b	MM_DATA_27	B5b	MP-R6	B6	PCI-AD17	B5a
+3V3	B1c	A-PLOP	B3e	CE1	B10a	FE-CLK	B2a	DV5-DATA9_7	B7b	FE-CLK	B2a	ITX-POD	B10b	MM_DATA_28	B5b	MP-R7	B6	PCI-AD17	B8
+3V3	B2a	A-PLOP	B3g	CE2	B10a	FE-CLK	B10a	DV5-DATA9_7	B7b	FE-CLK	B10a	JTAG-TCK	B10a	MM_DATA_29	B5b	MP-R8	B6	PCI-AD17	B9a
+3V3	B3e	A-PLOP	B4a	CISEL-3V3	B10a	JTAG-TCK	B4e	DV5-DATA9_7	B7b	JTAG-TCK	B4e	JTAG-TCK	B4e	MM_DATA_3	B5b	MP-ROUT-0	B4b	PCI-AD18	B11b
+3V3	B4a	A-PLOP	B5a	CLK-MPIF	B3b	FE-DATA0	B10a	DV5-DATA9_7	B7b	FE-DATA0	B10a	JTAG-TCK	B5a	MM_DATA_30	B5b	MP-ROUT-0	B6	PCI-AD18	B5a
+3V3	B4e	ARX0-	B7a	CLK-MPIF	B4a	FE-DATA1	B10a	DV5-DATA9_7	B7b	FE-DATA1	B10a	JTAG-TCK	B7b	MM_DATA_31	B5b	MP-ROUT-1	B4b	PCI-AD18	B8
+3V3	B4g	ARX0+	B7a	C-MON-OUT	B3f	DV-BOUT-1	B6	DV-BOUT-1	B6	DV-BOUT-1	B6	JTAG-TD-CON-VIPER	B5a	MM_DATA_4	B5b	MP-ROUT-1	B6	PCI-AD18	B9a
+3V3	B5a	ARX1+	B7a	C-MON-OUT	B5c	DV-BOUT-2	B10a	DV-BOUT-2	B5c	DV-BOUT-2	B10a	JTAG-TD-DVB-HDMI	B4e	MM_DATA_5	B5b	MP-ROUT-2	B4b	PCI-AD19	B11b
+3V3	B5c	ARX1+	B7a	COM-SND	B3g	DV-BOUT-3	B6	DV-BOUT-3	B5c	DV-BOUT-3	B6	JTAG-TD-DVB-HDMI	B7b	MM_DATA_6	B5b	MP-ROUT-2	B6	PCI-AD19	B5a
+3V3	B5d	ARX2-	B7a	COM-SND	B4e	DV-BOUT-4	B6	DV-BOUT-4	B5c	DV-BOUT-4	B6	JTAG-TD-HDMI-POD	B10a	MM_DATA_7	B5b	MP-ROUT-3	B4b	PCI-AD19	B8
+3V3	B5e	ARX2+	B7a	COM-SND	B4e	DV-BOUT-5	B6	DV-BOUT-5	B5c	DV-BOUT-5	B6	JTAG-TD-HDMI-POD	B7b	MM_DATA_8	B5b	MP-ROUT-3	B6	PCI-AD19	B9a
+3V3	B6	ARXC-	B7a	CRX_POD-A(8)	B10b	DV-BOUT-6	B6	DV-BOUT-6	B5c	DV-BOUT-6	B6	JTAG-TD-POD-CON	B10a	MM_DATA_9	B5b	MP-ROUT-4	B4b	PCI-AD19	B11b
+3V3	B7a	ARXC+	B7a	CRX_POD-A(8)	B10b	DV-BOUT-7	B6	DV-BOUT-7	B5c	DV-BOUT-7	B6	JTAG-TD-POD-CON	B4e	MM_DOM_0	B5b	MP-ROUT-4	B6	PCI-AD2	B5a
+3V3	B7b	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-8	B6	DV-BOUT-8	B5c	DV-BOUT-8	B6	JTAG-TD-VIPER-PNX2015	B5a	MM_DOM_1	B5b	MP-ROUT-5	B4b	PCI-AD2	B8
+3V3	B7c	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-9	B6	DV-BOUT-9	B5c	DV-BOUT-9	B6	JTAG-TD-VIPER-PNX2015	B10a	MM_DOM_2	B5b	MP-ROUT-5	B6	PCI-AD2	B9a
+3V3	B8	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-10	B6	DV-BOUT-10	B5c	DV-BOUT-10	B6	JTAG-TMS	B4e	MM_DOM_3	B5b	MP-ROUT-6	B4b	PCI-AD20	B11b
+3V3	B9a	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-11	B6	DV-BOUT-11	B5c	DV-BOUT-11	B6	JTAG-TMS	B4e	MM_DOS0	B5b	MP-ROUT-6	B6	PCI-AD20	B5a
+3V3-AV	B7c	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-12	B6	DV-BOUT-12	B5c	DV-BOUT-12	B6	JTAG-TMS	B4e	MM_DOS1	B5b	MP-ROUT-7	B4b	PCI-AD20	B8
+3V3-BUFF	B11b	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-13	B6	DV-BOUT-13	B5c	DV-BOUT-13	B6	JTAG-TMS	B4e	MM_DOS2	B5b	MP-ROUT-7	B6	PCI-AD20	B9a
+3V3-ET-ANA	B9a	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-14	B6	DV-BOUT-14	B5c	DV-BOUT-14	B6	JTAG-TMS	B4e	MM_DOS3	B5b	MP-ROUT-8	B4b	PCI-AD21	B11b
+3V3-ET-DIG	B9a	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-15	B6	DV-BOUT-15	B5c	DV-BOUT-15	B6	JTAG-TMS	B4e	MM_DOS4	B5b	MP-ROUT-8	B6	PCI-AD21	B5a
+3V3M	B6	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-16	B6	DV-BOUT-16	B5c	DV-BOUT-16	B6	JTAG-TMS	B4e	MM_WE	B5b	MP-ROUT-9	B4b	PCI-AD21	B8
+3V3-MAIN	B2a	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-17	B6	DV-BOUT-17	B5c	DV-BOUT-17	B6	JTAG-TMS	B4e	MOCLKA	B10a	MP-ROUT-9	B6	PCI-AD21	B9a
+3V3-STANDBY	B10d	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-18	B6	DV-BOUT-18	B5c	DV-BOUT-18	B6	JTAG-TMS	B4e	MOCLKA-POD	B10a	MP-VS	B6	PCI-AD22	B11b
+3V3-STANDBY	B12	ARXC+	B7a	CRX-POD	B2a	DV-BOUT-19	B6												

SRP Overview SSB

PCI-AD29	B5a	PLL-3V3	B4f	POD-SOP	B10a	SDA-UP-VIP	B4e	TUN-VIPER-RX-DATA9	B4c	VSYNCHIRATE	B7b
PCI-AD29	B8	PLL-OUT	B5a	POD-SOP	B10c	SDA-UP-VIP	B5a	TUN-VIPER-RX-DATA9	B5c	WAITA	B10a
PCI-AD29	B9a	PNX-MA-0	B4d	POD-VALID	B10a	SDM	B3b	TUN-VIPER-TX-BUSY	B4c	WE	B10a
PCI-AD3	B11b	PNX-MA-1	B4d	POD-VALID	B10c	SDM	B4e	TUN-VIPER-TX-BUSY	B5c	XIO-A0_CLE	B10c
PCI-AD3	B5a	PNX-MA-10	B4d	POD-VCC	B10a	SEL-IF-LL1	B5a	TUN-VIPER-TX-CLKN	B4c	XIO-A0_CLE	B10d
PCI-AD3	B8	PNX-MA-11	B4d	POD-VPP	B10a	SEL-IF-LL2	B3c	TUN-VIPER-TX-CLKN	B5c	XIO-A0_CLE	B11b
PCI-AD3	B9a	PNX-MA-12	B4d	POWERDOWN-1394	B11a	SEL-IF-LL2	B5a	TUN-VIPER-TX-CLKP	B4c	XIO-A1_ALE	B10c
PCI-AD30	B10c	PNX-MA-2	B4d	POWERDOWN-1394	B5a	SEL-POD	B10c	TUN-VIPER-TX-CLKP	B5c	XIO-A1_ALE	B10d
PCI-AD30	B10d	PNX-MA-3	B4d	POWERDOWN-1394	B7b	SEL-POD	B2a	TUN-VIPER-TX-DATA0	B4c	XIO-A1_ALE	B11a
PCI-AD30	B11b	PNX-MA-4	B4d	POWER-OK-DISPLAY	B4e	SOUND-ENABLE	B3g	TUN-VIPER-TX-DATA0	B5c	XIO-A1_ALE	B11b
PCI-AD30	B5a	PNX-MA-5	B4d	POWER-OK-DISPLAY	B5e	SOUND-ENABLE	B5a	TUN-VIPER-TX-DATA1	B4c	XIO-A10	B10c
PCI-AD30	B8	PNX-MA-6	B4d	POWER-OK-PLATFORM	B5a	SOUND-ENABLE-VPR	B5a	TUN-VIPER-TX-DATA1	B5c	XIO-A10	B11a
PCI-AD30	B9a	PNX-MA-7	B4d	POWER-OK-PLATFORM	B5e	SPDIF-HDMI	B5c	TUN-VIPER-TX-DATA10	B4c	XIO-A10	B11b
PCI-AD31	B10c	PNX-MA-8	B4d	POWER-OK-PLATFORM-3V3	B4e	SPDIF-HDMI	B7b	TUN-VIPER-TX-DATA10	B5c	XIO-A11	B10c
PCI-AD31	B10d	PNX-MA-9	B4d	POWER-OK-PLATFORM-3V3	B5a	SPDIF-IN1	B3e	TUN-VIPER-TX-DATA11	B4c	XIO-A11	B11a
PCI-AD31	B11b	PNX-MBA0	B4d	PROT-AUDIOSUPPLY	B3e	SPDIF-IN1	B5c	TUN-VIPER-TX-DATA11	B5c	XIO-A11	B11b
PCI-AD31	B5a	PNX-MBA1	B4d	PROT-AUDIOSUPPLY	B3g	SPDIF-OUT1	B3e	TUN-VIPER-TX-DATA12	B4c	XIO-A12	B10c
PCI-AD31	B8	PNX-MCAS	B4d	PROT-AUDIOSUPPLY	B4e	SPDIF-OUT1	B5c	TUN-VIPER-TX-DATA12	B5c	XIO-A12	B11a
PCI-AD31	B9a	PNX-MCKE	B4d	PROT-AUDIOSUPPLY	B5e	SPI-1	B3e	TUN-VIPER-TX-DATA13	B4c	XIO-A12	B11b
PCI-AD4	B11b	PNX-MCLK-N	B4d	PSEN	B4e	SPI-1	B3g	TUN-VIPER-TX-DATA13	B5c	XIO-A13	B10c
PCI-AD4	B5a	PNX-MCLK-P	B4d	QTX_POD-A(7)	B10a	SPI-CLK	B4e	TUN-VIPER-TX-DATA14	B4c	XIO-A13	B11a
PCI-AD4	B8	PNX-MCS-0	B4d	QTX_POD-A(7)	B10b	SPI-CSB	B4e	TUN-VIPER-TX-DATA14	B5c	XIO-A13	B11b
PCI-AD4	B9a	PNX-MDATA-0	B4d	QTX-POD	B10b	SPI-OUT	B3e	TUN-VIPER-TX-DATA15	B4c	XIO-A14	B11a
PCI-AD5	B11b	PNX-MDATA-1	B4d	RC	B3f	SPI-OUT	B3g	TUN-VIPER-TX-DATA15	B5c	XIO-A14	B11b
PCI-AD5	B5a	PNX-MDATA-10	B4d	RC	B4e	SPI-PROG	B3b	TUN-VIPER-TX-DATA2	B4c	XIO-A15	B11a
PCI-AD5	B8	PNX-MDATA-11	B4d	RDY_IRQA	B10a	SPI-PROG	B4e	TUN-VIPER-TX-DATA2	B5c	XIO-A15	B11b
PCI-AD5	B9a	PNX-MDATA-12	B4d	REG	B10a	SPI-SDI	B4e	TUN-VIPER-TX-DATA3	B4c	XIO-A16_D8	B10d
PCI-AD6	B11b	PNX-MDATA-13	B4d	REGIMBEAU	B3f	SPI-SDO	B4e	TUN-VIPER-TX-DATA3	B5c	XIO-A16_D8	B11b
PCI-AD6	B5a	PNX-MDATA-14	B4d	REGIMBEAU	B5a	SPI-WP	B4e	TUN-VIPER-TX-DATA4	B4c	XIO-A17_D9	B10d
PCI-AD6	B8	PNX-MDATA-15	B4d	REGIMBEAU-AV6-VSYNC	B3f	STANDBY	B12	TUN-VIPER-TX-DATA4	B5c	XIO-A17_D9	B11b
PCI-AD6	B9a	PNX-MDATA-2	B4d	RESET-1394	B11a	STANDBY	B5e	TUN-VIPER-TX-DATA5	B4c	XIO-A18_D10	B10d
PCI-AD7	B11b	PNX-MDATA-3	B4d	RESET-1394	B5a	STBY-WP-NAND-FLASH	B10d	TUN-VIPER-TX-DATA5	B5c	XIO-A18_D10	B11b
PCI-AD7	B5a	PNX-MDATA-4	B4d	RESET-AUDIO	B4a	STBY-WP-NAND-FLASH	B4e	TUN-VIPER-TX-DATA6	B4c	XIO-A19_D11	B10d
PCI-AD7	B8	PNX-MDATA-5	B4d	RESET-AUDIO	B4e	STROBE1N-MAIN	B3a	TUN-VIPER-TX-DATA6	B5c	XIO-A19_D11	B11b
PCI-AD7	B9a	PNX-MDATA-6	B4d	RESET-ETHERNET	B5a	STROBE1N-MAIN	B4a	TUN-VIPER-TX-DATA7	B4c	XIO-A2	B10c
PCI-AD8	B11b	PNX-MDATA-7	B4d	RESET-ETHERNET	B9a	STROBE1P-MAIN	B3a	TUN-VIPER-TX-DATA7	B5c	XIO-A2	B11b
PCI-AD8	B5a	PNX-MDATA-8	B4d	RESET-FE-MAIN	B2a	STROBE1P-MAIN	B4a	TUN-VIPER-TX-DATA8	B4c	XIO-A20_D12	B10d
PCI-AD8	B8	PNX-MDATA-9	B4d	RESET-FE-MAIN	B5a	STROBE2N-MAIN	B3a	TUN-VIPER-TX-DATA8	B5c	XIO-A20_D12	B11b
PCI-AD8	B9a	PNX-MDQM-0	B4d	RESET-MAIN-NVM	B10d	STROBE2N-MAIN	B4a	TUN-VIPER-TX-DATA9	B4c	XIO-A21_D13	B10d
PCI-AD9	B11b	PNX-MDQM-1	B4d	RESET-MAIN-NVM	B4e	STROBE2P-MAIN	B3a	TUN-VIPER-TX-DATA9	B5c	XIO-A21_D13	B11b
PCI-AD9	B5a	PNX-MDQS-0	B4d	RESET-MIPS	B4e	STROBE2P-MAIN	B4a	TXD	B10d	XIO-A22_D14	B10d
PCI-AD9	B8	PNX-MDQS-1	B4d	RESET-MIPS	B5a	STROBE3N-MAIN	B3a	TXD	B1c	XIO-A22_D14	B11b
PCI-AD9	B9a	PNX-MRAS	B4d	RESET-PNX2015	B4e	STROBE3N-MAIN	B4a	TXD	B9b	XIO-A23_D15	B10d
PCI-CBE0	B5a	PNX-MWE	B4d	RESET-POD-CI	B10a	STROBE3P-MAIN	B3a	TXD-UP	B10d	XIO-A23_D15	B11b
PCI-CBE0	B8	POD-A(0)	B10a	RESET-POD-CI	B5a	STROBE3P-MAIN	B4a	TXD-UP	B4e	XIO-A3	B10c
PCI-CBE0	B9a	POD-A(0)	B10c	RESET-STBY	B12	SUPPLY-FAULT	B10a	TXD-VIPER	B10d	XIO-A3	B11b
PCI-CBE1	B11b	POD-A(1)	B10a	RESET-STBY	B4e	SUPPLY-FAULT	B1a	TXD-VIPER	B5a	XIO-A4	B10c
PCI-CBE1	B5a	POD-A(1)	B10c	RESET-SYSTEM	B1c	SUPPLY-FAULT	B4e	TXPNXA-	B4b	XIO-A4	B11b
PCI-CBE1	B8	POD-A(10)	B10a	RESET-SYSTEM	B4e	SUPPLY-FAULT	B5e	TXPNXA-	B4g	XIO-A5	B10c
PCI-CBE1	B9a	POD-A(10)	B10c	RESET-SYSTEM	B5a	TEMP-SENSOR	B4e	TXPNXA+	B4b	XIO-A5	B11b
PCI-CBE2	B11b	POD-A(11)	B10a	RESET-USB20	B5a	TS-CLK	B11a	TXPNXA+	B4g	XIO-A6	B10c
PCI-CBE2	B5a	POD-A(11)	B10c	RESET-USB20	B8	TS-CLK	B5c	TXPNXB-	B4b	XIO-A6	B11b
PCI-CBE2	B8	POD-A(12)	B10a	RSTA	B10a	TS-DATA0	B11a	TXPNXB-	B4g	XIO-A7	B10c
PCI-CBE2	B9a	POD-A(12)	B10c	RXD	B10d	TS-DATA0	B5c	TXPNXB+	B4b	XIO-A7	B11b
PCI-CBE3	B5a	POD-A(13)	B10a	RXD	B1c	TS-DATA1	B11a	TXPNXB+	B4g	XIO-A8	B10c
PCI-CBE3	B8	POD-A(13)	B10c	RXD	B9b	TS-DATA1	B5c	TXPNXC-	B4b	XIO-A8	B11b
PCI-CBE3	B9a	POD-A(2)	B10a	RXD-UP	B10d	TS-DATA2	B11a	TXPNXC-	B4g	XIO-A9	B10c
PCI-CLK-ETHERNET	B5a	POD-A(2)	B10c	RXD-UP	B4e	TS-DATA2	B5c	TXPNXC+	B4b	XIO-A9	B11b
PCI-CLK-ETHERNET	B9a	POD-A(3)	B10a	RXD-VIPER	B10d	TS-DATA3	B11a	TXPNXC+	B4g	XIO-ACK	B10d
PCI-CLK-USB20	B5a	POD-A(3)	B10c	RXD-VIPER	B5a	TS-DATA3	B5c	TXPNXC+	B4b	XIO-ACK	B11b
PCI-CLK-USB20	B8	POD-A(4)	B10b	SCL-DMA	B5a	TS-DATA4	B11a	TXPNXC+	B4g	XIO-AS_REn	B5a
PCI-CLK-VPR	B5a	POD-A(4)	B10c	SCL-DMA-BUS1	B11a	TS-DATA4	B5c	TXPNXC+	B4b	XIO-AS_REn	B10a
PCI-DEVSEL	B5a	POD-A(5)	B10b	SCL-DMA-BUS1	B12	TS-DATA5	B11a	TXPNXC+	B4g	XIO-AS_REn	B10d
PCI-DEVSEL	B8	POD-A(5)	B10c	SCL-DMA-BUS1	B5a	TS-DATA5	B5c	TXPNXC+	B4b	XIO-AS_REn	B11a
PCI-DEVSEL	B9a	POD-A(6)	B10b	SCL-DMA-BUS1-ATSC	B12	TS-DATA6	B11a	TXPNXC+	B4g	XIO-AS_REn	B11b
PCI-FRAME	B5a	POD-A(6)	B10c	SCL-DMA-BUS1-ATSC	B2a	TS-DATA6	B5c	TXPNXD+	B4b	XIO-D0	B11a
PCI-FRAME	B8	POD-A(7)	B10b	SCL-DMA-BUS2	B3b	TS-DATA7	B11a	TXPNXD+	B4g	XIO-D0	B11b
PCI-FRAME	B9a	POD-A(7)	B10c	SCL-DMA-BUS2	B4e	TS-DATA7	B5c	TXPNXD+	B4b	XIO-D1	B11a
PCI-GNT	B5a	POD-A(8)	B10b	SCL-DMA-BUS2	B5a	TS-SOP	B11a	TXPNXE-	B4g	XIO-D10	B11a
PCI-GNT	B8	POD-A(8)	B10c	SCL-i2C4	B4g	TS-SOP	B5c	TXPNXE+	B4b	XIO-D10	B5a
PCI-GNT-A	B5a	POD-A(9)	B10b	SCL-i2C4	B5a	TS-VALID	B11a	TXPNXE+	B4g	XIO-D11	B11a
PCI-GNT-A	B9a	POD-A(9)	B10c	SCL-i2C4	B5e	TS-VALID	B5c	TXPNXE+	B4b	XIO-D11	B5a
PCI-INTA	B5a	POD-CLK	B10a	SCL-i2C4-DISP	B4g	TUNERAGC-MON	B2a	UART-SWITCH	B10d	XIO-D12	B11a
PCI-IRDY	B5a	POD-CLK	B10c	SCL-MM	B3g	TUNERAGC-MON	B2b	UART-SWITCHn	B10d	XIO-D12	B5a
PCI-IRDY	B8	POD-D(0)	B10a	SCL-MM	B5a	TUN-VIPER-RX-BUSY	B4c	UP-3V3	B4f	XIO-D13	B11a
PCI-IRDY	B9a	POD-D(0)	B10c	SCL-MM-BUS1	B10a	TUN-VIPER-RX-BUSY	B5c	USB1-DM	B5a	XIO-D13	B5a
PCI-PAR	B5a	POD-D(1)	B10a	SCL-MM-BUS1	B5a	TUN-VIPER-RX-CLKN	B4c	USB1-DP	B5a	XIO-D14	B11a
PCI-PAR	B8	POD-D(1)	B10c	SCL-MM-BUS1	B6	TUN-VIPER-RX-CLKN	B5c	USB20-DM1	B8	XIO-D14	B5a
PCI-PAR	B9a	POD-D(2)	B10a	SCL-MM-BUS1	B7b	TUN-VIPER-RX-CLKP	B4c	USB20-DP1	B8	XIO-D15	B11a
PCI-PERR	B5a	POD-D(2)	B10c	SCL-MOP	B5e	TUN-VIPER-RX-CLKP	B5c	USB20-OC1	B5a	XIO-D15	B5a
PCI-PERR	B8	POD-D(3)	B10a	SCL-MOP	B6	TUN-VIPER-RX-DATA0	B4c	USB20-OC1	B8	XIO-D2	B11a
PCI-PERR	B9a	POD-D(3)	B10c	SCL-UP-SW	B4e	TUN-VIPER-RX-DATA0	B5c	USB20-OC2	B8	XIO-D2	B11b
PCI-REQ	B5a	POD-D(4)	B10a	SCL-UP-SW	B5e	TUN-VIPER-RX-DATA1	B4c	USB20-PWE1	B5a	XIO-D3	B11a
PCI-REQ	B8	POD-D(4)	B10c	SCL-UP-VIP	B10d	TUN-VIPER-RX-DATA1	B5c	USB20-PWE1	B8	XIO-D3	B11b
PCI-REQ-A	B5a	POD-D(5)	B10a	SCL-UP-VIP	B4e	TUN-VIPER-RX-DATA10	B4c	USB2-DM	B5a	XIO-D4	B11a
PCI-REQ-A	B9a	POD-D(5)	B10c	SCL-UP-VIP	B5a	TUN-VIPER-RX-DATA10	B5c	USB2-DP	B5a	XIO-D4	B11b
PCI-REQ-B	B10a	POD-D(6)	B10a	SDA-DMA	B5a	TUN-VIPER-RX-DATA10	B4c	USB-BUS-PW	B5a	XIO-D5	B11a
PCI-REQ-B	B5a	POD-D(6)	B10c	SDA-DMA-BUS1	B11a	TUN-VIPER-RX-DATA11	B5c	USB-OVERCUR	B5a	XIO-D5	B11b
PCI-SERR	B5a	POD-D(7)	B10a	SDA-DMA-BUS1	B12	TUN-VIPER-RX-DATA12	B4c	VCC_EXT0	B10a	XIO-D6	B11a
PCI-SERR	B8	POD-D(7)	B10c	SDA-DMA-BUS1	B5a	TUN-VIPER-RX-DATA12	B5c	VCCEN	B10a	XIO-D6	B11b
PCI-SERR	B9a	POD-DATA0	B10a	SDA-DMA-BUS1-ATSC	B12	TUN-VIPER-RX-DATA13	B4c	VDISP	B4g	XIO-D7	B11a
PCI-STOP	B5a	POD-DATA0	B10c	SDA-DMA-BUS1-ATSC	B2a	TUN-VIPER-RX-DATA13	B5c	VDISP2	B4g	XIO-D7	B11b
PCI-STOP	B8	POD-DATA1	B10a	SDA-DMA-BUS2	B3b	TUN-VIPER-RX-DATA14	B4c	VISUAL-CHECK	B3c	XIO-D8	B11a
PCI-STOP	B9a	POD-DATA1	B10c	SDA-DMA-BUS2	B4e	TUN-VIPER-RX-DATA14	B5c	VPPEN	B10a	XIO-D8	B5a
PCI-TRDY	B5a	POD-DATA2	B10a	SDA-DMA-BUS2	B5a	TUN-VIPER-RX-DATA15	B4c	VREF-AUD	B3e	XIO-D9	B11a
PCI-TRDY	B8	POD-DATA2	B10c	SDA-i2C4	B4g	TUN-VIPER-RX-DATA15	B5c	VREF-AUD-POS	B3b	XIO-D9	B5a
PCI-TRDY	B9a	POD-DATA3	B10a	SDA-i2C4	B5a	TUN-VIPER-RX-DATA2	B4c	VREF-AUD-POS	B4a	XIO-RWn_WEn	B10a
PDIR	B10a	POD-DATA3	B10c	SDA-i2C4	B5e	TUN-VIPER-RX-DATA2	B5c	VREF-DEFL	B3b	XIO-RWn_WEn	B10d
PDIR	B10b	POD-DATA4	B10a	SDA-i2C4-DISP	B4g	TUN-VIPER-RX-DATA3	B4c	VREF-PNX	B4c	XIO-RWn_WEn	B11a
PDOE	B10a	POD-DATA4	B10c	SDA-MM	B3g	TUN-VIPER-RX-DATA3	B5c	VREF-PNX	B4d	XIO-RWn_WEn	B11b
PDOE	B10b	POD-DATA5	B10a	SDA-MM	B5a	TUN-VIPER-RX-DATA4	B4c	VREF-VPR	B5b	XIO-SEL0	B10d
PHY-D(0)	B11a	POD-DATA5	B10c	SDA-MM-BUS1	B10a	TUN-VIPER-RX-DATA4	B5c	VS1	B10a	XIO-SEL0	B11b
PHY-D(1)	B11a	POD-DATA6	B10a	SDA-MM-BUS1	B5a	TUN-VIPER-RX-DATA5	B4c	VS2	B10a	XIO-SEL0	B5a
PHY-D(2)	B11a	POD-DATA6	B10c	SDA-MM-BUS1	B6	TUN-VIPER-RX-DATA5	B5c	VS2	B10b	XIO-SEL1	B11a
PHY-D(3)	B11a	POD-DATA7	B10a	SDA-MM-BUS1	B7b	TUN-VIPER-RX-DATA6	B4c	VS2_MOCLKA-CI	B10a	XIO-SEL1	B11b
PHY-D(4)	B11a	POD-DATA7	B10c	SDA-MOP	B5e	TUN-VIPER-RX-DATA6	B5c	VS2_MOCLKA-CI	B10b	XIO-SEL1	B5a
PHY-D(5)	B11a	POD-MODE	B12	SDA-MOP	B6	TUN-VIPER-RX-DATA7	B4c	VSW	B1a	XIO-SEL2	B10a
PHY-D(6)	B11a	POD-MODE	B1a	SDA-UP-SW	B4e	TUN-VIPER-RX-DATA7	B5c	VSW	B1b	XIO-SEL2	B5a
PHY-D(7)	B11a	POD-MODE	B4e	SDA-UP-SW	B5e	TUN-VIPER-RX-DATA8	B4c	VSYNCHIRATE	B5a	Y-CVBS-MON-OUT	B3b
PLL-1V2	B4f	POD-MODE	B4g	SDA-UP-VIP	B10d	TUN-VIPER-RX-DATA8	B5c	VSYNCHIRATE	B7a	Y-CVBS-MON-OUT	B3f

1.1. Introduction

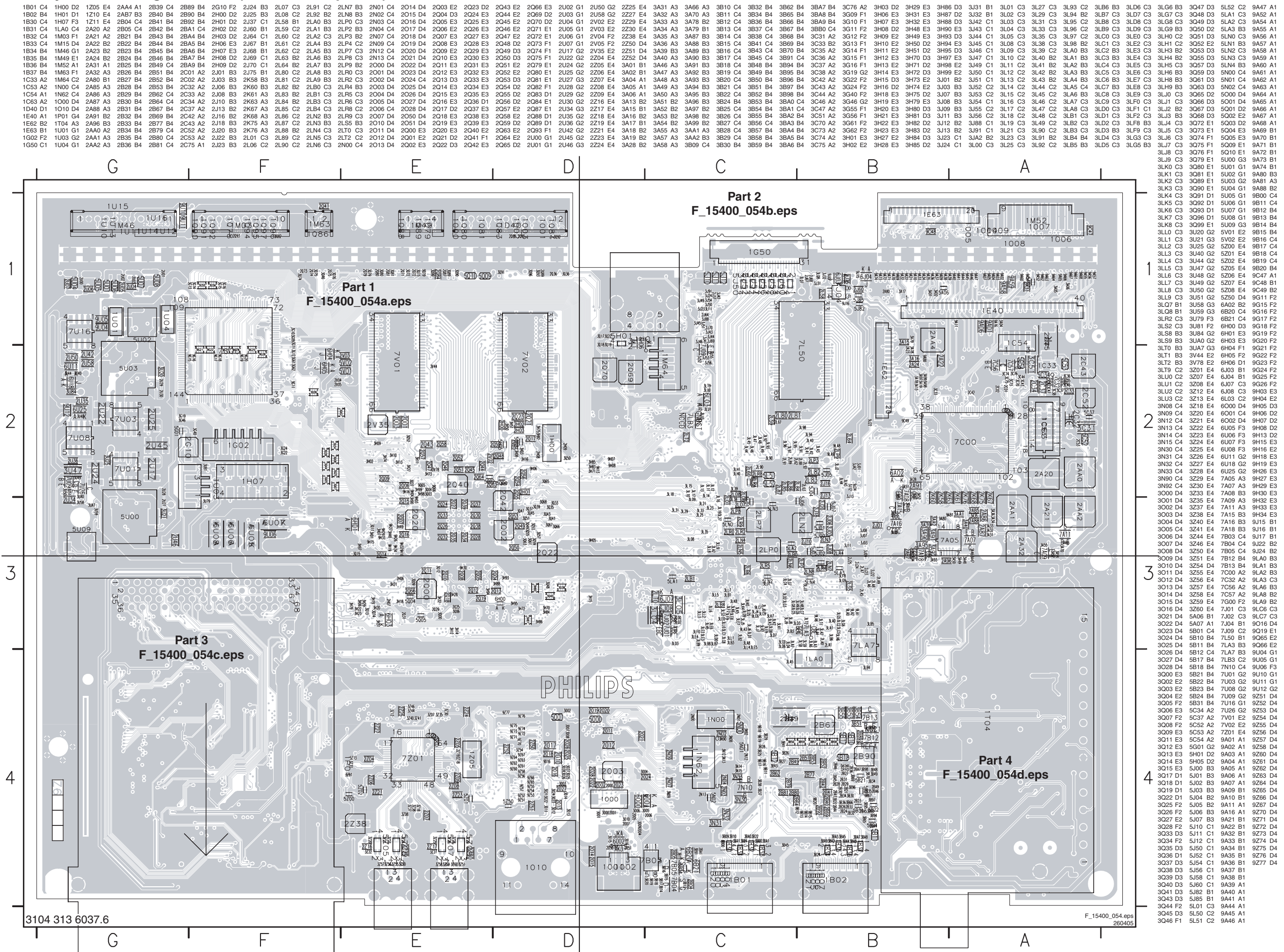
SRP (Service Reference Protocol) is a software tool that creates a list with all references to signal lines. The list contains references to the signals within all schematics of a PWB. It replaces the text references currently printed next to the signal names in the schematics. These printed references are created manually and are therefore not guaranteed to be 100% correct. In addition, in the current crowded schematics there is often none or very little place for these references. Some of the PWB schematics will use SRP while others will still use the manual references. Either there will be an SRP reference list for a schematic, or there will be printed references in the schematic.

1.2. Non-SRP Schematics

There are several different signals available in a schematic:

</

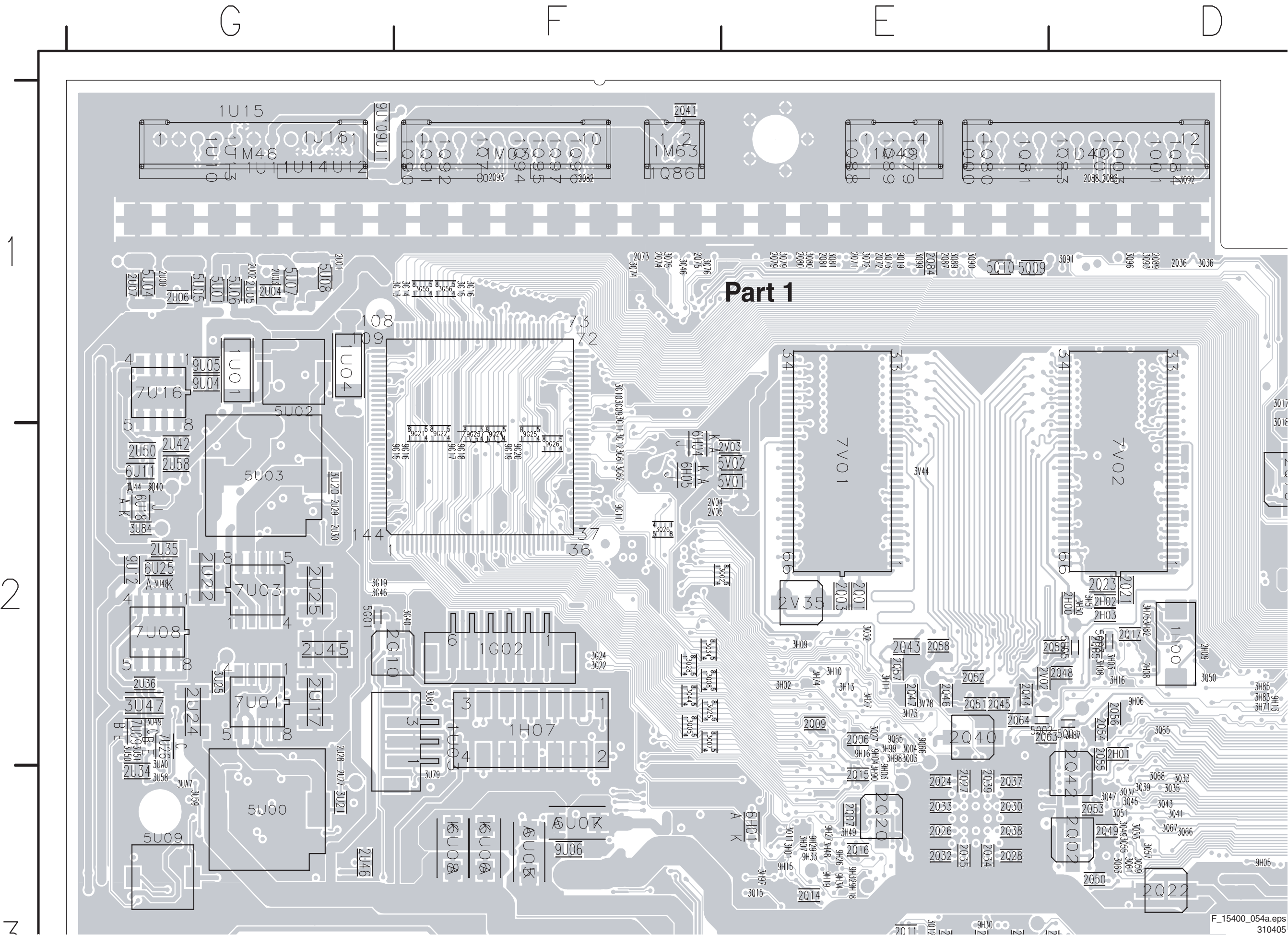
Layout Small Signal Board (Overview Top Side)



3104 313 6037.6

F_15400_054c.eps
260405

Layout Small Signal Board (Part 1 Top Side)



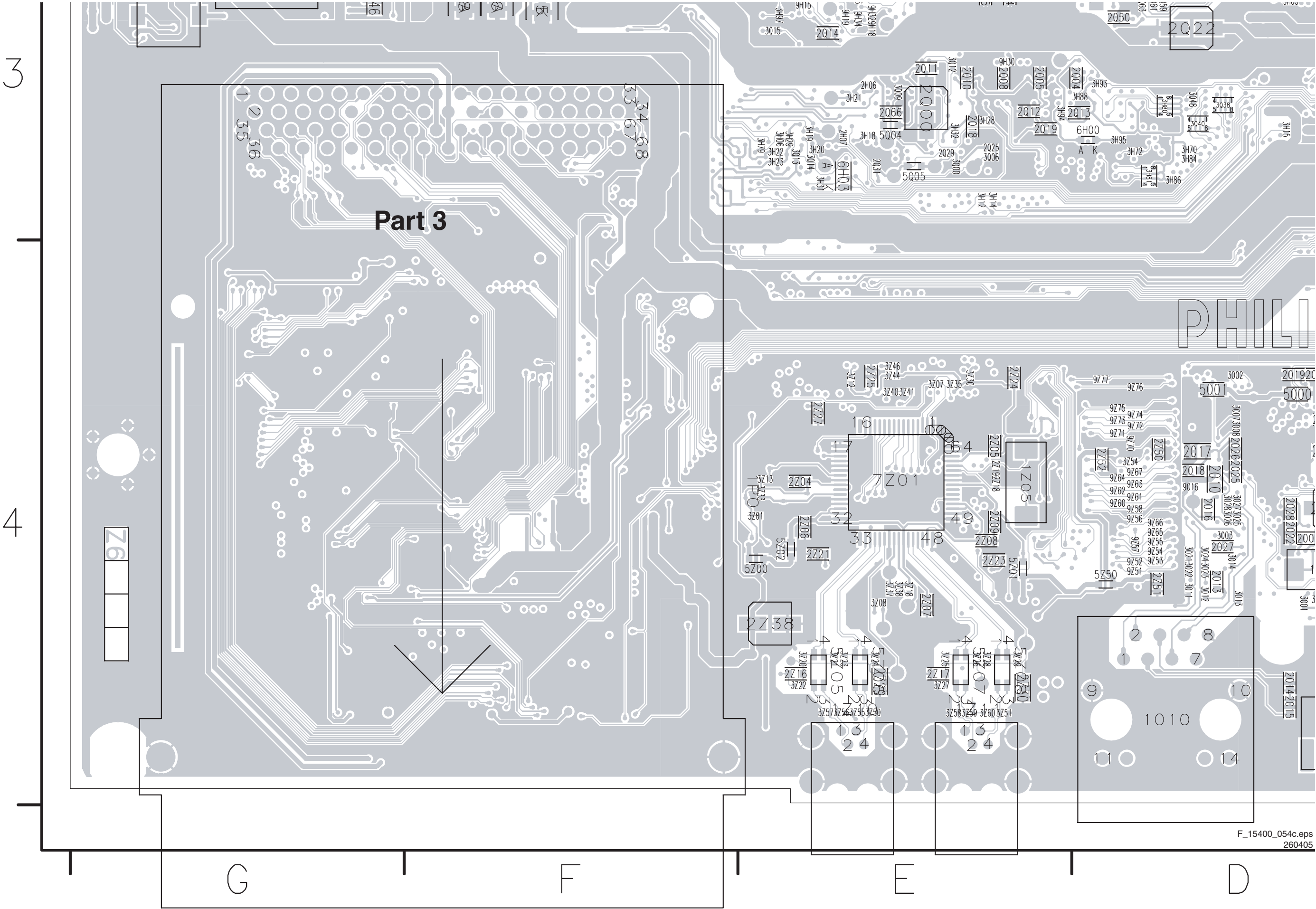
D

C

B

A

Layout Small Signal Board (Part 3 Top Side)



Part 4

3

4

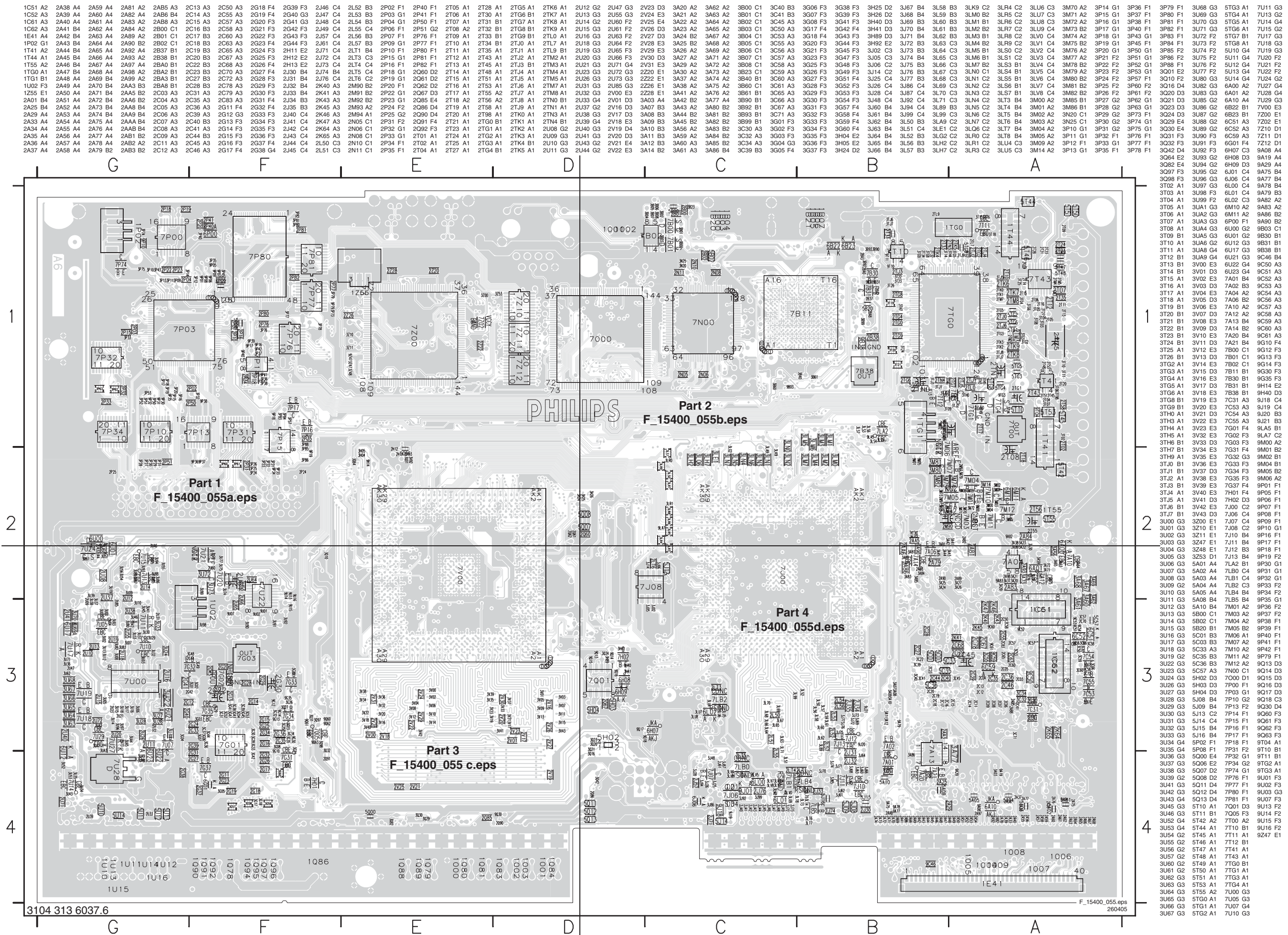
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C

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A

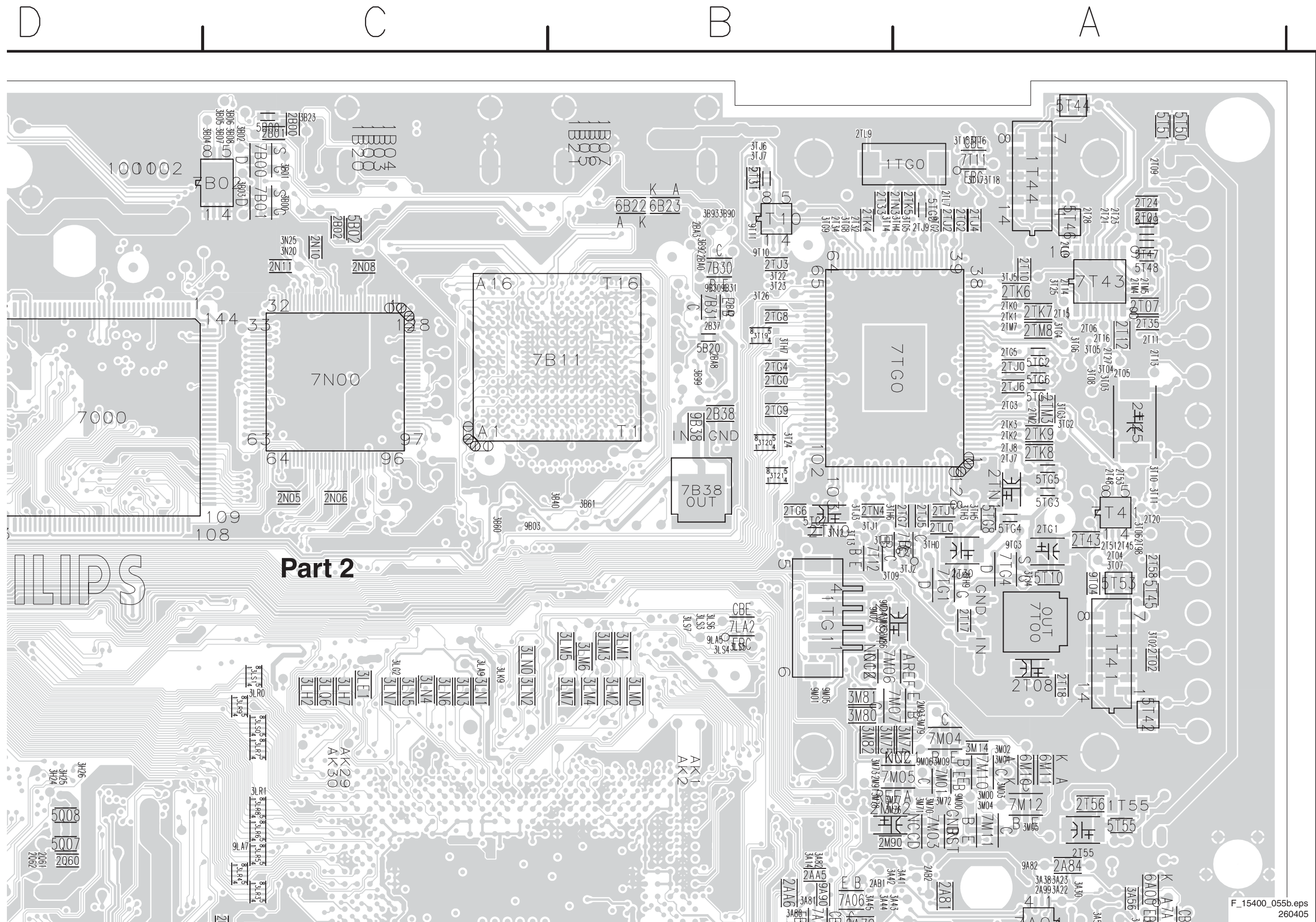
Layout Small Signal Board (Overview Bottom Side)



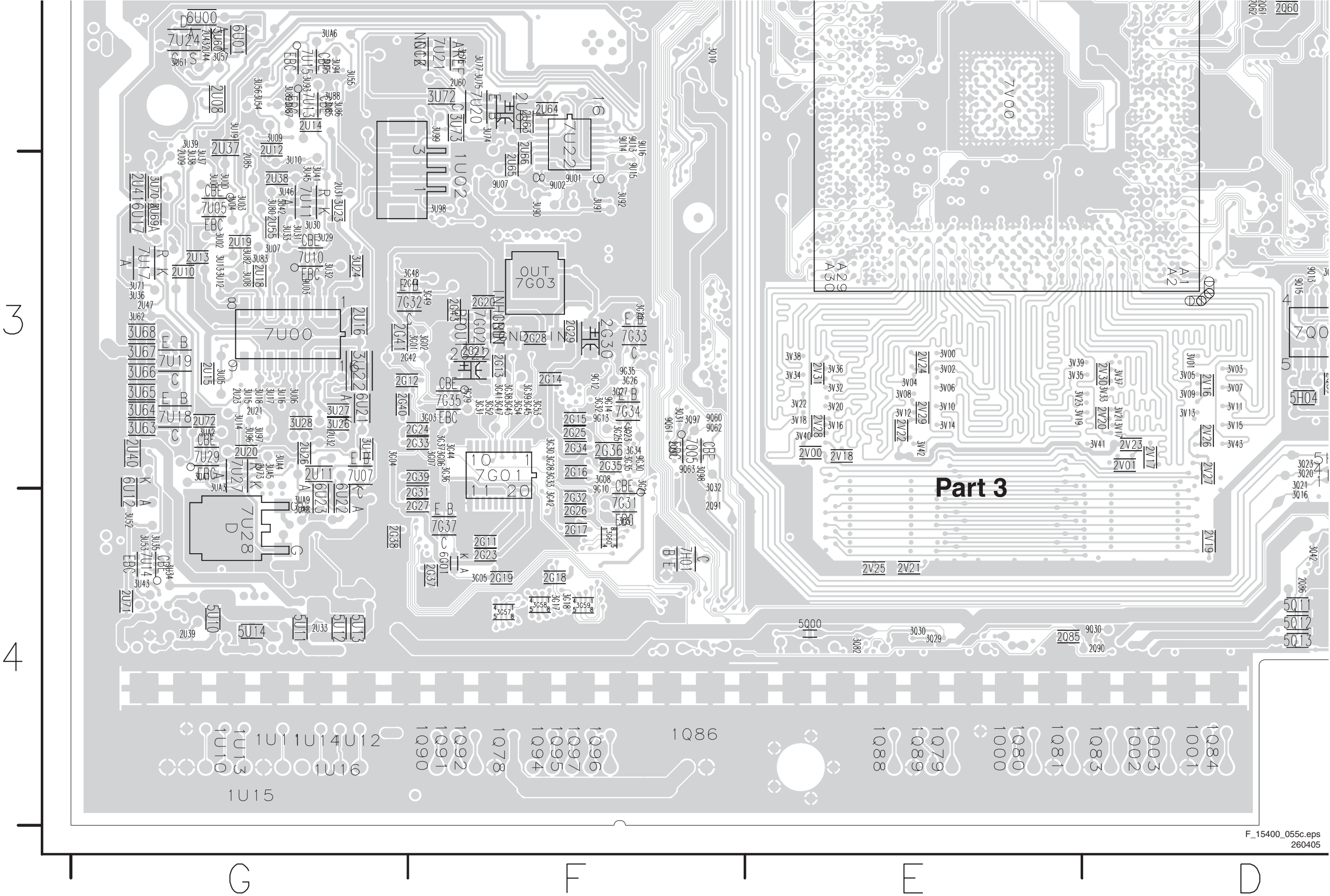
D



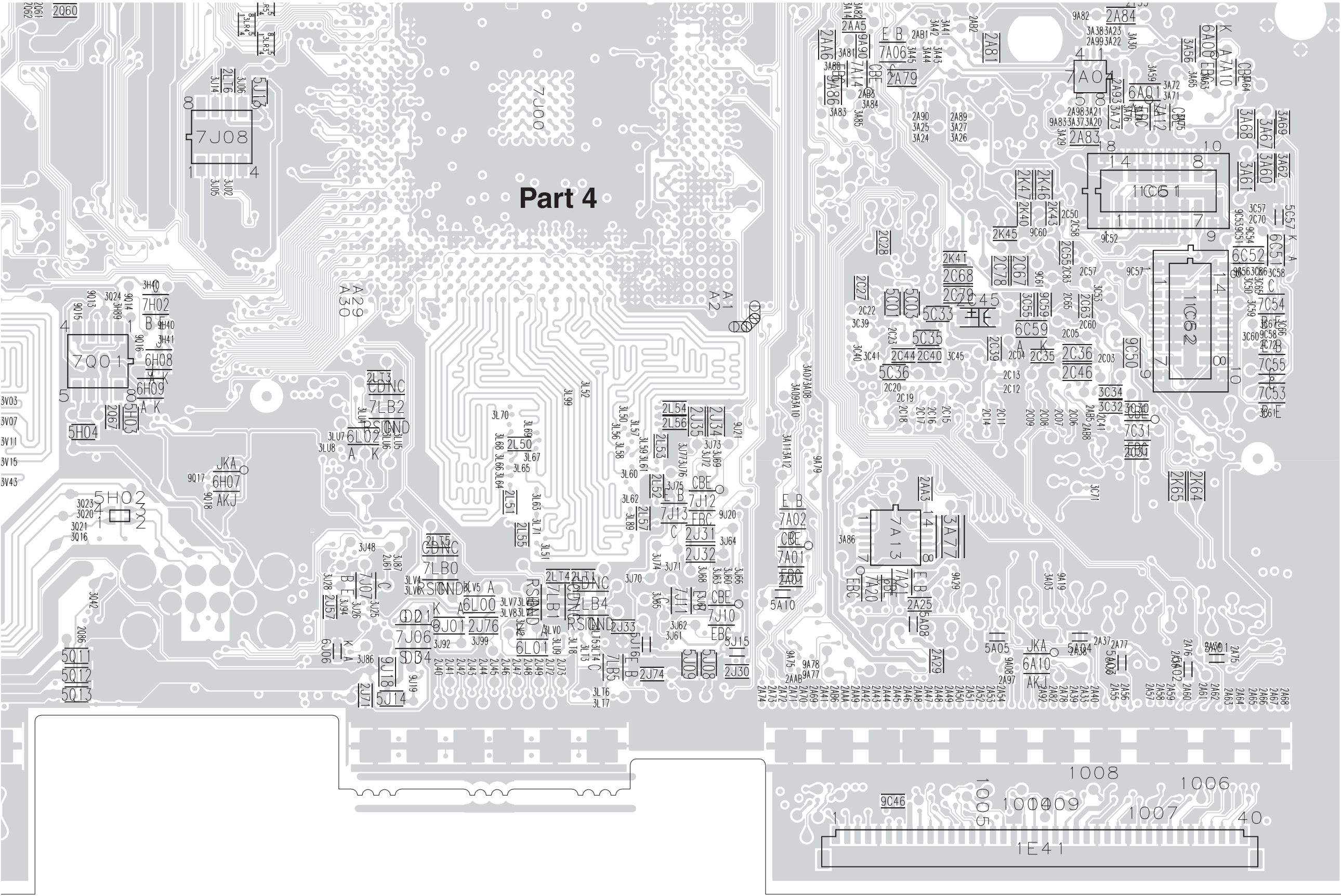
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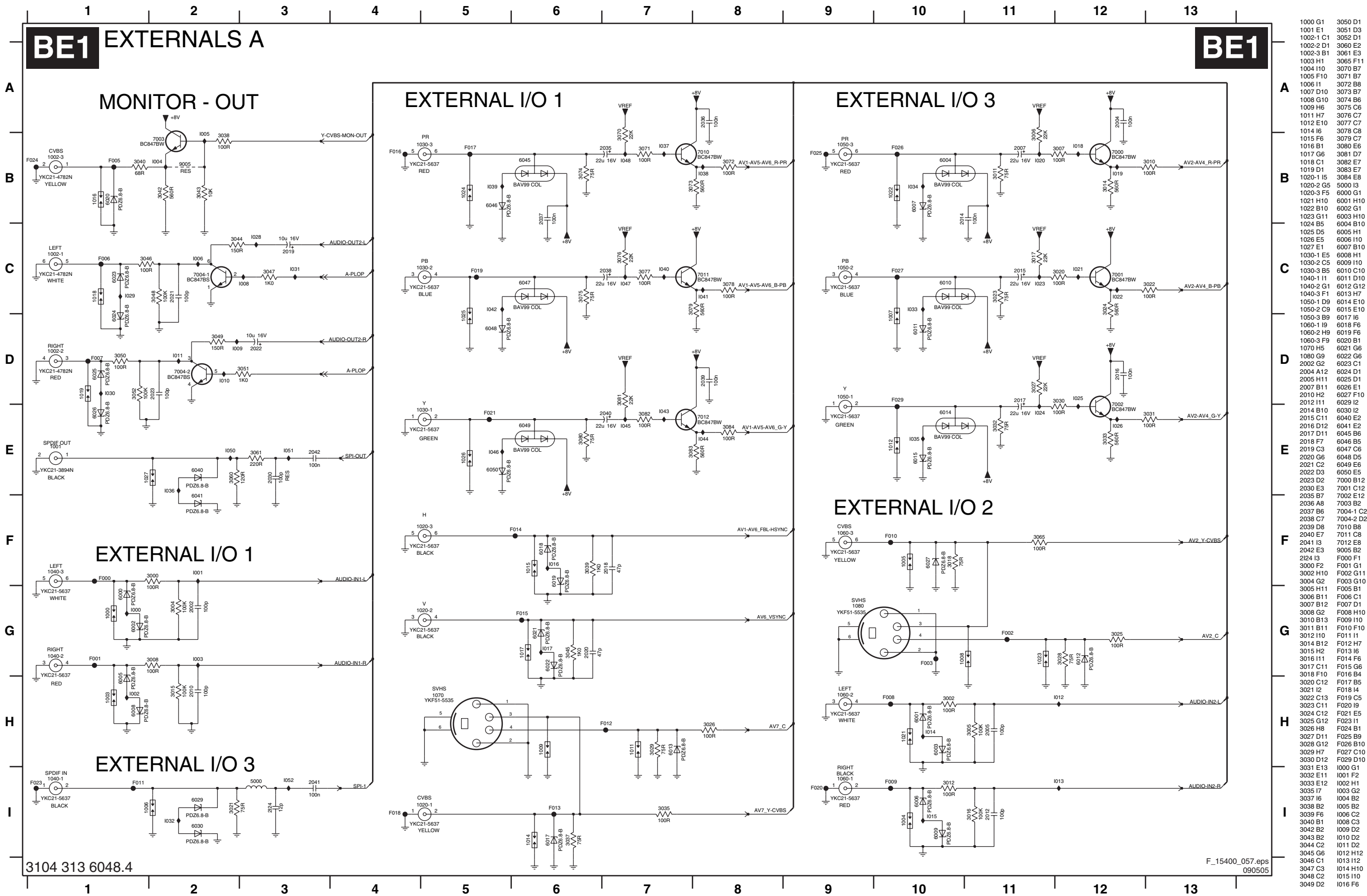
Layout Small Signal Board (Part 3 Bottom Side)



Layout Small Signal Board (Part 4 Bottom Side)

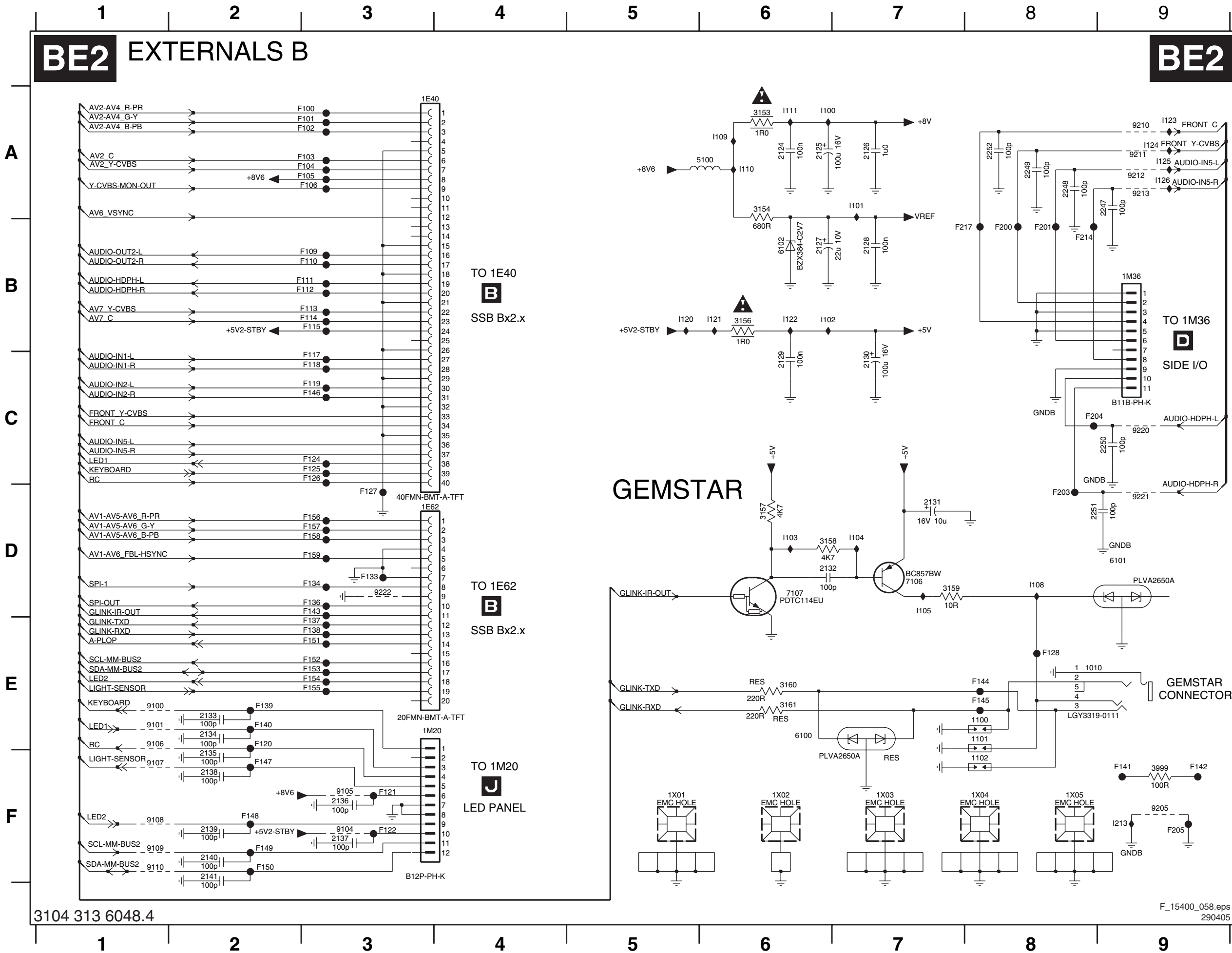


External I/O Panel: Externals A



1000 G1	3050 D1	I017 G6
1001 E1	3051 D3	I018 B12
1002-1 C1	3052 D1	I019 B12
1002-2 D1	3060 E2	I020 B11
1002-3 B1	3061 E3	I021 C12
1003 H1	3065 F11	I022 C12
1004 I10	3070 B7	I023 C11
1005 F10	3071 B7	I024 E11
1006 I1	3072 B8	I025 D12
1007 D10	3073 B7	I026 E12
1008 G10	3074 B6	I028 C3
1009 H6	3075 C6	I029 C1
1011 H7	3076 C7	I030 D1
1012 E10	3077 C7	I031 C3
1014 I6	3078 C8	I032 I2
1015 F6	3079 C7	I033 C10
1016 B1	3080 E6	I034 B10
1017 G6	3081 D7	I035 E10
1018 C1	3082 E7	I036 E2
1019 D1	3083 E7	I037 B7
1020-1 I5	3084 E8	I038 B8
1020-2 G5	5000 I3	I039 B5
1020-3 F5	6000 G1	I040 C7
1021 H10	6001 H10	I041 C8
1022 B10	6002 G1	I042 C5
1023 G11	6003 H10	I043 E7
1024 B5	6004 B10	I044 E8
1025 D5	6005 H1	I045 E7
1026 E5	6006 I10	I046 E5
1027 E1	6007 B10	I047 C7
1030-1 E5	6008 H1	I048 B7
1030-2 C5	6009 I10	I050 E2
1030-3 B5	6010 C10	I051 E3
1040-1 I1	6011 D10	I052 I3
1040-2 G1	6012 G12	
1040-3 F1	6013 H7	
1050-1 D9	6014 E10	
1050-2 C9	6015 E10	
1050-3 B9	6017 I6	
1060-1 I9	6018 F6	
1060-2 H9	6019 F6	
1060-3 F9	6020 B1	
1070 H5	6021 G6	
1080 G9	6022 G6	
2002 G2	6023 C1	
2004 A12	6024 D1	
2005 H11	6025 D1	
2007 B11	6026 E1	
2010 H2	6027 F10	
2012 I11	6029 I2	
2014 B10	6030 I2	
2015 C11	6040 E2	
2016 D12	6041 E2	
2017 D11	6045 B6	
2018 F7	6046 B5	
2019 C3	6047 C6	
2020 G6	6048 D5	
2021 C2	6049 E6	
2022 D3	6050 E5	
2023 D2	7000 B12	
2030 E3	7001 C12	
2035 B7	7002 E12	
2036 A8	7003 B2	
2037 B6	7004-1 C2	
2038 C7	7004-2 D2	
2039 D8	7010 B8	
2040 E7	7011 C8	
2041 I3	7012 E8	
2042 E3	9005 B2	
2124 I3	F000 F1	
3000 F2	F001 G1	
3002 H10	F002 G11	
3004 G2	F003 G10	
3005 H11	F005 B1	
3006 B11	F006 C1	
3007 B12	F007 D1	
3008 G2	F008 H10	
3010 B13	F009 I10	
3011 B11	F010 F10	
3012 I10	F011 I1	
3014 B12	F012 H7	
3015 F2	F013 I6	
3016 I11	F014 F6	
3017 C11	F015 G6	
3018 F10	F016 B4	
3020 C12	F017 B5	
3021 I2	F018 I4	
3022 C13	F019 C5	
3023 C11	F020 I9	
3024 C12	F021 E5	
3025 G12	F023 I1	
3026 H8	F024 B1	
3027 D11	F025 B9	
3028 G12	F026 B10	
3029 H7	F027 C10	
3030 D12	F029 D10	
3031 E13	I000 G1	
3032 E11	I001 F2	
3033 E12	I002 H1	
3035 I7	I003 G2	
3037 I6	I004 B2	
3038 B2	I005 B2	
3039 F6	I006 C2	
3040 B1	I008 C3	
3042 B2	I009 D2	
3043 B2	I010 D2	
3044 C2	I011 D2	
3045 G6	I012 H12	
3046 C1	I013 I12	
3047 C3	I014 H10	
3048 C2	I015 I10	
3049 D2	I016 F6	

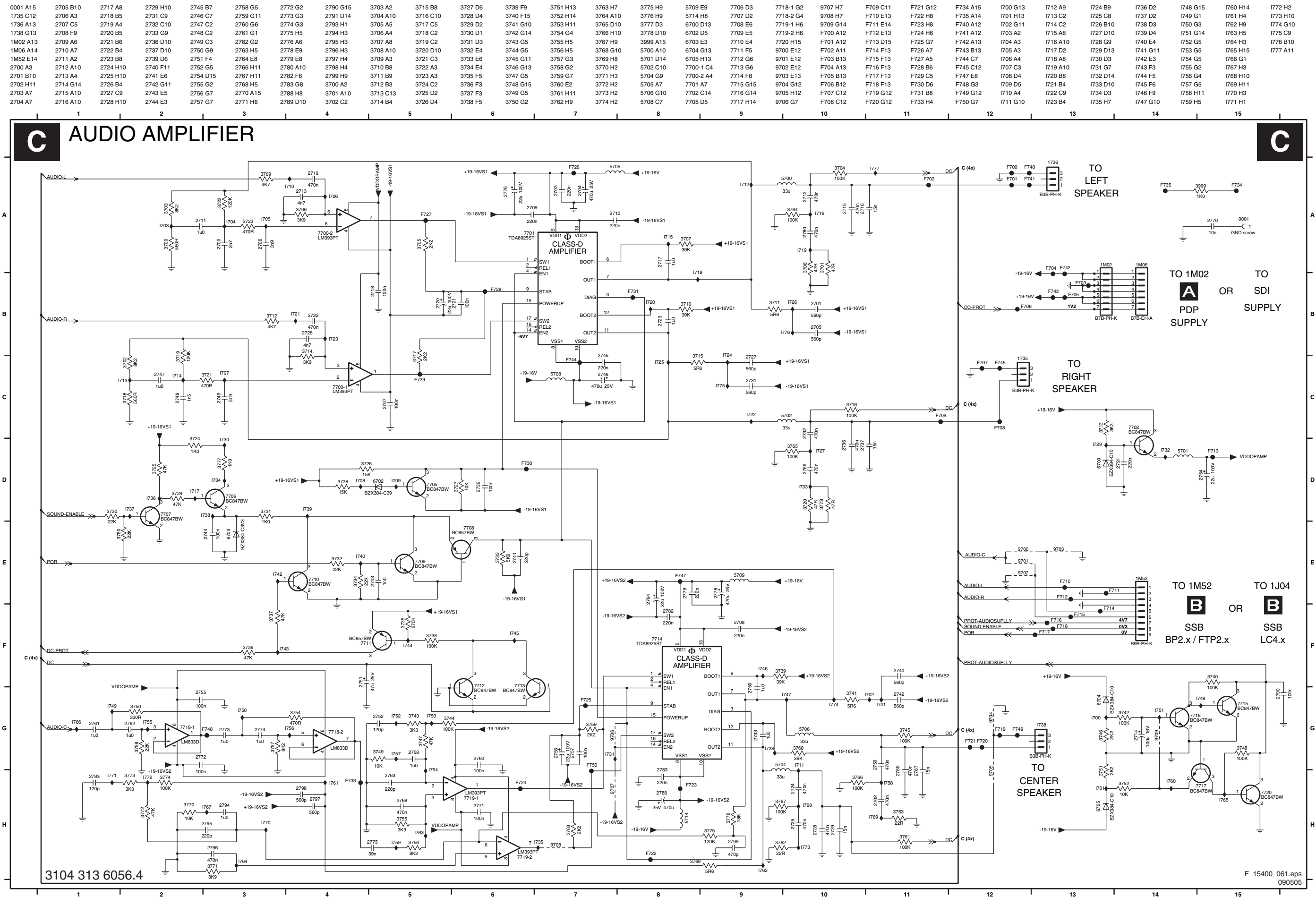
External I/O Panel: Externals B



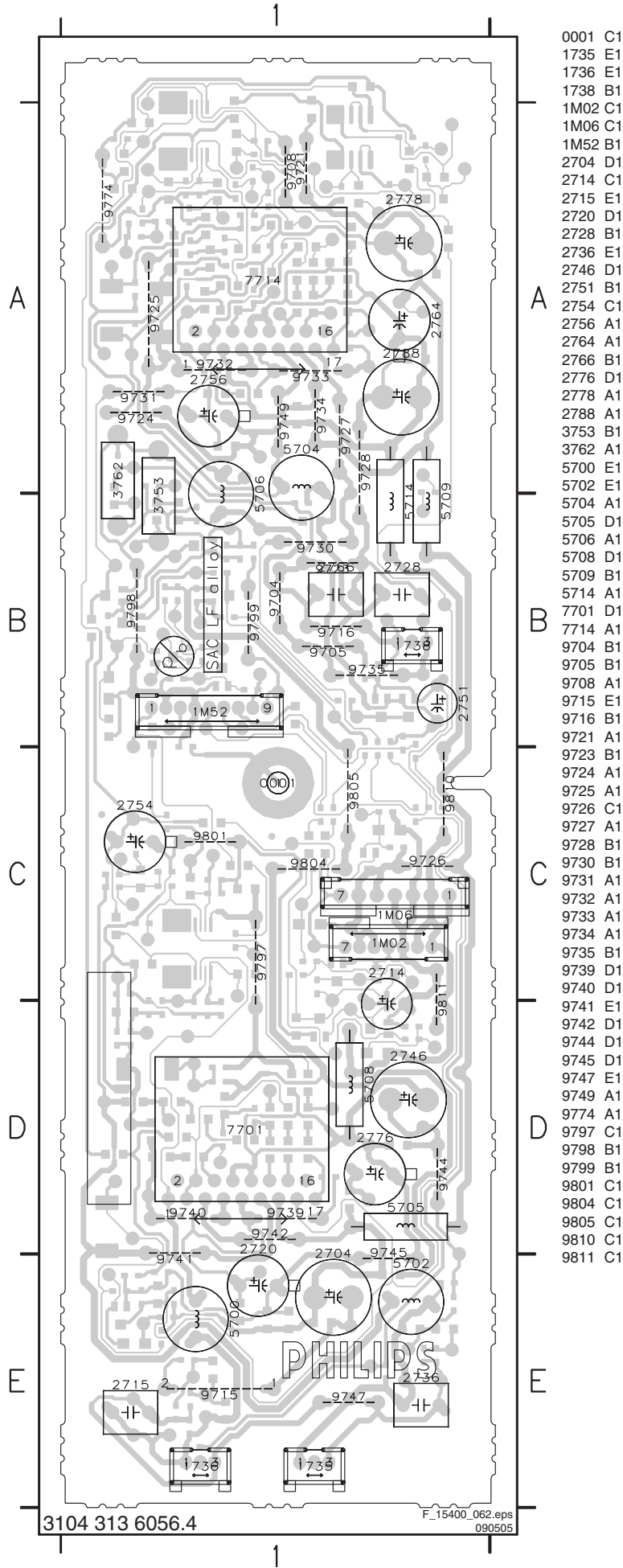
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1101 E8	F112 B3
1102 F8	F113 B3
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1E62 D3	F115 B3
1M20 E3	F117 C3
1M36 B9	F118 C3
1X01 F5	F119 C3
1X02 F6	F120 E2
1X03 F7	F121 F3
1X04 F8	F122 F3
1X05 F8	F124 C3
2124 A6	F125 C3
2125 A6	F126 C3
2126 A7	F127 D3
2127 B6	F128 E8
2128 B7	F133 D3
2129 C6	F134 D3
2130 C7	F136 D3
2131 D7	F137 E3
2132 D6	F138 E3
2133 E2	F139 E2
2134 E2	F140 E2
2135 F2	F141 F9
2136 F3	F142 F9
2137 F3	F143 D3
2138 F2	F144 E8
2139 F2	F145 E8
2140 F2	F146 C3
2141 F2	F147 F2
2247 A9	F148 F2
2248 A8	F149 F2
2249 A8	F150 F2
2250 C9	F151 E3
2251 D8	F152 E3
2252 A8	F153 E3
3153 A6	F154 E3
3154 A6	F155 E3
3156 B6	F156 D3
3157 D6	F157 D3
3158 D6	F158 D3
3159 D7	F159 D3
3160 E6	F200 B8
3161 E6	F201 B8
3999 F9	F203 D8
5100 A6	F204 C8
6100 E6	F205 F9
6101 D9	F214 B8
6102 B6	F217 B7
7106 D7	I100 A6
7107 D6	I101 A7
9100 E1	I102 B6
9101 E1	I103 D6
9104 F3	I104 D7
9105 F3	I105 D7
9106 E1	I108 D8
9107 F1	I109 A6
9108 F1	I110 A6
9109 F1	I111 A6
9110 F1	I120 B5
9205 F9	I121 B6
9210 A9	I122 B6
9211 A9	I123 A9
9212 A9	I124 A9
9213 A9	I125 A9
9220 C9	I126 A9
9221 D9	I213 F9
9222 D3	
F100 A3	
F102 A3	
F103 A3	
F104 A3	
F105 A3	
F106 A3	
F109 B3	

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1040	A2
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1060	D2
1070	B1
1080	C1
1E40	A1
1E62	C1
1M20	A2
1M36	A1
2004	B1
2007	B2
2015	C1
2016	C1
2017	D1
2019	D1
2022	D2
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3158	D2
3159	D2
3160	D2
3161	D2
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7106	D2
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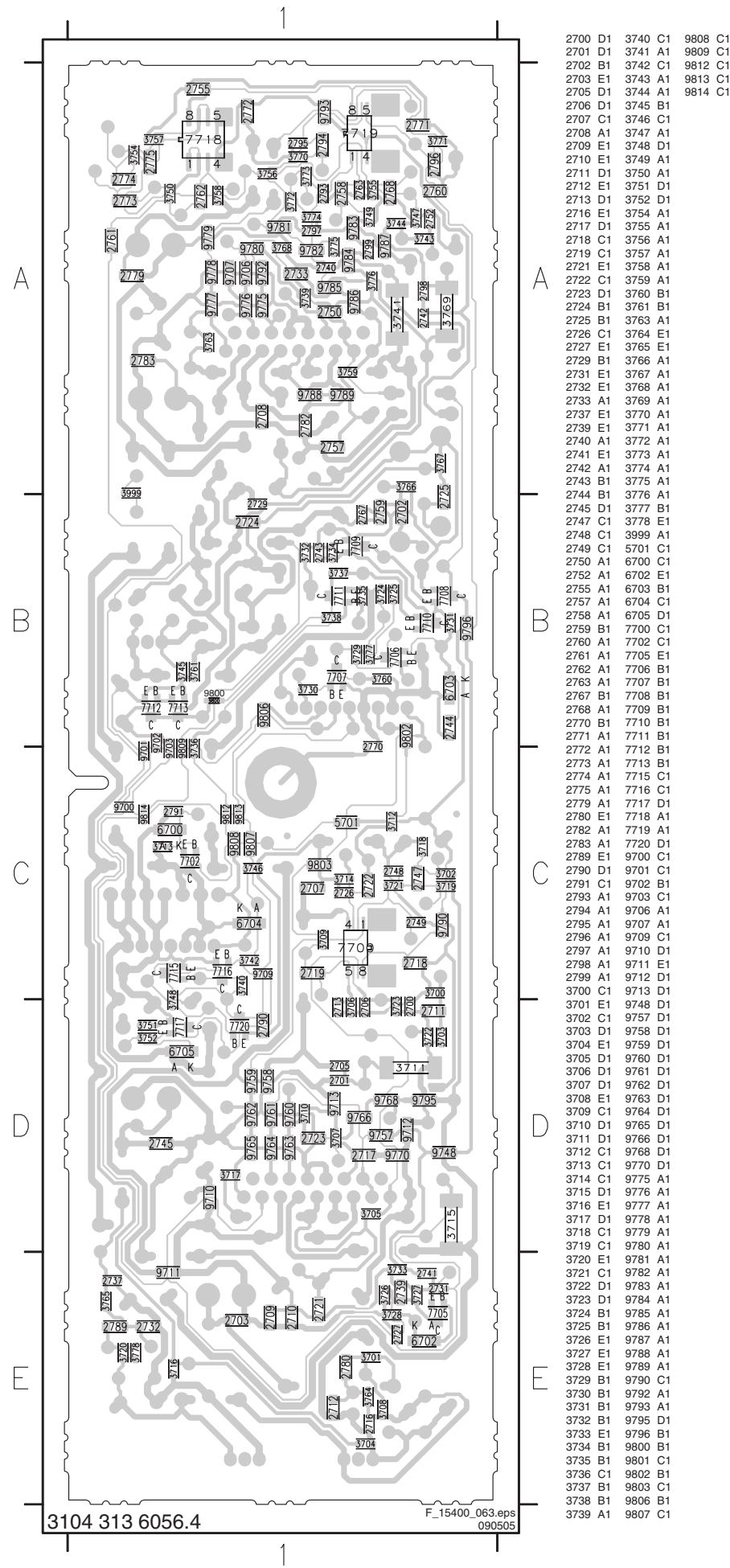
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2020	A2	9109	A1
2021	D2	9110	A1
2023	D1	9205	A2
2030	D2	9211	A2
2037	A1	9212	A2
2039	B1	9213	A2
2041	B1	9220	A2
2042	D2	9221	A2
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2126	A1		
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2248	A2		
2249	A2		
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2251	A2		
2124	B1		
3000	A1		
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3004	A1		
3005	C1		
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3012	C1		
3014	B2		
3015	A1		
3016	C1		
3018	C1		
3021	B1		
3023	C1		
3025	C2		
3026	B2		
3028	C2		
3029	B2		
3032	C1		
3035	B2		
3037	B2		
3038	D1		
3039	A2		
3040	D1		
3042	D1		
3043	D1		
3044	D2		
3045	A2		
3046	D2		
3047	D1		
3048	D2		
3049	D1		
3050	D1		
3051	D2		
3052	D1		
3060	D2		
3061	D2		
3065	B1		
3074	A1		
3075	A1		
3080	B1		
3081	B1		
3082	B1		
3083	B2		
3084	B2		
3153	A1		
3999	B1		
5000	B1		
6000	A1		
6001	C1		
6002	A1		
6003	C1		
6004	C1		
6005	B1		
6006	C1		
6007	B1		
6008	B1		
6009	D1		
6010	C1		
6011	C1		
6012	C2		
6013	B2		
6014	C1		
6015	C1		
6017	B2		
6018	A2		
6019	A2		
6020	D1		
6021	A2		
6022	A2		
6023	D2		
6024	D2		
6025	D1		
6026	D1		
6027	B1		
6029	B1		
6030	B1		
6040	D2		
6041	D2		
6045	A1		
6046	A1		
6047	A1		
6048	A1		

Audio Amplifier Panel

Layout Audio Amplifier Panel (Top Side)



Layout Audio Amplifier Panel (Bottom Side)

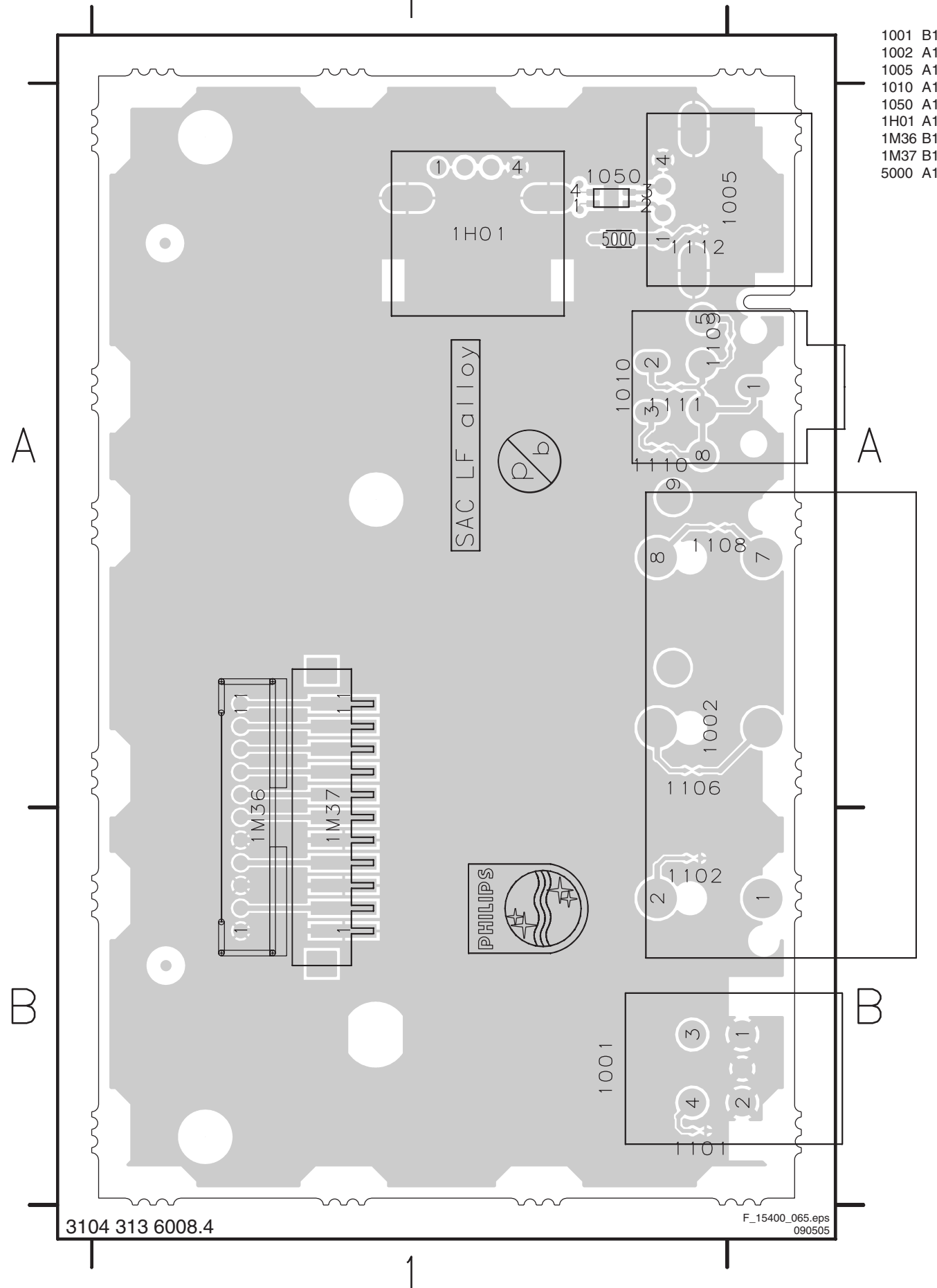


D SIDE I/O

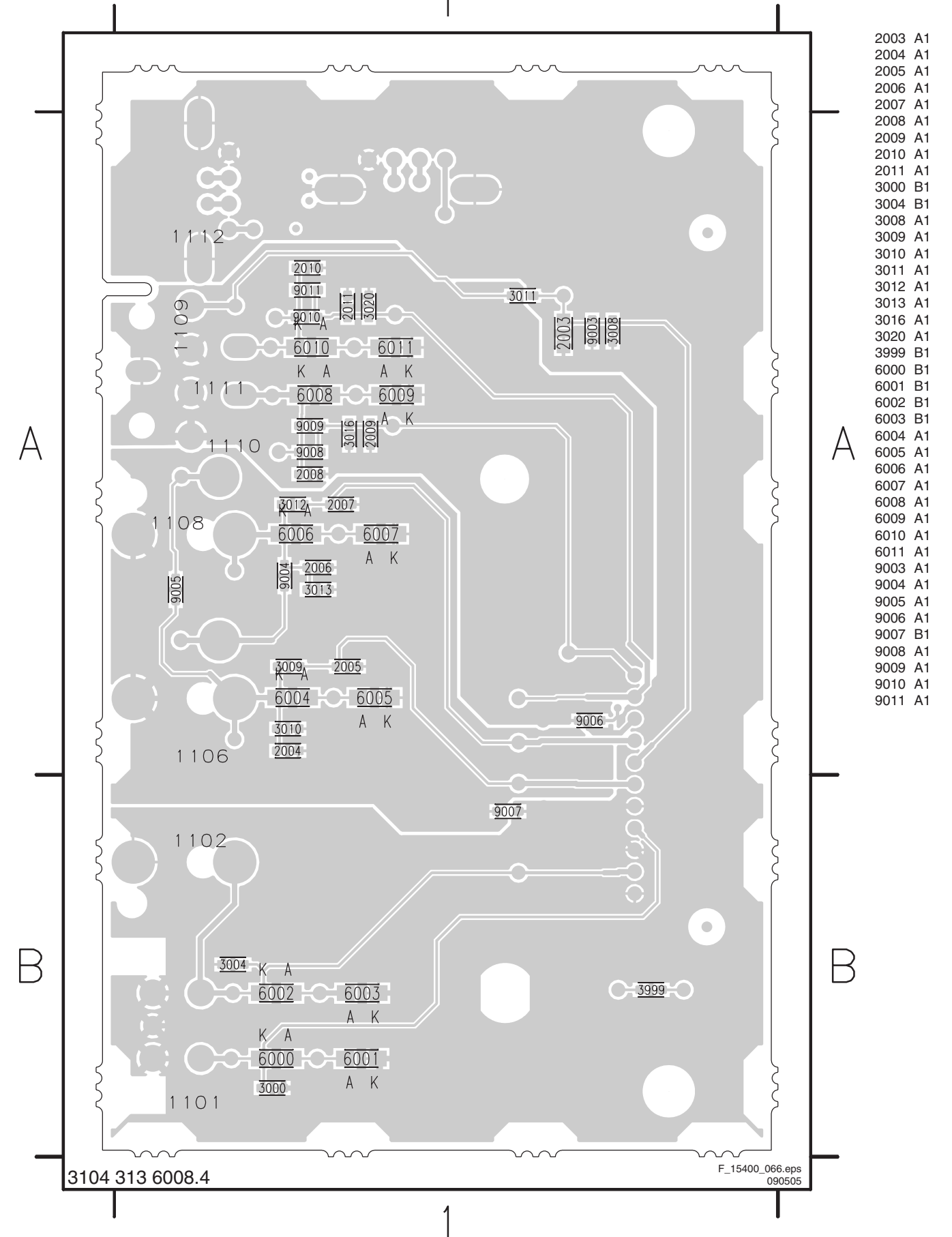


1001 B2	F002 A2
1002-1 B1	F003 B2
1002-2 C1	F004 C2
1002-3 D1	F005 C2
1005 A8	F006 D2
1010 E1	F007 E2
1050 A7	F008 E2
1101 A3	F009 E2
1102 B3	F010 F8
1106 C3	F011 F9
1108 D3	F012 A6
1109 E3	F013 A7
1110 F3	F014 A6
1111 E3	F015 A7
1112 A7	F016 A6
1H01 A6	F017 A7
1M36 B8	F018 F7
1M37 B8	F019 F2
2003 C5	F020 B4
2004 C3	F021 C6
2005 C4	F022 C6
2006 D3	F023 C6
2007 D4	F024 E6
2008 F2	F025 E6
2009 F5	I001 C2
2010 E2	I002 C3
2011 E5	I003 D2
3000 A4	I004 A3
3004 B3	I005 F4
3008 C5	I006 F4
3009 C4	I007 E4
3010 C4	I008 E4
3011 C5	I009 B3
3012 D4	I010 D3
3013 D4	I011 F7
3016 F5	I012 F8
3020 E5	I013 F3
3999 F9	I014 E3
5000 A7	
6000 A3	
6001 A3	
6002 B3	
6003 B3	
6004 C3	
6005 C3	
6006 D3	
6007 D3	
6008 F3	
6009 F3	
6010 E3	
6011 F3	
9003 C6	
9004 C2	
9005 D2	
9006 F7	
9007 F8	
9008 F4	
9009 F4	
9010 E4	
9011 E4	
F001 A2	

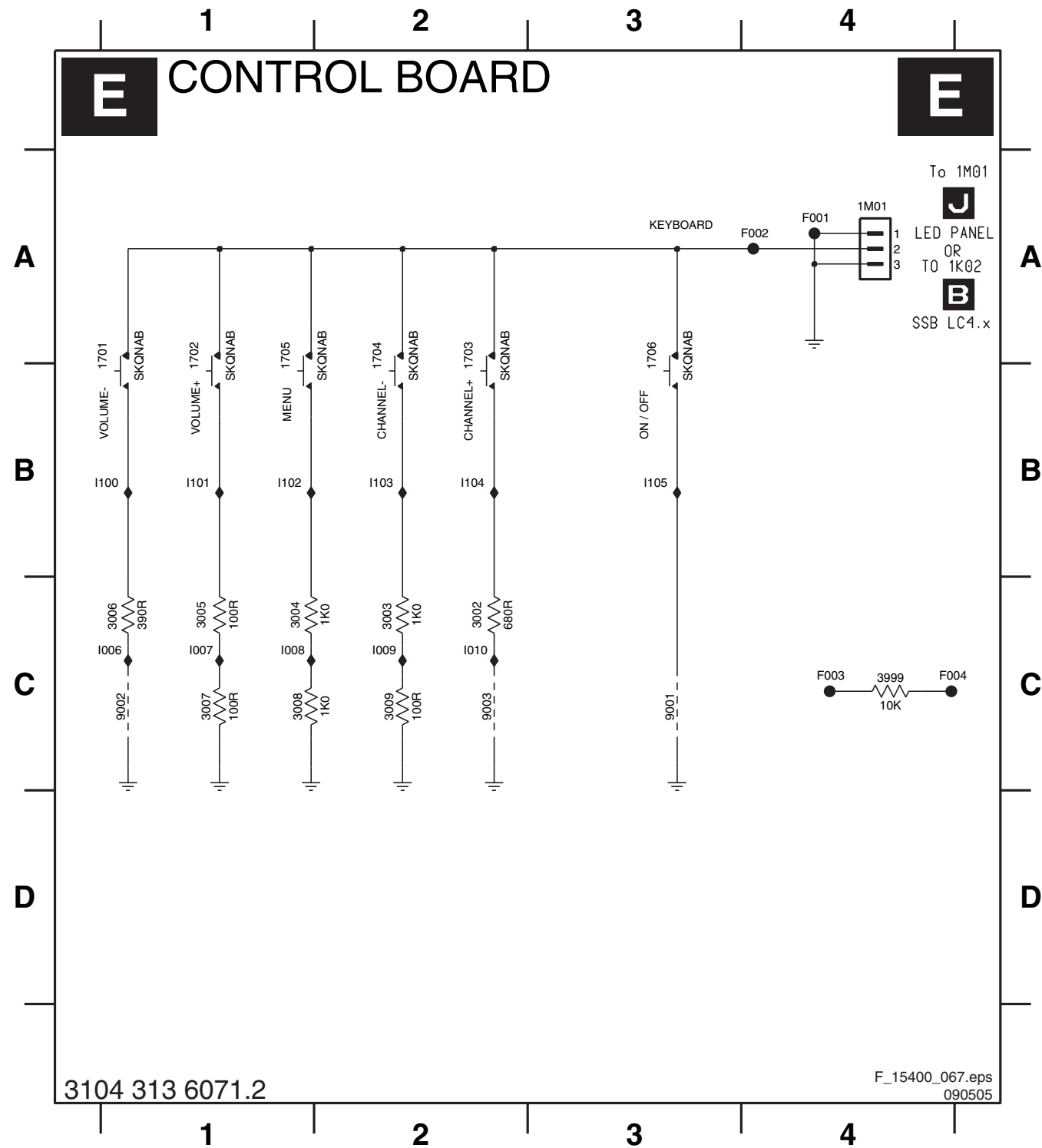
1



1



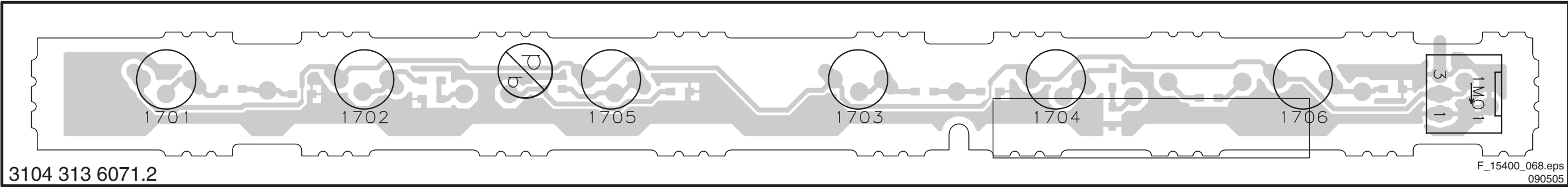
1701 A1	1704 A2	1M01 A4	3004 C1	3007 C1	3999 C4	9003 C2	F003 C4	I007 C1	I010 C2	I102 B1	I105 B3
1702 A1	1705 A1	3002 C2	3005 C1	3008 C1	9001 C3	F001 A4	F004 C4	I008 C1	I100 B1	I103 B2	
1703 A2	1706 A3	3003 C2	3006 C1	3009 C2	9002 C1	F002 A4	I006 C1	I009 C2	I101 B1	I104 B2	



Personal Notes:

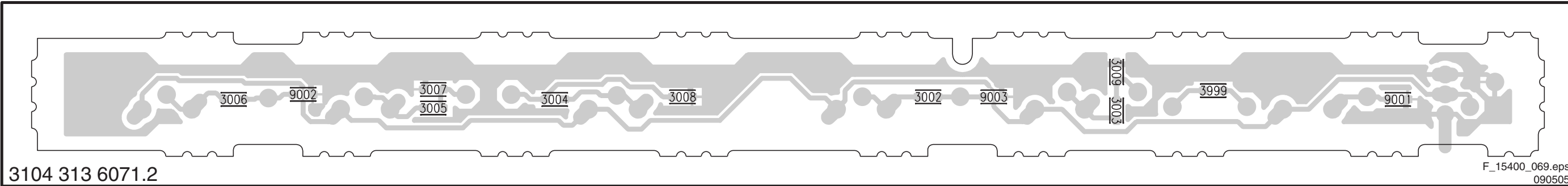
Layout Control Board (Top Side)

1701 -- 1702 -- 1703 -- 1704 -- 1705 -- 1706 -- 1M01 --

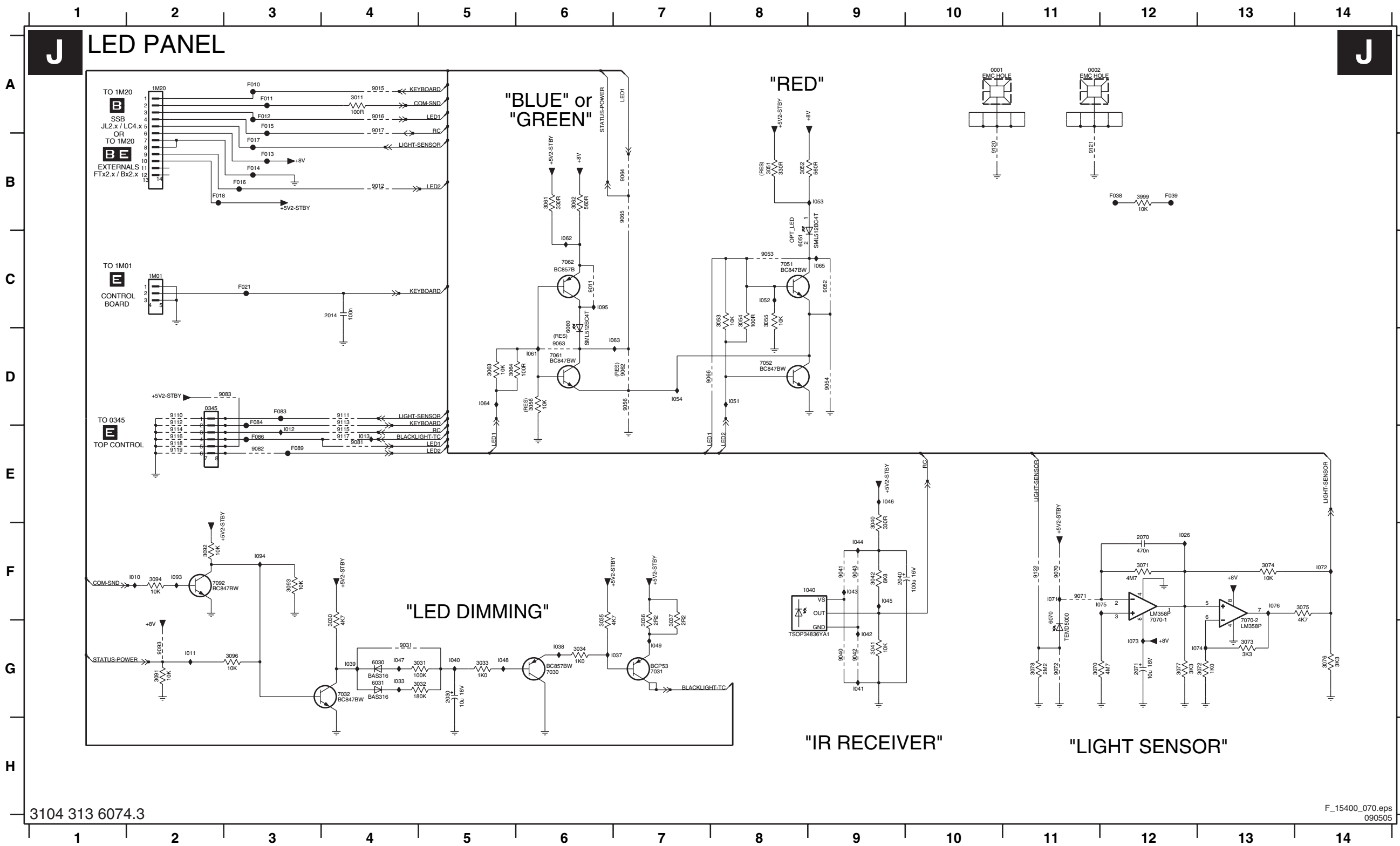


Layout Control Board (Bottom Side)

3002 -- 3003 -- 3004 -- 3005 -- 3006 -- 3007 -- 3008 -- 3009 -- 3999 -- 9001 -- 9002 -- 9003 --



LED Panel



Personal Notes:

This image shows a full page of blank white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. In the bottom right corner, there is small black text that reads "E_06532_012.eps" and "131004".

E_06532_012.eps
131004

8. Alignments

Index of this chapter:

- 8.1 General Alignment Conditions
- 8.2 Hardware Alignments
- 8.3 Software Alignments
- 8.4 Option Settings

8.1 General Alignment Conditions

8.1.1 Start Conditions

Perform all electrical adjustments under the following conditions:

- Power supply voltage: 120 V_{AC} / 60 Hz (± 10%).
 - Connect the set to the AC Power via an isolation transformer with low internal resistance.
 - Allow the set to warm up for approximately 15 minutes.
 - Measure voltages and waveforms in relation to chassis ground (with the exception of the voltages on the primary side of the power supply).
- Caution:** It is not allowed to use heatsinks as ground.
- Test probe: R_i > 10 Mohm, C_i < 20 pF.
 - Use an isolated trimmer/screwdriver to perform alignments.

8.1.2 Initial Settings

Perform all electrical adjustments with the following initial settings (via the "Active Control" button on the RC):

1. To avoid the working of the lightsensor, set ACTIVE CONTROL to OFF.
2. Set SMART PICTURE to NATURAL/ECO.

8.1.3 Alignment Sequence

- First, set the correct options:
 - In SAM, select (SERVICE) OPTIONS -> OPT. NO,
 - Fill in the option settings according to the set sticker (see also paragraph "Option Settings"),
 - Select STORE OPTIONS and push OK on the remote control,
 - After storing, the set must be restarted!
- Warming up (>10 minutes).
- White point alignment.

8.2 Hardware Alignments

Not applicable.

8.3 Software Alignments

Put the set in SAM mode (see the "Service Modes, Error Codes and Fault Finding" section). The SAM menu will now appear on the screen. Select ALIGNMENTS and go to one of the sub menus. The alignments are explained below.

Notes:

- All changes must be stored manually.
- If an empty EARM (permanent memory) is detected, all settings are set to pre-programmed default values.

8.3.1 General

For the next alignments, supply the following test signals via a video generator to the RF input: NTSC M/N TV-signal with a signal strength of at least 1 mV and a frequency of 61.25 MHz (channel 3).

IF AFC

Alignment procedure:

1. During the IF AFC-parameter adjustment, one can see OSD feedback on the screen.
2. The OSD feedback can give four kinds of messages:
3. The first item ("IN/OUT") informs you whether you are in or out of the AFC-window.
4. The second item ("HIGH/LOW") informs you whether the AFC-frequency is too high or too low.

Table 8-1 AFC

AFC-window	AFC-frequency vs. reference
Out	High
In	High
[In]	[Low]
Out	Low

1. Adjust the IF AFC parameter until the **first** value is within the AFC window (= IN).
2. Next, adjust the IF AFC parameter until the **second** value is LOW.

Tuner AGC

Purpose: To keep the tuner output signal constant as the input signal amplitude varies.

Default value: "32".

In case the default value gives problems, use the next method:

1. Set the video generator to a color bar test pattern and a RF amplitude of 1 mV.
2. Select the channel with the test picture.
3. Measure the DC voltage on pin 1 of the (main) Tuner.
4. Adjust this voltage via TUNER AGC to just below 3.5 V.

8.3.2 White Point

- Set ACTIVE CONTROL to OFF.
- In the [MENU] -> PICTURE user menu, set:
 - DYNAMIC CONTRAST to OFF.
 - COLOUR ENHANCEMENT to OFF.
 - COLOUR to "0".
 - CONTRAST to "100".
 - BRIGHTNESS to "50".
- Go to the SAM and select ALIGNMENTS -> WHITE POINT.

Method 1 (with color analyzer):

- Use a 100% white screen as input signal and set the following values:
 - COLOR TEMPERATURE: "Tint to be aligned".
 - All WHITE POINT values to: "127".
 - RED and GREEN BL OFFSET values to: "3".
- Measure with a calibrated (phosphor- independent) color analyzer in the centre of the screen. Consequently, the measurement needs to be done in a dark environment.
- Adjust, by means of decreasing the value of one or two white points, the correct x,y coordinates (see table "White D alignment values"). Tolerance: dx,dy: ± 0.004.
- Repeat this step for the other Color Temperatures that need to be aligned.
- When finished press STORE (in the SAM root menu) to store the aligned values to the NVM.
- Restore the initial picture settings after the alignments.

Table 8-2 White D alignment values

Color Temp.	Cool	Normal	Warm
x	0.276	0.285	0.313
y	0.282	0.293	0.329

When such equipment is not available, use "method 2".

Method 2 (without color analyzer):

If you do not have a color analyzer, you can use the default values. This is the next best solution. The default values are average values coming from production (statistics).

1. Select a COLOUR TEMPERATURE (e.g. COOL, NORMAL, or WARM).
2. Set the RED, GREEN and BLUE default values according to the values in the "Tint settings" table.
3. When finished press STORE (in the SAM root menu) to store the aligned values to the NVM.
4. Restore the initial picture settings after the alignments.

Table 8-3 Tint settings (42"/50")

	Default Values (42"/50")		
	Cool	Normal	Warm
R	110/127	127/127	122/127
G	123/114	114/94	127/107
B	127/125	83/71	121/108

Note: These values were not available at the time of writing, therefore they come from an early production sample (for indication only). As soon as the production data become available, a Service Info or Service Manual update will be issued via the appropriate channels.

8.4 Option Settings

8.4.1 Introduction

The microprocessor communicates with a large number of I²C ICs in the set. To ensure good communication and to make digital diagnosis possible, the microprocessor has to know which ICs to address. The presence / absence of these specific ICs (or functions) is made known by the option codes.

Notes:

- After changing the option(s), save them with the STORE command.
- The new option setting is only active after the TV is switched "off" and "on" again with the Mains switch (the EAROM is then read again).

8.4.2 Dealer Options**Table 8-4 Dealer options**

Menu item	Subjects	Options	Description
Personal Options	Picture Mute	On	Picture mute active in case no picture detected
		Off	Noise in case of no picture detected
	Virgin Mode	On	TV starts up (once) with a language selection menu after the Mains switch is turned "on" for the first time (virgin mode)
		Off	TV does not start up (once) with a language selection menu after the Mains switch is turned "on" for the first time (virgin mode)

8.4.3 (Service) Options

Select the sub menu's to set the initialization codes (options) of the set via text menus.

Table 8-5 Service options

Menu-item	Subjects	Options	Description
PIP/DS	Dual Screen	None / 1 tuner / 2 tuners	no DS / DS with one tuner / DS with two tuners
Data	TV Guide US	On / Off	Feature present / not present
Display	Screen	"Value"	Used screen size, type, and resolution
	Scanning Backlight	On / Off	Feature present / not present
	Dimming Backlight	On / Off	Feature present / not present
Video Repro	Picture Processing	Spider / No Spider	Feature present / not present
	Combfilter	None / 2D / 3D	Only selectable when Columbus is present
	Ambient Light	None / Mono / Stereo	Inverter not present / one inverter / two inverters
	MOP	On / Off	Feature present / not present (for sets with AmbiLight this is "on")
Source Selection	HDMI 1	None / Audio / No Audio	No HDMI / HDMI with analog audio / HDMI without analog audio
	HDMI 2	None / Audio / No Audio	No HDMI / HDMI with analog audio / HDMI without analog audio
	USB version	None / 1.1 / 2.0 + CR	No USB / USB 1.1 in side I/O panel / USB 2.0 in cardreader panel
	IEEE1394	Yes / No	Connector present / not present
	Ethernet	Yes / No	Connector present / not present
	S/PDIF inputs	None / 1 conn. / 2 conn.	None / 1 connector present (in)/ 2 connectors present (in/out)
Audio Repro	Subw. Internal Present	Yes / No	Internal sub woofer present / not present
	Acoustic System (Cabinet design, used for setting dynamic audio parameters).	None	n.a.
		Entry ME5 5W	n.a.
		Entry ME5 15W	42/50PF7320A
		(Soft) Wrap	n.a.
		Top	n.a.
		Entry+	42/50PF9630A, 50PF9830A
		Others	n.a.
Miscellaneous	Alternative Tuner	Philips / Alps	Tuner brand
	Tuner Type	TD1336S	Tuner type
Opt. no.	Group 1		xxxxx xxxxx xxxxx xxxxx (see set sticker)
	Group 2		xxxxx xxxxx xxxxx xxxxx (see set sticker)

8.4.4 Opt. No. (Option numbers)

Select this sub menu to set all options at once (expressed in two long strings of numbers).

An option number (or "option byte") represents a number of different options. When you change these numbers directly, you can set all options very quickly. All options are controlled via eight option numbers.

When the EARAM is replaced, all options will require resetting. To be certain that the factory settings are reproduced exactly, you must set both option number lines. You can find the correct option numbers on a sticker inside the TV set.

Example: The options sticker gives the following option numbers:

- 04368 00005 01066 08707
- 00000 00032 00512 00000

The first line (group 1) indicates hardware options 1 to 4, the second line (group 2) indicates software options 5 to 8. Every 5-digit number represents 16 bits (so the maximum value will be 65536 if all options are set). When all the correct options are set, the sum of the decimal values of each Option Byte (OB) will give the option number. See next table for the option overview.

Table 8-6 Option code overview

Byte	Bit (dec. value)	Subject	Options	Settings (in decimal values)	Remarks
1	0 (1)	Video Repro	Picture Processing	0= No Spider, 1= Spider	Spider availability, influences, digital options.
	1 (2)				
	2 (4)				
	3 (8)		Comb Filter	0= None, 8= 2D Comb (Columbus without DRAM), 16= 3D Comb (Columbus with DRAM)	
	4 (16)				
	5 (32)		Ambient Light	0= None, 32=Ambi-light Stereo, 64= Ambi-light Mono	
	6 (64)				
	7 (128)		Dual Screen	0= None, 256= One Tuner DS, 512= Two Tuner DS	
	8 (256)				
	9 (512)		MOP	0= Off, 1024= On	Matrix Output Processor (or EBILD)
	10 (1024)				
	11 (2048)		JOP	0= Off, 2048= On	Jaguar Output Processor (or EBILD) Reserved for future use
	12 (4096)		POD	0= Off, 4096= On	
	13 (8192)		n.a.		
	14 (16384)		n.a.		
	15 (32768)		n.a.		
2	0 (1)	Sound Repro	Acoustic System (Cabinet)	0= None, 1= Entry_ME5_5W, 2= Entry_ME5_15W, 3= (Soft)Wrap, 4= Top, 5= Entry+, 15= Others	Cabinet design, used for setting dynamic audio parameters.
	1 (2)				
	2 (4)				
	3 (8)		Aux Headphone Sound	0= Off, 16= On	Dual AC3 sound in Aux available.
	4 (16)				
	5 (32)		n.a.		
	6 (64)		n.a.		
	7 (128)		n.a.		
	8 (256)		n.a.		
	9 (512)		Sub woofer Internal	0= Not Present, 512= Present	
	10 (1024)		Centre Mode Support	0= Not Supported, 1024= Supported	
	11 (2048)		n.a.		
	12 (4096)		n.a.		
	13 (8192)		n.a.		
	14 (16384)		n.a.		
	15 (32768)		n.a.		
3	0 (1)	Source Select	HDMI1	0= None, 1= With analog audio, 2= Without analog audio	
	1 (2)		HDMI2	0= None, 4= With analog audio, 8= Without analog audio	
	2 (4)				
	3 (8)		n.a.		
	4 (16)				
	5 (32)		USB Version	0= None, 32= USB 1.1, 64= USB 2.0 + Card reader	USB support.
	6 (64)		IEEE1394	0= Not Present, 128= Present	
	7 (128)				
	8 (256)		Ethernet	0= LAN not present, 256= LAN present	
	9 (512)		n.a.		
	10 (1024)		S/PDIF Inputs	0= None, 1024= 1 Connector, 2048= 2 Connectors	
	11 (2048)		LCOS I/O	0= Not Present, 4096= Present	
	12 (4096)				
	13 (8192)		n.a.		
	14 (16384)		n.a.		
	15 (32768)		n.a.		
4	0 (1)	Region	Region	0= EU, 1= AP-P, 2= AP-N, 3= US, 4= Latam	
	1 (2)				
	2 (4)				
	3 (8)	Interconnect	China IF	0= Off, 8= On	
	4 (16)		Alternative Tuner	0= Philips, 16= Alps	Tuner make.
	5 (32)		Tuner Type	0= TD1336s (B-Chassis US), 32= TD1331(J-Chassis US), 64= UV1318 (Analogue EU), 96= TD1316 (Hybrid EU)	Tuner type (B-chassis US is e.g "BP2.3U").
	6 (64)				
	7 (128)	Source Select	n.a.		
	8 (256)		AV1	0= CVBS/RGB, 256= CVBS/YC/LR, 512= CVBS/YC/YPbPr/HV/LR	Input type.
	9 (512)		AV2	0= CVBS/YC/RGB/P50, 1024= CVBS/YC/LR	Input type.
	10 (1024)				
	11 (2048)		AV3	0= Not Available, 4096= CVBS, 8192= YPbPr	Input type.
	12 (4096)				
	13 (8192)		AV4	0= Not Available, 16384= YPbPr	Input type.
	14 (16384)				
	15 (32768)				

Byte	Bit (dec. value)	Subject	Options	Settings (in decimal values)	Remarks
5	0 (1)	Display	Screen	000 (0000)= 42-inch PDP (SDI) HD V3, 001 (0256)= 50-inch PDP (SDI) HD V3, 002 (0512)= 42-inch PDP (FHP) ALiS, 003 (0768)= 30-inch LCD (LPL), 004 (1024)= 37-inch LCD (LPL), 005 (1280)= 42-inch LCD (LPL), 006 (1536)= 32-inch LCD (Sharp), 007 (1792)= 42-inch PDP (SDI) SD, 008 (2048)= 37-inch PDP (FHP) ALiS, 009 (2304)= Reserved, 010 (2560)= 30-inch LCD (AUO), 011 (2816)= 32-inch LCD (LPL), 012 (3072)= 32-inch LCD (AUO), 013 (3328)= 37-inch LCD (Sharp), 014 (3584)= 42-inch LCD (LPL) HD, 015 (3840)= 37-inch PDP (SDI) SD, 016 (4096)= 37-inch PDP (FHP) ALiS, 017 (4352)= 42-inch PDP (FHP) ALiS, 018 (4608)= 55-inch PDP (FHP), 019 (4864)= Reserved, 020 (5120)= Reserved, 021 (5376)= 26-inch LCD (LPL), 022 (5632)= 32-inch LCD (LPL) scan. BL, 023 (5888)= 42-inch PDP (LG) SD, 024 (6144)= 42-inch PDP (SDI) SD V4, 025 (6144)= 42-inch PDP (SDI) HD V4, 026 (6400)= 42-inch PDP (FHP) HD A2, 027 (6656)= 50-inch PDP (SDI) HD V4, 028 (6912)= 37-inch LCD (Sharp) HD	Screen size, type, and resolution.
	1 (2)				
	2 (4)				
	3 (8)				
	4 (16)				
	5 (32)				
	6 (64)				
	7 (128)				
	8 (256)		n.a.		
	9 (512)		n.a.		
	10 (1024)		Dimming Backlight	0= Off, 1024= On	
	11 (2048)		Scanning Backlight	0= Off, 2048= On	
	12 (4096)		n.a.		
	13 (8192)		n.a.		
	14 (16384)		n.a.		
	15 (32768)		n.a.		
6	0 (1)	Miscellaneous	Monitor	0= Off, 2= On	Reserved for future use
	1 (2)		n.a.		
	2 (4)		Stand Alone	0= Off, 4= On	Reserved for future use
	3 (8)		n.a.		
	4 (16)		n.a.		
	5 (32)		n.a.		
	6 (64)		Proximity Sensor	0= Off, 64= On	
	7 (128)		n.a.		
	8 (256)		Touch Pad	0= Off, 256= On	Reserved for future use
	9 (512)		n.a.		
	10 (1024)		n.a.		
	11 (2048)		n.a.		
	12 (4096)		n.a.		
	13 (8192)		n.a.		
	14 (16384)		n.a.		
	15 (32768)		n.a.		
7	0 (1)	Personal	Self Learning TV	0= Off, 1= On	Reserved for future use
	1 (2)		Auto Store Mode	0= None, 2= PDC/VPS, 4= TXT Page, 6= PDC/VPS/TXT Page	Fixed to: "None" in the AP-N and US versions.
	2 (4)				
	3 (8)		2CS Korea	0= Off, 8= On, 16= Auto	
	4 (16)				
	5 (32)		Picture Mute	0= Off, 32= On	
	6 (64)		n.a.		
	7 (128)		Virgin Mode	0= Off, 128= On	
	8 (256)		Hotel Mode	0= Off, 256= On	
	9 (512)		Content Browser	0= Not Present, 512= Present	
	10 (1024)		Connected Planet	0= Off, 1024= Full Connected Planet + logo support	
	11 (2048)		n.a.		
	12 (4096)				
	13 (8192)		EPG	0= None, 8192= TXT Guide only, 16384= NextView 2C3, 24576 = NexTVView 2	
	14 (16384)				
	15 (32768)		TV Guide USA (Gemstar)	0= Off, 32768= On	
8	0 (1)	n.a.	n.a.		
	1 (2)	n.a.	n.a.		
	2 (4)	n.a.	n.a.		
	3 (8)	n.a.	n.a.		
	4 (16)	n.a.	n.a.		
	5 (32)	n.a.	n.a.		
	6 (64)	n.a.	n.a.		
	7 (128)	n.a.	n.a.		
	8 (256)	n.a.	n.a.		
	9 (512)	n.a.	n.a.		
	10 (1024)	n.a.	n.a.		
	11 (2048)	n.a.	n.a.		
	12 (4096)	n.a.	n.a.		
	13 (8192)	n.a.	n.a.		
	14 (16384)	n.a.	n.a.		
	15 (32768)	n.a.	n.a.		

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

- 9.1 Introduction
- 9.2 Power Supply
- 9.3 Inputs
- 9.4 Front-End
- 9.5 POD (Point Of Deployment)
- 9.6 MPIF (PNX 3000)
- 9.7 PNX2015
- 9.8 PNX2015: AVIP
- 9.9 PNX2015: Columbus (Comb Filter)
- 9.10 PNX2015: HD Subsystem
- 9.11 PNX2015: LVDS Transmitter
- 9.12 PNX2015: Stand-by Processor
- 9.13 VIPER 2 (PNX 8550)
- 9.14 MOP
- 9.15 Ambient Light (if present)
- 9.16 Abbreviation List
- 9.17 IC Data Sheets

Notes:

- Only **new** circuits (circuits that are not published recently) are described.
- Figures can deviate slightly from the actual situation, due to different set executions.
- For a good understanding of the following circuit descriptions, please use the wiring, block (chapter 6) and circuit diagrams (chapter 7). Where necessary, you will find a separate drawing for clarification.

9.1 Introduction

The BP2.x is a new TV chassis, specifically developed for ATSC reception. The key components are:

- POD circuitry.
- MPIF (PNX3000).
- AVIP/COLUMBUS (PNX2015).
- VIPER 2 (PNX8550).

9.1.1 Features

Table 9-1 Main chassis features

Feature	BP2.1 (Top)	BP2.2 (Step)	BP2.3 (Entry)
AmbiLight	Stereo	Mono	None
USB	2 x USB2.0	2 x USB2.0	1 x USB1.1
Card reader	Yes	Yes	No
ROM / RAM	64 / 128 MB	32 / 64 MB	32 / 64 MB
MOP (EPLD)	Yes	Yes	No
PixelPlus	2 HD	2 HD	1

The main features for this chassis are (see also table):

- The move from the analog world to the digital world. W.o.w. from signal processing via "hardware circuits" to signal processing via "software algorithms". This means: no software = no picture and sound!
- Fit for both analog and digital signal processing, this by converting analog signals into digital transport streams and allowing seamless zapping between all possible signal sources. This makes the chassis applicable for e.g. receiving ATSC in an integrated product form.
- AmbiLight (BP2.1, 2.2): To be able to control lamps at the rear of the TV with respect to the measured ambient light level from the light sensor or the picture content, a control output from AutoTV has been foreseen.
- The internal digital processing allows new "Multi-Media" applications such as Content Browser, Memory Card Slot, Local Area Network support (future) and all kinds of streaming applications (future).

- The chassis can be upgraded in the future with internal functionality such as Personal Video Recording, DVD/RW.

9.1.2 Chassis Block Diagram

Description below refers to the block diagrams in chapter 6 "Block Diagrams, Test Point Overview, and Waveforms".

Analog Reception

The TV receives multimedia information by tuning to one of many 6 MHz input channels available via a cable connection. When the input channel is an analog channel, the signal is processed via the NTSC decoder and the VBI data decoder.

Digital Reception

As depicted in the block diagram, the POD module consists of the following functional blocks: POD Common Interface, Out of Band part, and buffering. These blocks are interfacing with the ATSC In Band (IB) channel decoder and Out of Band (OOB) channel decoder. The interface is connected to the VIPER. Also the POD Interface outgoing Transport Stream (TS) is routed to the VIPER.

The TV receives multimedia information by tuning to one of many 6 MHz input channels available via a cable connection. When the input channel is a digital channel, it is processed via the QAM demodulator and then passed to the CableCARD device (POD) where secure and scrambled information is processed. Non-scrambled information is passed through the CableCARD Device to the MPEG-2 Transport Demultiplexer. When the CableCARD Device is not inserted, the output of the QAM demodulator is routed directly to the MPEG-2 Transport Demultiplexer. The multi-media processor (VIPER) handles the synchronization and display of audio-visual material.

The OpenCable Host Device also receives control information and other data by tuning to an Out-Of-Band (OOB) Forward Data Channel (FDC) channel. The terminal will remain tuned to the OOB Forward Data Channel (own tuner) to continuously receive information. This information is passed to the CableCARD Device for processing, and relevant information is passed back to the TV.

Signal Processing

The AVIP together with the MPIF device is used to perform the input decoding of a single stream of analog audio and video broadcast signals. In addition, the AVIP is used for decoding and presentation of audio output streams. The main data connection between MPIF and AVIP is done via an I²D bus. The AVIP converts the incoming video data to ITU-656 format for communication to the VIPER IC.

The audio data is transferred between the AVIP and VIPER using I²S.

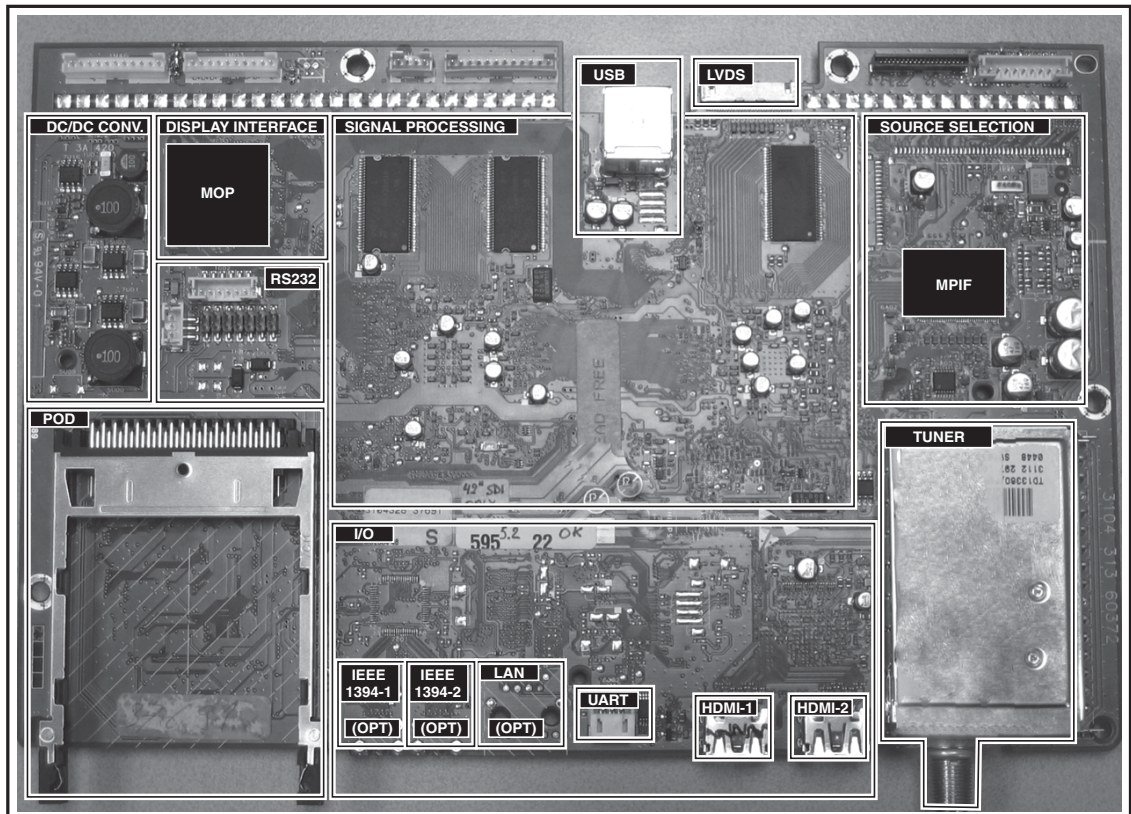
The AVIP IC is controlled by the VIPER via the I²C bus.

The key part in the system, the VIPER, performs almost all key features, like video quality enhancement, motion compensation, picture-in-picture processing, and others. It is a completely digital IC with a TriMedia DSP (Digital Signal Processor) core and a MIPS microcontroller core. The DSP and some additional cores are used to do the video feature processing and some auxiliary sound feature processing. The MIPS microcontroller core is used for all internal and external controlling tasks including a system wide I²C bus.

The VIPER provides a primary digital (YUV or RGB) output to the LVDS transmitter. For models with the AmbiLight feature, an EPLD is connected between VIPER output and LVDS

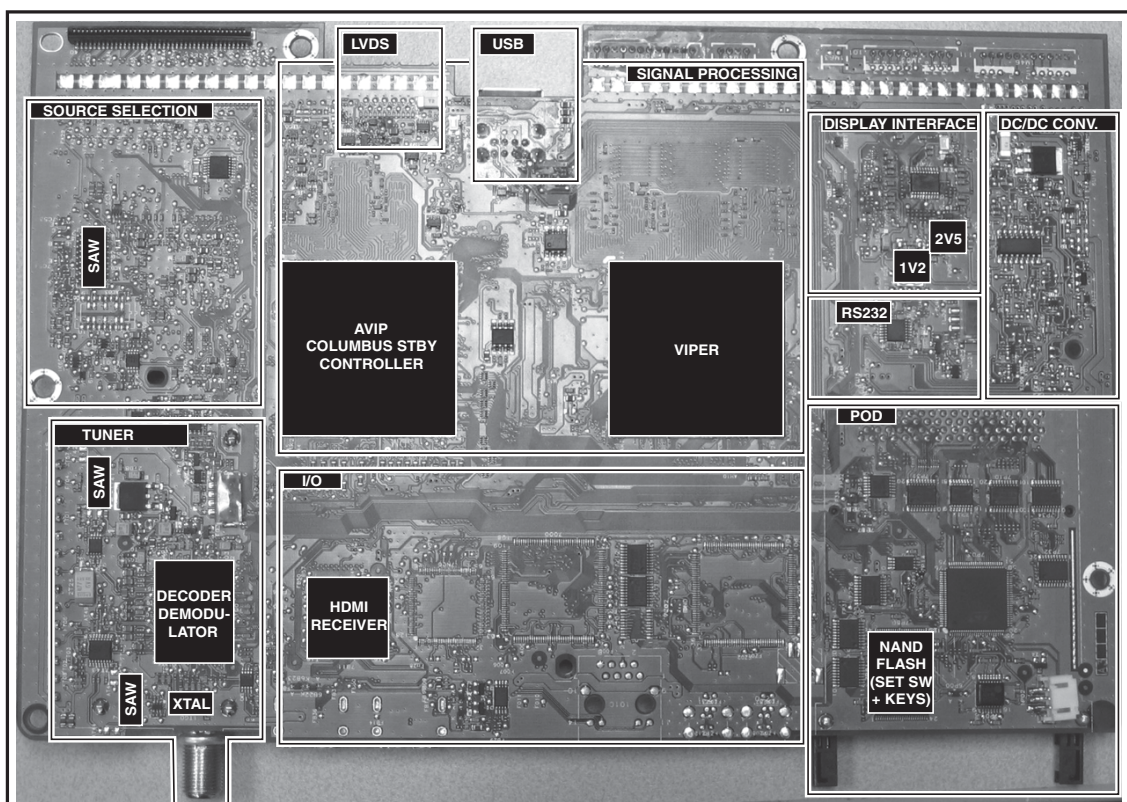
Transmitter input. This EPLD (or MOP) is used for the AmbiLight processing and some picture enhancements.

SSB Cell Layout



F_15400_009.eps
210405

Figure 9-1 SSB top view



F_15400_010.eps
300505

Figure 9-2 SSB bottom view

9.2 Power Supply

9.2.1 Introduction

The Main Power Supply is a buy-in module (it belongs to the PDP), and therefore is a "black box" for Service. When defective, a new panel must be ordered and after receipt, the defective panel must be send for repair.

This Power Supply delivers the following supply voltages to the chassis:

- +12VS.
- +8V6.
- +5V2.
- +5V.

As the VIPER and many other ICs on the SSB require low supply voltages at high current (up to 3 A for the main voltages), onboard DC/DC converters are implemented.

The circuit on the SSP provides the 3.3 and 1.2 voltages.

A DC/DC converter has the following advantages:

- The DC/DC converter is directly on the SSB near the circuits that needs to be powered.
- Some circuits on the SSB need high current by low voltage, so there is no risk to have power dips or voltage loss in connections between the PSU and the SSB panel.

9.2.2 Block Diagram

See also diagrams B1A and B1B.

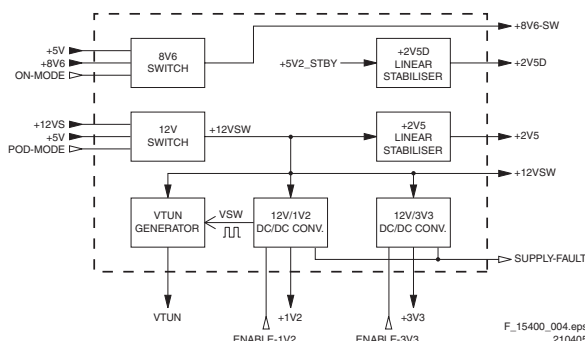


Figure 9-3 DC/DC converter block diagram

9.2.3 PSU Start-up Sequence

1. If the input voltage of the DC/DC converters is around 12 V (measured on the decoupling capacitors 2U17/2U25/2U45) and the ENABLE signals are "low" (active), then the output voltages should have their normal values.
2. First, the Stand-by Processor activates the +1V2 supply (via ENABLE-1V2).
3. Then, after this voltage becomes present and is detected OK (about 100 ms), the other two voltages (+2V5 and +3V3) will be activated (via ENABLE-3V3).
4. The current consumption of controller IC 7U00 is around 20 mA (that means around 200 mV drop voltage across resistor 3U22).

9.2.4 +2V5D Linear Stabilizer

- Provides the +2V5D voltage, and is derived from the +5V2-STBY voltage coming from the Main Power Supply.
- The output current is limited to a few tenths of mA.
- Output over-voltage protection is done by zener diode 6U17.

9.2.5 +12V Switch

- The +12V switch is activated when the POD-MODE signal is "low".
- The rise time of the output voltage is set by components 2U42, 3U43, and 3U95 at about 30 ms.
- The switch "off" is fast, because there can be fault currents that must be interrupted.
- When the input voltage (+12VS) is higher than 15 V, the switch is disabled via circuit 6U12, 3U52, 3U53, 2U71, and 7U14-2.

9.2.6 Internal Protection

- Provides a SUPPLY-FAULT signal (active "low"), when the output voltage of any DC/DC converter is out of its limits ($\pm 10\%$ of the normal value). In such cases, the Stand-by Processor will immediately stop the supplies by sending a "high" control signal towards the external and internal supplies: ENABLE-xVx, POD-MODE, ON-MODE, and STAND-BY.

Note: The SUPPLY-FAULT control signal is "low" when any DC/DC converter is disabled by its control signal (ENABLE-xVx) and +12VSW is present, therefore it is ignored during start-up!

- The internal protection works together with the output over-voltage detector transistors 7U15-1, 7U15-2, 7U29-1, and 7U29-2.

9.2.7 1.2V and 3.3V DC/DC Converters

Introduction

The circuit used is a so-called "synchronous buck converter". Some characteristics:

- Switching frequency: approx. 250 kHz.
- Efficiency: approx. 90%.
- Built-in output over-voltage and over-current protections
- Soft start.
- Software controlled "on/off" (via ENABLE line).

Block Diagram

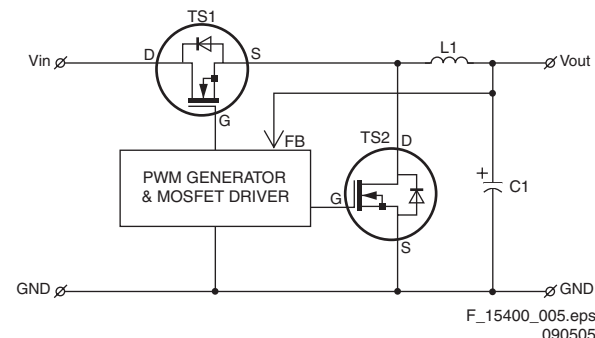


Figure 9-4 Block diagram synchronous buck converter.

The advantage of a "synchronous buck converter" over a "classical buck converter" is its better efficiency (about 90%). The difference between the two is that in a synchronous buck converter the "low -side" diode is replaced by a MOSFET TS2 (item 7U03). This, because the voltage drop across a MOSFET is smaller than the forward voltage drop of a diode.

This second MOSFET TS2 conducts current during the "off" times of the first MOSFET TS1 (item 7U01 at the input side). The upper MOSFET TS1 conducts, to transfer energy from the input to the inductor L_1 and load R_L , while the lower MOSFET TS2 conducts to circulate the inductor current (free wheel). The synchronous PWM control block regulates the output voltage by modulating the conduction intervals of the upper and lower MOSFETs.

PWM Generator and MOSFET Drivers

This circuit is a one-chip solution (item 7U00). It contains all the circuitry for two independent buck regulators (3V3 and 1V2). The MOSFETs T7U01 and T7U03 are the switching transistors, they are conducting alternatively.

- Time sequence 1: T7U01 is conducting; energy is stored in coil 5U00/5U03. The current is flowing from the +12VSW power supply source.
- Time sequence 2: T7U01 is blocked; energy is stored in coil 5U00/5U03.
- Time sequence 3: T7U03 is conducting, and the current circuit is now closed via T7U03, Coil 5U00/5U03, C2U24/2U22, and the load. So the energy stored in the coil during time sequence T1 is consumed during sequence T3. The signal on the gate T7U03 is 180 degrees turned compared with the signal on the gate T7U01.

Voltage Booster

This circuit is build around capacitors 2U11 and 2U26, resistor 3U11, diodes 6U22 and 6U23, and transistor 7U07. It generates the +18 V boost voltage on pin 4 of item 7U00, to drive the "high-side" power MOS-FET 7U01. The voltage is generated only during normal operation of the converter; therefore, any drop in its value means an internal fault condition, which is sensed by the internal protection circuit. The AC component of the voltage on the source of transistor 7U01 is rectified by the diodes and added to the input voltage, resulting into the boost voltage. The resistor 3U11 limits the peak current through the rectifier diodes.

Over-current Detection

Over-current detection is done via components 3U07, 3U08, 3U82, 3U83, and 2U18 for the 3.3 V converter and 3U09, 3U10, 3U96, 3U97, and 2U12 for the 1.2 V converter.

Under-voltage Detection

There is an additional circuit (7U10 and 7U11) to switch "off" the 3.3 V converter in case the +12VS drops below 9 V.

Service Tips

- When a power MOS-FET is found defective, replace the other power MOS-FET and fuse 1U01 as well.
- For a normal operation of the converter, it is important to check the switching frequency, the value of the boost voltage, and the amplitude of the gate voltage of transistor 7U04 (it should be close to the boost voltage).

9.2.10 Useful Data

Voltage Name	Value [V]	Tolerance [%]
+5V2	5.2	5
+5V	5.1	5
+8V6	8.6	5
+12VS	12	5
+VTUN	33	5
+1V2	1.26	3
+2V5	2.6	4
+2V5D	2.6 (2.5) *	4 (5) *
+3V3	3.3	5
+5V2S	5.1	5
+8V6-SW	8.6	5
+12VSW	12	5

*) ON mode (STAND-BY mode)

9.2.8 V_{TUN} Generator

The +VTUN supply voltage (value 31...35 V at 4 mA) for the analog tuner(s) is generated by a boost converter. It uses the incoming +12 V_{DC} and the pulses have a duty cycle of about 10% from those of the 1.2 V DC/DC converter.

9.2.9 8V6 Switch

- Provides the +8V6-SW supply voltage from the incoming +8V6.
- It is activated by the ON-MODE signal, which is active "low". This is needed to switch "off" the +8V6-SW in POD Stand-by mode, to lower the power consumption.
Note: It is not active if the +5V voltage is not present.

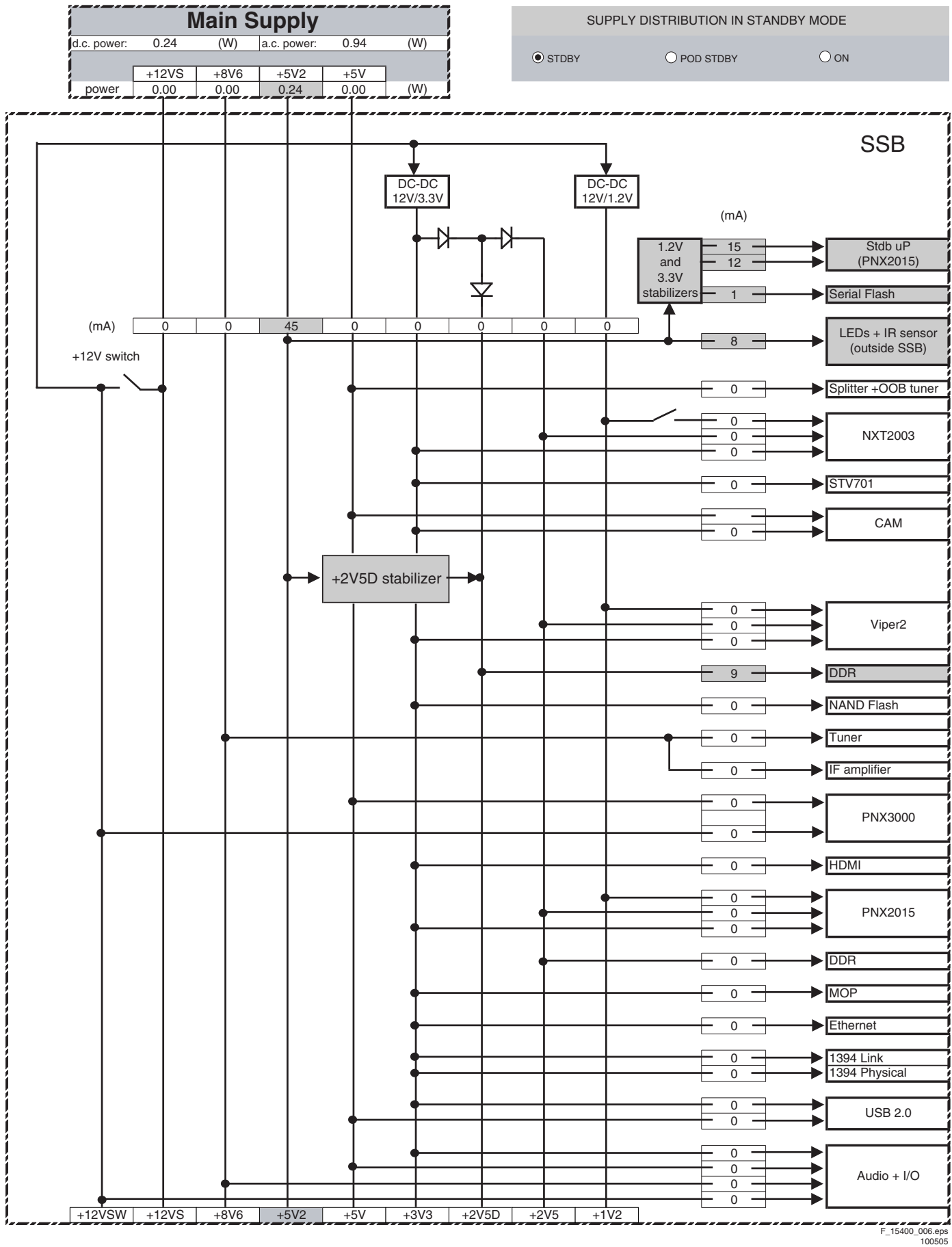


Figure 9-5 Supply distribution: STANDBY Mode (mentioned values are indicative)

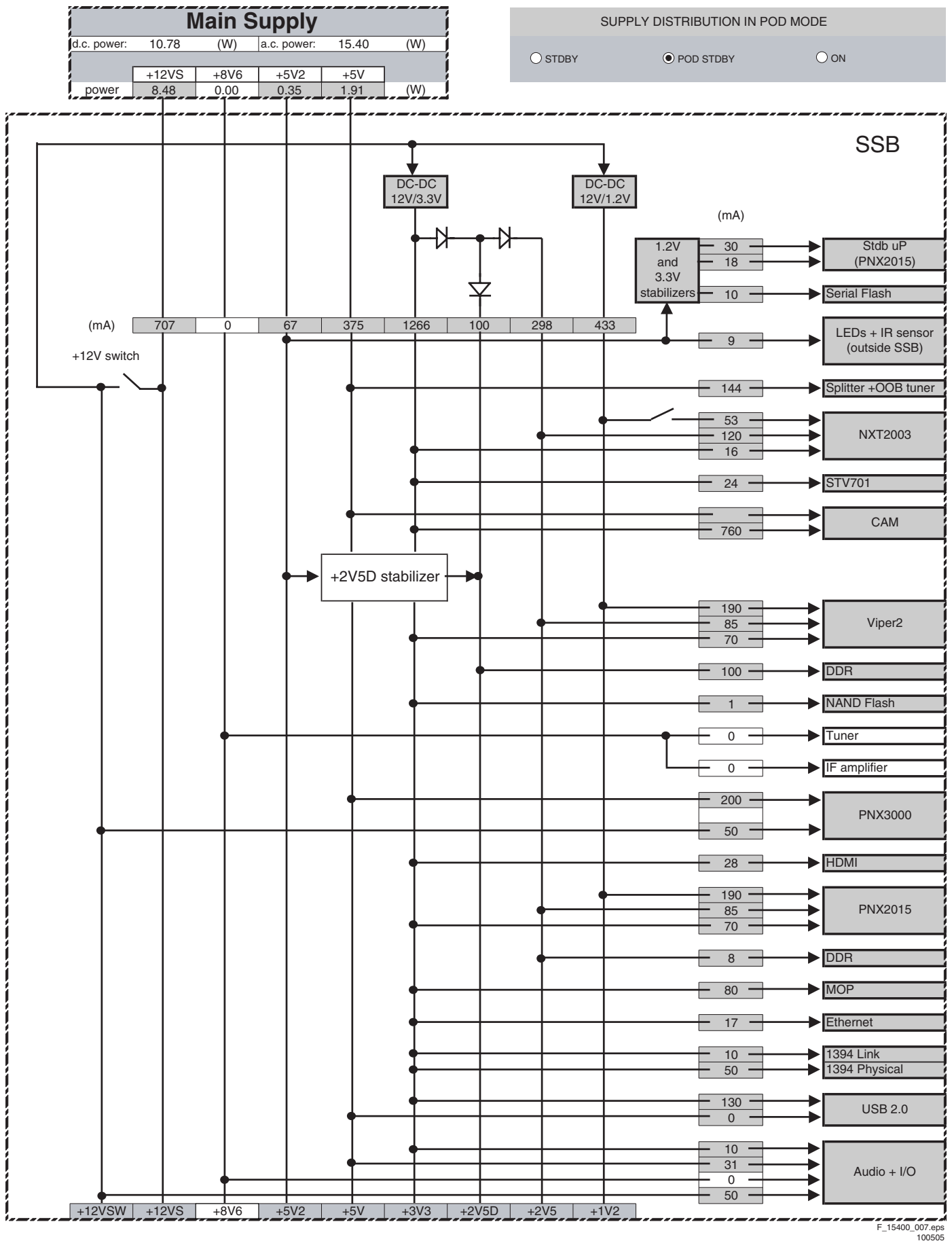


Figure 9-6 Supply distribution: POD STDBY Mode (mentioned values are indicative)

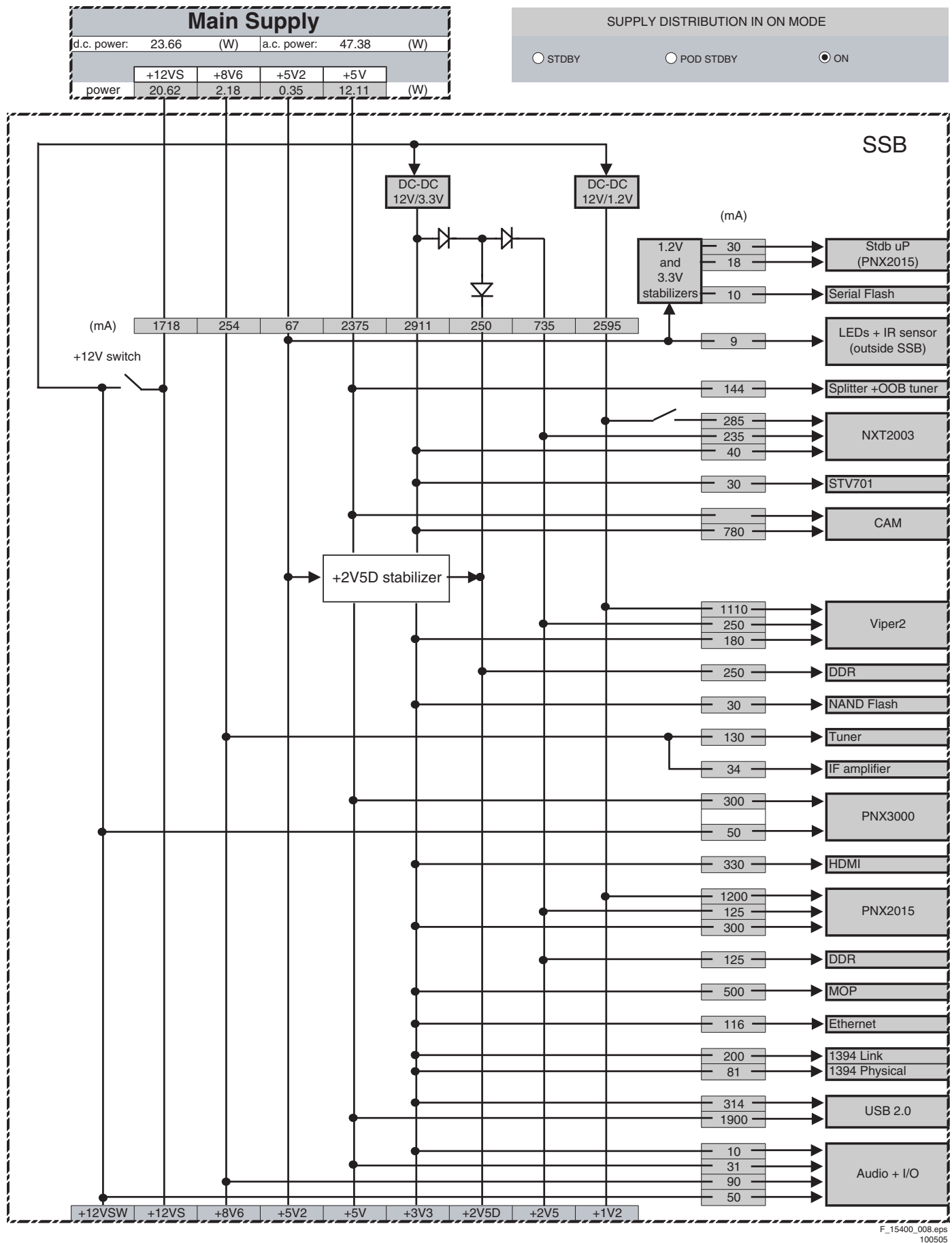


Figure 9-7 Supply distribution: ON Mode (mentioned values are indicative)

9.3 Inputs

9.3.1 USB

These chassis have different USB specifications:

- Chassis BP2.2 features USB2.0. This USB version is hosted by a separate IC (7N00) which communicates with the VIPER via a PCI bus.
- Chassis BP2.3 features USB1.1. This USB version is hosted directly by the VIPER.

Each USB port has four lines:

- 5V (red).
- D- (white).
- D+ (green).
- GND (black).

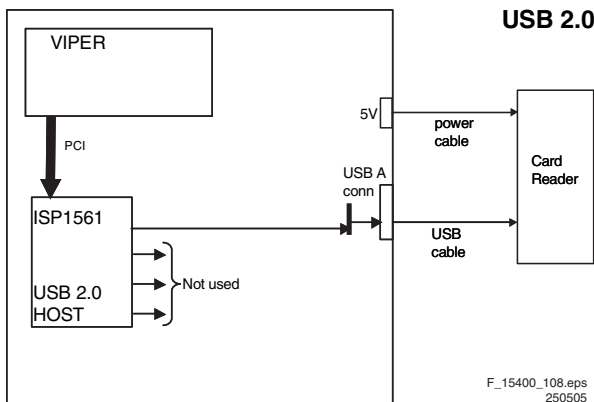
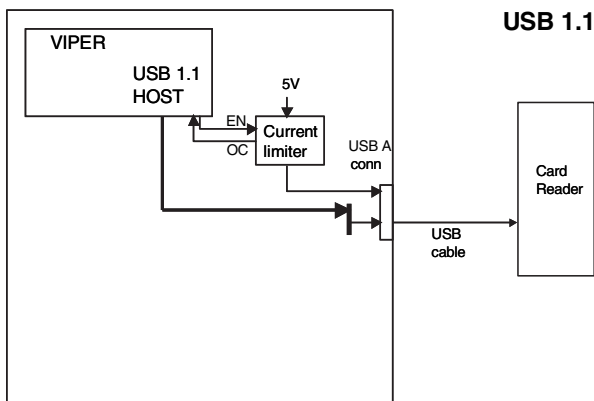


Figure 9-8 USB configurations

USB1.1

The USB1.1 is a hardware block in the VIPER. There are two USB ports. Each port has a D+ and D- line; this is the differential signal path for USB. There is also one over-current detect and power enable line that is used for both ports (these lines are controlled by VIPER).

A tandem USB connector is mounted on the SSB, on which you can connect two USB devices; one device will be the SCM digital media card-reader. Only USB mass storage class device is supported, so other USB devices (card-readers) have to be compliant with this class.

The host (= SSB) needs to provide the power supply to the attached devices (like memory cards or other USB devices). Since it is not known what the customer will attach (e.g. a USB hub with multiple USB devices), and these USB devices draw current from the SSB, these supply lines must be protected against over-current and/or too many connected devices. This is controlled by the VIPER via the USB_OVERCUR line (see diagram B5A): when more than 500 mA per channel is

drawn from the USB ports, the protection becomes active (= "high").

During stand-by, when there is no +5V available (and VIPER is not active), the USB port does not work. This is controlled by the VIPER via the USB_BUS_PW line (see diagram B5A), which switches the 5V input to the outputs of IC7Q01.

USB2.0

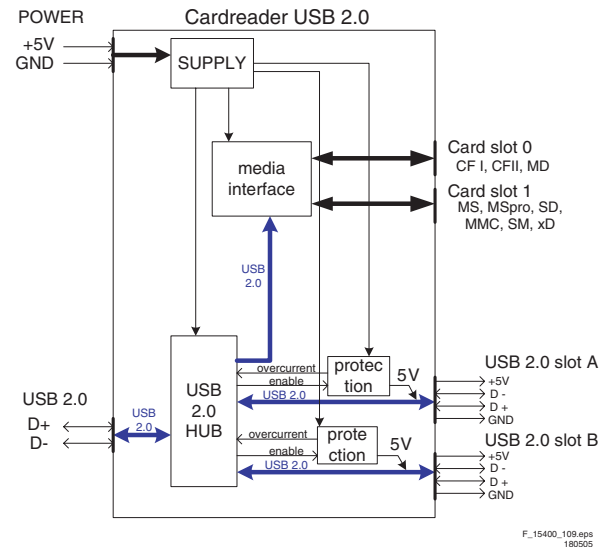


Figure 9-9 Multimedia card reader Assy

9.3.2 HDMI

Introduction

Note: Text below is an excerpt from the "HDMI Specification" that is issued by the HDMI founders (see <http://www.hdmi.org>).

This High-Definition Multimedia Interface is developed for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. HDMI can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats. Content protection technology is available. HDMI can also carry control and status information in both directions.

As shown in the HDMI block diagram, the HDMI connector carries four differential pairs that make up the TMDS (Transition Minimized Differential Signalling) data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC channel. The DDC is used for configuration and status exchange between a single source device and a single sink device.

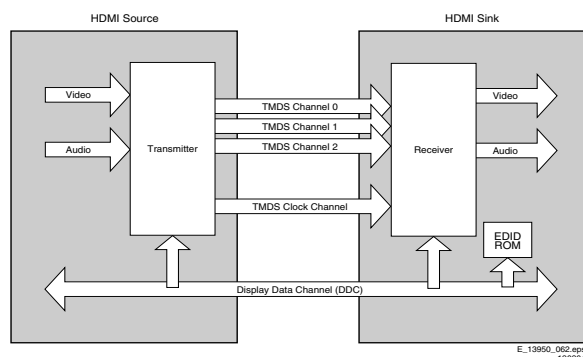


Figure 9-10 HDMI block diagram

Audio, video, and auxiliary data is transmitted across the three TMDs data channels. The video pixel clock is transmitted on the TMDs clock channel and is used by the receiver as a frequency reference for data recovery on the three TMDs data channels.

Video data is carried as a series of 24-bit pixels on the three TMDs data channels. TMDs encoding, converts the 8 bits per channel into the 10 bit DC-balanced transition minimized sequence, which is then transmitted serially across the pair at a rate of 10 bits per pixel clock period.

Video pixel rates can range from 25 MHz to 165 MHz. Video formats with rates below 25 MHz (e.g. 13.5 MHz for 480i/NTSC) can be transmitted using a pixel-repetition scheme. The video pixels can be encoded in either RGB, $YCbCr$ 4:4:4, or $YCbCr$ 4:2:2 formats. In all three cases, up to 24 bits per pixel can be transferred.

In order to transmit audio and auxiliary data across the TMDs channels, HDMI uses a packet structure. In order to attain the higher reliability required of audio and control data, this data is protected with a BCH error correction code and is encoded using a special error reduction coding to produce the 10-bit word that is transmitted.

Basic audio functionality consists of a single IEC 60958 audio stream at sample rates of 32 kHz, 44.1 kHz, or 48 kHz. This can accommodate any normal stereo stream. Optionally, HDMI can carry a single such stream at sample rates up to 192 kHz or from two to four such streams (3 to 8 audio channels) at sample rates up to 96 kHz. HDMI can also carry IEC 61937 compressed (e.g. surround-sound) stream at sample rates up to 192 kHz.

The DDC is used by the source to read the sink's Enhanced Extended Display Identification Data (E-EDID) in order to discover the sink's configuration and/or capabilities.

HDMI is backward compatible with DVI (1.0). Compared with DVI, HDMI offers extra:

- YUV 4:4:4 (3 x 8-bit) or 4:2:2 (up to 2 x 12-bit), where DVI offers only RGB 4:4:4 (3 x 8 bit).
- Digital audio in CD quality (16-bit, 32/44.1/48 kHz), higher quality available (8 channels, 192 kHz).
- Remote control via CEC bus (Consumer Electronics Control): allows user to control all HDMI devices with the TV's remote control and menus.
- Smaller connector (SCART successor).
- Less cables: e.g. from 10 audio/9 video cables to 3 HDMI cables.

Implementation

The IC used is the TDA9975 (triple 10-bit video converter interface), item 7B11 on the SSB.

- Power supply: 3V3 and 1V8.
- Inputs:

- HDMI connectors (Video, Audio, HDCP, Control).
- Analogue (YPbPr, RGB, and H/V).
- Control signals:
 - I²C coming from TDA9975 (MM-BUS1).
 - 13.5 MHz clock for analog format detection.
 - JTAG.
- Output to PNX2015: Video (DV4 and DV5):
 - YUV 4:2:2 20 bit (10 bit Y, 10 bit UV multiplexed) + clock + sync.
 - ITU-656 (compressed DVD video) encoded in data stream.
- Output to VIPER:
 - Audio: S/PDIF.
 - Interrupt signal.

Data Content

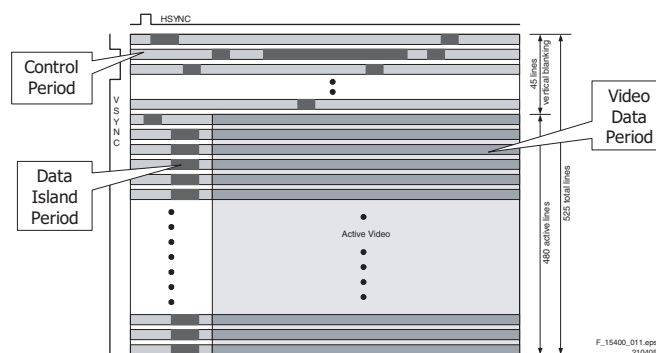


Figure 9-11 Typical video frame

A typical video frame is built up with the following info blocks:

- Control Period.
 - Transmission of the pre-amble.
 - Character synchronization.
- Data Island Period.
 - Audio and auxiliary information are carried in packets within a Data Island.
 - HSYNC, VSYNC are also carried during Data Island Period.
 - Packet Types:
 - Audio Sample.
 - Audio Clock Recovery.
 - InfoFrame: Aux. Video IF, Audio IF, MPEG IF, vendor-defined IF.
- Video Data Period.
 - Carries the pixels of an active video line.
 - TMDs encoding.

Data Islands: Audio Formats

- All current CE audio formats can be transmitted.
- Supports compressed formats like:
 - Dolby Digital.
 - Dolby Digital EX (THX-EX).
 - DTS.
 - Etc.
- Supports uncompressed formats ("discrete" PCM audio):
 - Up to 8 channels, up to 192 kHz, up to 24 bits.
- CD-quality audio is always available, so the user will always hear sound.
 - 2 channel, 16 bit at 32 kHz (STB), 44.1kHz (CD), or 48 kHz (DVD)

Data Islands: InfoFrames (EIA/CEA-861B)

- Auxiliary Video Information (AVI):
 - Specifies active aspect ratio, colorimetric info, pixel encoding, etc.
- Audio InfoFrame:
 - Describes audio stream, speaker/channel allocation, etc.
- Source Product Info:

- Contains manufacturer name, product name, type, etc. (replaced by CEC).
- MPEG Source:
 - Contains flags that permit optimized display of de-compressed video.
- Vendor unique info.

Content Protection: HDCP

- HDCP (High-bandwidth Digital Content Protection) for HDMI encrypts and protects video, audio, and other auxiliary data.
- If a source device is HDCP coded and is connected to a HDTV display or projector via DVI/HDMI without the proper HDCP decoding mechanism, the picture is relegated to "snow" or in some cases, a very low (480p) resolution. In order to see HDTV with HDCP compliance, both the source and display devices must be equipped with DVI/HDMI connections that can enable HDCP using "software key" decoding.
- HDCP requires that decoding takes place in the display device (no external converters).

CEC Bus (Consumer Electronics Control)

- This is the successor of the P50 protocol.
- It allows the user to control all HDMI devices with the TV's remote control and menus.
- High-level functions such as "One-touch play".
- Optional for device to implement protocol.
- Mandatory to implement wire pass-through.

9.4 Front-End

See description in paragraph "Introduction" -> "Chassis Block Diagram".

9.5 POD (Point Of Deployment)

9.5.1 Introduction

This chassis is provided with a special slot called CableCARD™. This means that it is not necessary to have a separate Set Top Box to receive digital cable SDTV and HDTV programs (however this is still possible). The CableCARD (or POD) is a removable card distributed by cable companies, which is inserted into the slot at the bottom of the television. It allows you to tune digital and high definition scrambled or encrypted cable channels through the cable antenna. The CableCARD is also required to receive premium digital TV channels and services (where available) through the cable. A CableCARD functionality includes conditional access and copy protection.

9.5.2 Implementation

1. The receiver receives the digital data stream.
2. The data flows into the Conditional Access Module, which contains the content provider's unscrambling algorithms.
3. This module verifies the existence of a smart card (POD) that contains the subscriber's authorization code.
4. If the authorization code is accepted, the CAM unscrambles the data and returns the data to the receiver (if the code is not accepted, the data remains scrambled, restricting access).
5. The receiver then decodes the data and outputs it for viewing.

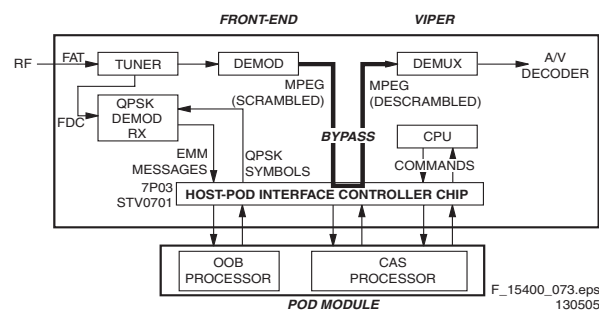


Figure 9-12 In Band channel reception (without POD inserted)

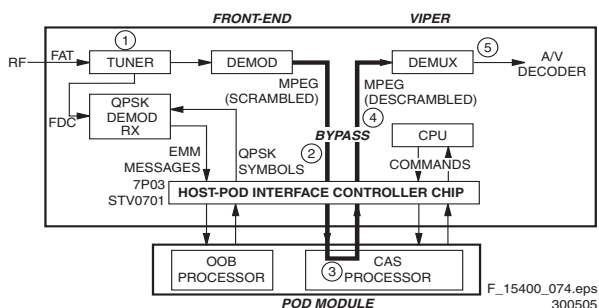


Figure 9-13 In Band channel reception (with POD inserted)

POD Working Principle

The POD is a removable CAM, implementing the CA system for a Host (i.e. the TV set). The POD module is inserted into a standard PCMCIA slot in the Host.

When the POD is inserted into the Host, it goes through an initialization procedure, which is called the "POD personality change". This initialization procedure consists of:

- POD and Host verify each other's identity by means of certificate and/or key exchange.
- Reporting POD-ID and Host-ID to the Cable Head end, in order to entitle the POD for descrambling services. In case of uni-directional operation (as for this chassis), this reporting requires user-interaction.
- Key generation for secure communication between POD and Host.

After initialization, the POD is used to unscramble any particular scrambled service in the In Band (IB) transport stream. The host must provide the selection choice (which program to descramble). The host can only do so if it gets specific data like PSIP (Program and System Information Protocol) data from the POD.

The POD implements a copy protection system, so the unscrambled Transport Stream signal from POD to Host can be re-scrambled.

Copy Protection (CP)

- Every TV-set has its own unique Host-certificate (with Host-ID). These certificates are stored on a dedicated PC at the TV supplier.
- The CP-key is refreshed at the following times:
 - At the end of the authentication process.
 - Periodically at a rate set by max_key_session_period.
 - At every power cycle.
 - When initiated by the CA System.
 - At every hard reset.
 - At power-up, the POD checks the Auth-key to see if the host is still the same, after this the re-authentication takes place.
 - During CP-refresh is the transport stream in the clear (<1s)

POD Stand-by Mode

- POD stack still alive:
 - Active Front-End.
 - Active VIPER, Stby-uP.
- Allows the POD to request services:
 - Listen to OOB.
 - Firmware upgrade.

Connector

- Mechanical
 - 68 pins PCMCIA connector.
 - Voltage keying (LV type).
 - Type I, II, III.
- Hot plug ability
 - Initial, V_{CC} is applied to the socket.
 - Card detection (CD1 & CD2 = low).
 - Voltage sense pins (VS1 & VS2).
 - Power controller to set V_{CC} and V_{PP} .
- CIS structure
 - All PCMCIA cards have a CIS structure.
 - Information about size, speed, functions, ...
 - Distinguish between PC-card and Cable-card.
 - Before reading the CIS, the PCMCIA driver is in an 8-bit memory card mode with reduced address- and control lines (only purpose is to read the CIS).
 - After reading the CIS, there is a personality change and the driver is ready to communicate with a Cable-card.
 - Once a card's client driver successfully parses the CIS and obtains the system resources required by the card, it assigns the resources to the card via the COR (Configuration Option Register).

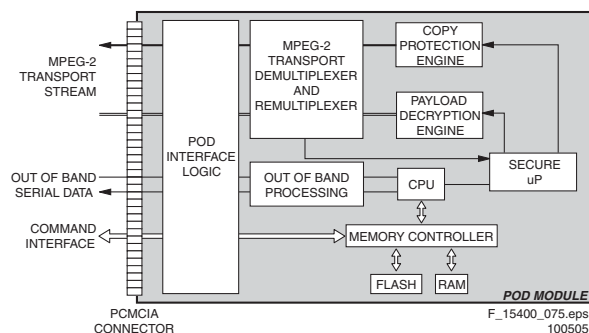


Figure 9-14 Example of POD design

9.5.3 Communication Channels**In Band (IB)**

- Forward Application Transport channels (FAT):
 - 256 QAM modulation (8 bits/symbol).
 - 54 - 864 MHz.
 - 6 MHz bandwidth.
 - Carry information via MPEG-2 streams.
 - Scrambled In-Band Channels.
 - TS packet header.
 - In-the-Clear channels.
- NTSC analog channels:
 - 8-VSB modulation (3 bits/symbol).
 - 54 - 806 MHz (UHF and VHF)
 - 6 MHz bandwidth.
 - Not via POD, but via MPIF.
 - With VBI (Vertical Blanking Interval) signals for closed captioning.

Out Of Band (OOB)

- Forward Data Channels (FDC):
 - DQPSK modulation (2 bits/symbol).
 - 70 - 130 MHz.
 - 6 MHz bandwidth.
 - Spaced between 6 MHz FAT and analog channels.

- Control and Access messages.
- Application code download.
- Only from cable operator towards user.
- Service Information (SI) like:
 - PMT: TS Program Map Table.
 - PAT: Program Association Table.
 - CAT: Conditional Access Table.
 - STT: System Time Table.
- Emergency Alert Service (EAS)= US federal system for alerting the public to emergencies; works before and after CableCARD insertion

9.6 MPIF (PNX 3000)**9.6.1 Introduction**

The MPIF (Multi Platform InterFace, type number PNX3000, item number 7C00) is an analog video and audio pre-processing unit for the AVIP TV processor. It contains the high frequent IF part and all the analog video and audio source switching for external in- and outputs. The MPIF can handle CVBS, Y/C, RGB (1fH/2fH) and YPbPr (1fH/2fH) video signals as well as stereo, I²S, and second sound IF audio signals. The MPIF converts the selected video and audio streams from the analog to the digital domain. Via three high-speed serial data links (I²D), the digitized audio and video signals are streamed (594 Mbit/s) to the AVIP IC for further processing. The MPIF uses a clock coming from the AVIP of 13.5 MHz and is I²C driven. The supply voltage for the MPIF is 5V.

The MPIF uses the following input signals:

- CVBS, Y/C, YPbPr, or RGB video format.
- 1fH or 2fH video.
- Clock 13.5 MHz from the AVIP.
- I²C from the VIPER.
- Clamping-pulse from the AVIP.

9.6.2 Block Diagram

Following figure shows the MPIF block diagram:

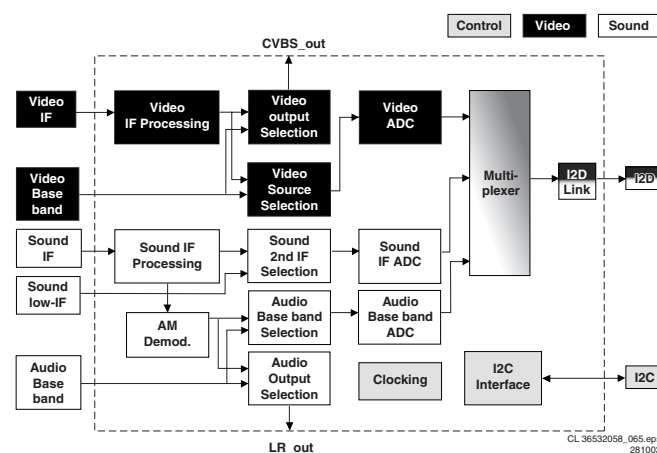


Figure 9-15 MPIF block diagram

9.6.3 IF Processing

The MPIF is capable of demodulation of RF signals.

Analogue Vision IF Processing

Some specifications:

- Synchronous demodulation of the IF vision carrier. Selectable frequency and auto-calibration of the VCO (Voltage controlled oscillator).
- Group delay correction for BG system.

- AGC at vision IF level to give fixed CVBS output level, and AGC at RF level (tuner AGC) to limit output level of the tuner.
- AGC gating for bad reception conditions.
- CVBS amplitude correction and mute.
- Detections for AFC and video presence.

The video signal is demodulated by means of an alignment-free PLL carrier regenerator with an internal VCO. This VCO is calibrated by means of a digital control circuit, which uses an external crystal frequency as reference. The frequency setting for the various standards (33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz) is realized via the I²C bus.

The AFC output is generated by the digital control circuit of the IF-PLL demodulator and can be read via the I²C bus.

The AGC-detector operates on "top sync" or "top white" level. The MPIF IC has an integrated sound trap filter. The trap frequencies can be switched via the I²C-bus.

Also, a group delay correction filter is integrated. The filter can be switched between the PAL BG curve and a flat group delay response characteristic. This has the advantage that in multi-standard receivers the video SAW filter does not need to be switchable (cost effective).

Analogue Sound IF Processing

Some specifications:

- A switch to select QSS or inter-carrier mode.
- Sound carrier frequency conversion at second IF sound frequency (SSIF)
- A switch to select internal or external SSIF.
- AGC at sound IF level (for QSS (quasi-split-sound) mode) and AGC at SSIF level (for inter-carrier and QSS modes).
- Demodulation of AM modulated carrier (L and L' standards).

The MPIF has a separate sound IF input to enable Quasi Split Sound (QSS) applications. The sound IF amplifier is similar to the vision IF amplifier and has a gain control range of about 55 dB.

The AGC detector measures the SIF carrier levels (average level of AM or FM carriers) and ensures a constant signal amplitude for the AM demodulator and QSS mixer.

For applications without SIF SAW filter, the IC can also be used in intercarrier mode. In this mode, the composite video signal from the VIF amplifier is fed to the QSS mixer and converted to the intercarrier frequency. AM sound demodulation is realized in the analog domain with the QSS mixer.

9.6.4 Source Selection

Below the main functions and features of the main blocks in the MPIF for video and audio are explained.

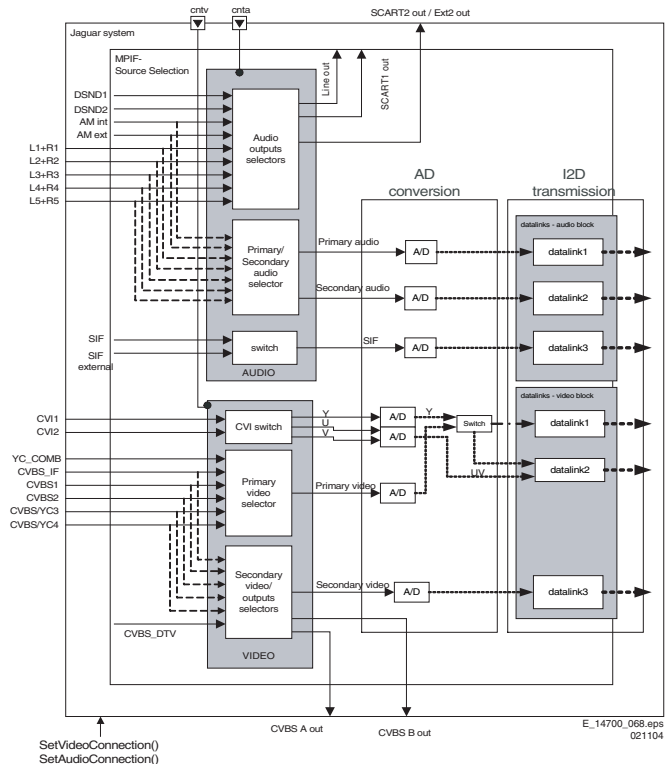


Figure 9-16 MPIF analog source selection block

Video Selectors

The CVI switch (Composite Video Input, including RGB, YUV, and YPbPr) is selecting the signal from one of the two CVI inputs; the output is always a YUV signal.

The primary video selector is selecting a signal from the CVBS and YC inputs; the video coding of the output signal equals to the video coding of the input signal.

The primary video selector has an extra input (YC_COMB), capable of selecting an Y/C signal from the comb filter. This input cannot be downscaled to a CVBS signal and fed back to the CVBS_A or CVBS_B output. It is also advisable not to connect other sources to the YC_COMB input because it is treated as an internal one that is not available for the outside world.

Two video output selectors are responsible for the contents of CVBS_A and CVBS_B video out.

Audio Selectors

The primary audio selector is selecting a signal from five external stereo inputs and one stereo input that handles two mono signals (AM internal and AM external). The AM internal signal is demodulated in the IF part and is internally routed, so not available as external input. Additionally, the AM internal signal is available on the left channel whereas the AM external signal is available on the right channel.

The secondary audio selector is selecting a signal from the same range as the primary audio selector; the second audio selector can work in stereo or mono mode. In case the stereo mode is selected, it is alike the primary audio selector. In mono mode, the input stereo signal L+R is transformed into a mono signal (L+R)/2 and put on the left channel of the stereo output. When the stereo input (handling two mono signals) is selected and the selector works in mono mode, the AMint and AMext can be swapped on the primary as well as on the secondary audio channel. It is also possible to digitize the mono + AM on the secondary audio channel.

Further it is possible to select the AM signal on the analog audio outputs independently from the AM signal that is selected for the secondary (digital) audio channel.

Three audio output selectors are responsible for the content of the Line, SCART1, and SCART2 outputs. These selectors

allow selection of the output out of five L+R inputs, two mono signals (AM internal or AM external) and two externally connected DSND streams.

SIF Switching

SIF (Sound Intermediate Frequency) switching allows selecting between internal or external SIF signals.

AD Converters

The second part of the MPiF is responsible for conversion of the chosen signals into digital signals and grouping them into three data streams. Each data stream handles both video and audio. These data streams are fed into three data links and send via I2D to the outside.

The MPiF contains four video ADCs for analog and digital video broadcast signals. The clock frequency for these ADCs is either 27 MHz or 54 MHz. In some cases, two analog signals are multiplexed at the input of one ADC. In these cases, the clock frequency of the ADCs is 54 MHz, while the sample frequency for each of the two signals is 27 MHz.

The sample frequency for standard 1fH video signals is 27 MHz. For the YUV channel the sample frequency of the U and V components is half the sample frequency of the Y signal. For 2fH YPbPr or RGB input signals (for instance 480p or 1080i ATSC signals), the frequency that is used to sample the YUV signals is twice as high as for 1fH signals. The sample frequency is 54 MHz for Y and 27 MHz for U and V. Due to the high sample frequency, two data links are needed for transport of the video data to the digital video processor.

I²D Data Link

The digital interface between MPiF and AViP is called Data Link (or I²D Link). This is a serial interface that transfers the data from MPiF to AViP over three Data Link interfaces. Each Data Link has a data signal and a strobe signal. The synchronization information is distributed over the data and the strobe signal. To minimize EMC, both signal outputs are low voltage differential swing signals, with a swing of about 300 mV.

Each Data Link has four lines, one differential pair for the data, and one differential pair for the strobe. The data rate is 594 Mbit/s. Each Data Link can carry two 27 MHz sampled video streams (or one 54 MHz sampled 2fH video stream) and two audio channels sampled at 6.75 MHz.

In the MPiF, the (video and audio) data to be transmitted is multiplexed in an output register of 44 bits (including the 2 bit sync information). The content of that 44 bits register is serial transmitted on one of the three data links. In the AViP, the serial data is de-multiplexed into parallel streams. The data on the data link is divided in several groups of signals (video, audio and strobe signals). Obvious it is important that the transmitter and receiver are in the same transmitting mode

Data links can operate in two different modes called:

1. Normal mode.
2. YUV2fH.

Normal Mode

In the normal mode the content of the data links is as follows:

Table 9-2 Normal mode

Data Stream	Video	Audio
1	CVBS/YC primary	(L+R) primary
2	YUV 1fH	(L+R) secondary
3	CVBS secondary	SIF
Data link Mode bit: DM= 0		

In the normal mode the data links can handle up to three video signals: CVBS or YC signal from the primary video selector, CVI 1fH source selected on the CVI switch, and CVBS signal from the secondary video selector.

YUV 2fH Mode

In the YUV 2fH mode (higher bandwidth signal) the data links content is as follows:

Table 9-3 YUV 2fH mode

Data Stream	Video	Audio
1	Y 2fH	(L+R) primary
2	UV 2fH	(L+R) secondary
3	CVBS secondary	SIF
Data link Mode bit: DM= 1		

The data link 1 can output only one of two input signals: the output of the primary video selector or the Y output of the CVI switch. Only one can be active at a moment, and that is determined by the data link mode bit (DM). It means, that for data links working in YUV 2fH mode, the data link 1 carries the Y component of the YUV 2fH signal, the data link 2 carries the UV component, and the data link 3 contains the signal that is connected through the secondary video selector.

9.7 PNX2015

The functional blocks of the PNX2015 (item 7J00) are:

- Audio Video Input Processor (AViP).
- 3D Comb Filter (COLUMBUS).
- High Definition MPEG Decoder (HD Subsystem).
- LVDS transmitter.
- Stand-by Processor for low-power control.

BLOCK DIAGRAM

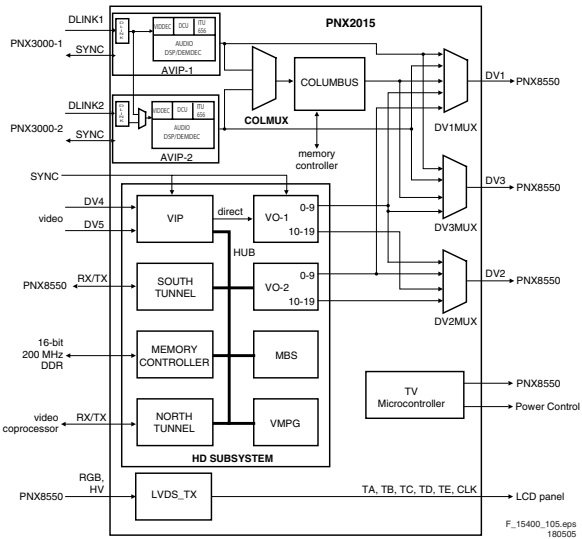


Figure 9-17 Block diagram PNX2015

These different blocks are described separately in the next paragraphs.

9.8 PNX2015: AVIP

9.8.1 Introduction

The AVIP (Audio Video Input Processor) receives the digital data via the I²D link (coming from MPIF). It reformats this data and maps (synchronizes) the data to the clock of the AVIP. Then a digital AGC is passed. After this, the video decoding is performed in the VIDDEC-block of the AVIP. The decoded video is sent to an output block, which formats the data to an ITU-656 compatible standard data stream.

The AVIP power supply is 1.2 V and 3.3 V. To ensure synchronization of video streams processed across the VIPER and PNX2015 devices, a 27 MHz is coming from the VIPER. The AVIP is I²C driven.

Initialization of this IC begins with a hard reset (MIPS-RESET) provided by the VIPER. Besides video decoding, the AVIP is also used for decoding and presentation of all audio output streams in the system.

9.8.2 Block Diagrams

Below the main functions and features in the AVIP for video and audio are given.

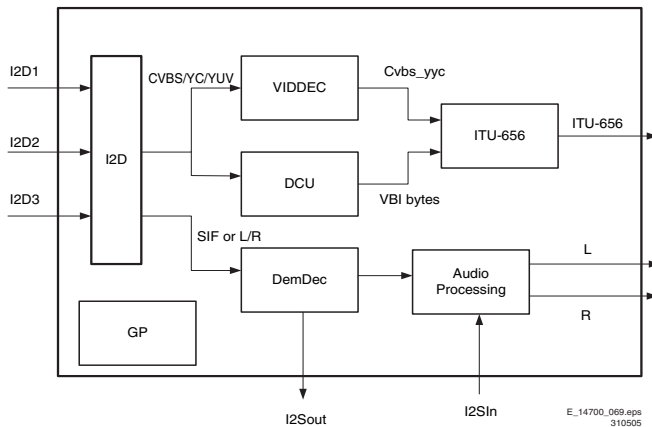


Figure 9-18 AVIP block diagram

Main AVIP function:

- I²D receiver.
- Color decoding into ITU-601 compatible format (1fH/2fH).
- Interface with 3D comb filter (called Columbus in this chassis).
- VBI data capture via DCU (Teletext, CC, etc.).
- ITU-656 formatting.
- Audio demodulation and decoding via DEMDEC.
- Audio processing and D/A conversion.

I²D Receiver

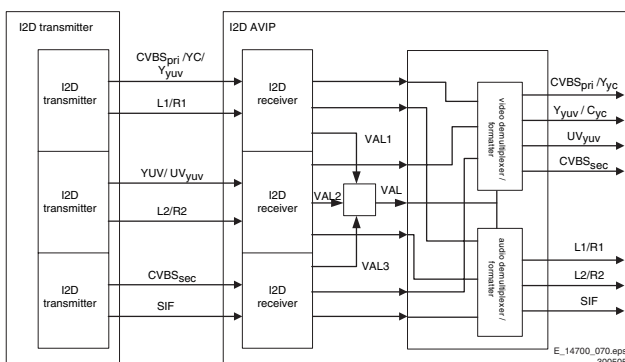


Figure 9-19 I²D receiver block diagram

The receiver block gets the serial data stream and converts it to a parallel stream. This parallel data is fed to the "de-multiplexer and formatter" block where the selected audio/video stream is forwarded to the video and audio decoder for further processing. This communication bus is completely digital and very difficult to monitor.

The I²D link has the following characteristics.

- The data-link runs at 297 MHz / 594 Mbps.
- The driver rise/fall time is around 200 ps.
- The data-link uses differential signals.

VIDDEC (Video Decoder)

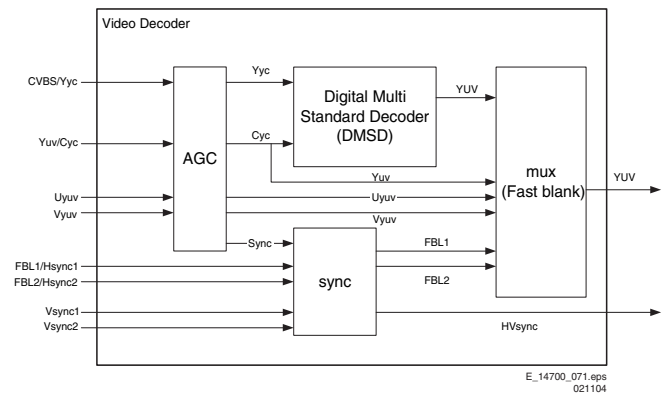


Figure 9-20 VIDDEC block diagram

The CVBS/YC/YUV signals (coming from the I²D receiver block) enter the DMSD block (Digital Multi Standard Decoder) via the AGC (Automatic Gain Control) block. The multiplexer block (MUX) takes care of the correct output signal. The sync signals are processed in the sync block.

The VIDDEC has the following main functions:

- Multi standard color decoder.
- Automatic system recognition.
- Fully programmable static or automatic (AGC) for all analog video base band signals.
- AGC on sync amplitude in digital domain.
- Selectable peak white control.
- AGC for chrominance (PAL and NTSC only).
- Programmable Luminance and Chrominance bandwidth for CVBS and Y/C sources.
- Programmable clamp window for the selected video base band signals.
- Digital PLL for synchronization on 2fH and ATSC standards.
- Horizontal (including 3-level sync for 2fH) and vertical sync detection.
- Automatic detection of 50/60Hz ATSC field frequency.
- Adaptive 2/4-line delay comb filter for two-dimensional Chrominance/Luminance separation.
- Copy protected source detection according to MacroVision up to version 7.01
- Possibility of RGB insertion through fast blanking in CVBS input mode, not in Y/C.

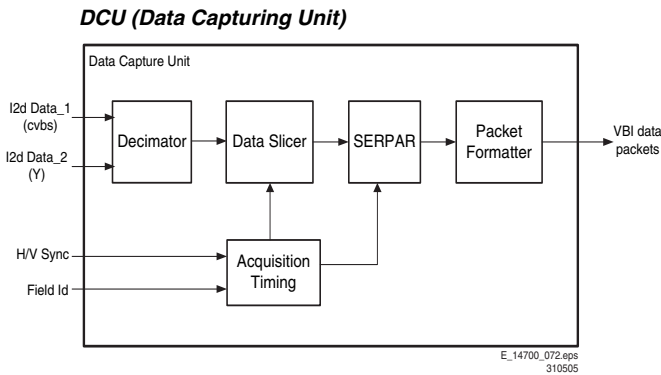


Figure 9-21 DCU block diagram

The purpose of this block is to acquire digital data (containing Teletext, Closed Captions, ...) from a CVBS/Y/C video input source. It performs processing on the received data and provides the data to the ITU-656 formatter unit.

The decimator reduces the sample rate (from 27 MHz to 13.5 MHz) of the incoming digitized CVBS or Y data stream from the I²D receiver. From the video input, the data slicer reconstructs the transmitted bit stream and associated clock. The SERPAR block converts the serial bits, coming from the data slicer, into parallel bytes. The packet processor performs data decoding and some error correction, assembles received bytes into packet structure, and streams out the data to the ITU-656 formatter.

The acquisition-timing block locks onto sync signals, and provides timing information to the other blocks of the data capture unit.

ITU656 Output Formatter

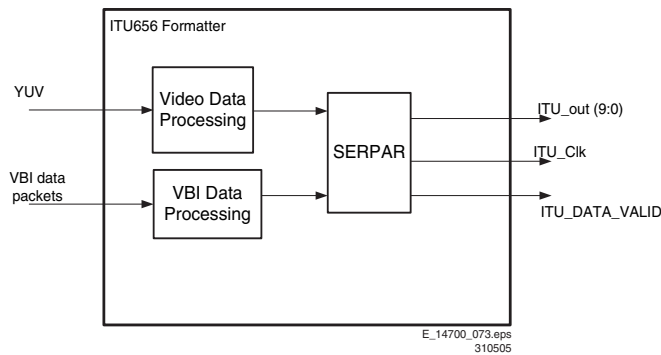


Figure 9-22 ITU656 formatter block diagram

The ITU656 formatter gets YUV data as video input signal, coming from the VIDDEC block. These YUV data are either decoded CVBS signals, matrixed RGB signals, or YUV input signals. The second input data are VBI sliced data coming from the DCU. The output of the ITU delivers a data stream, which is ITU-601/656/1364 compliant, and includes video as well as the VBI data.

DEMDEC (Demodulator and Decoder)

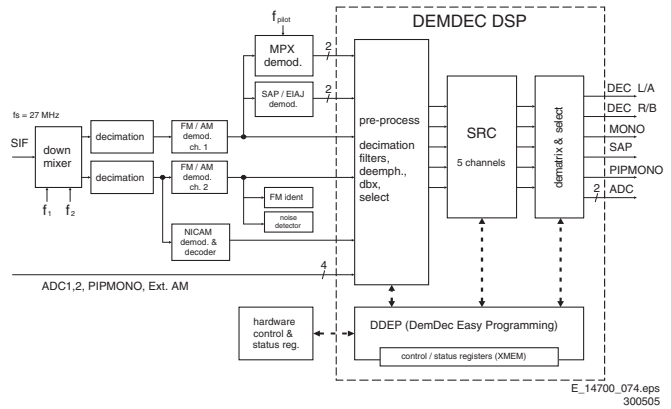


Figure 9-23 DEMDEC block diagram

The demodulator and decoder (DEMDEC) is responsible for demodulating and decoding incoming SIF signals.

The main features of the DEMDEC are:

- Auto Standard Detection (ASD).
- DQPSK demodulation for different standards, simultaneously with 1-channel demodulation.
- NICAM decoding (B/G, I, D/K, and L standard).
- Two-carrier multi standard FM demod. (B/G, D/K and M).
- Optional AM demodulation for system L, simultaneously with NICAM.
- Identification A2 systems (B/G, D/K and M standard) with different identification time constants.
- FM pilot carrier present detector.
- BTSC MPX decoder.
- SAP decoder.
- dBx noise reduction.
- Japan (EIAJ) decoder.
- FM radio decoder.

Audio Processing

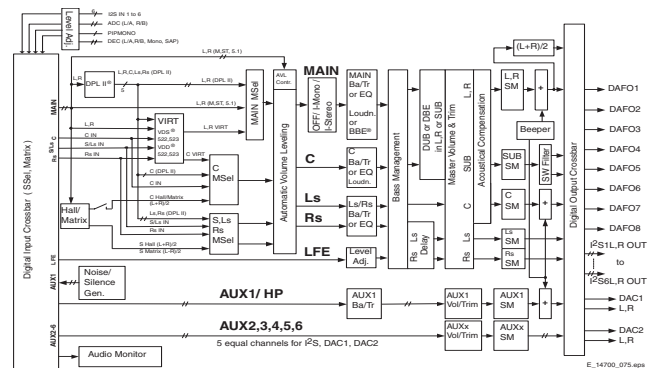


Figure 9-24 Audio processing block diagram

Main features are:

- Master volume control and Balance.
- Tone control (Loudness, Bass, Treble, Equalizer).
- Dolby ProLogic delay.
- Incredible Mono and Stereo.
- Virtual Dolby Surround (VDS 522, 523).
- Virtual Dolby Digital (VDD 522, 523).
- Digital audio I/O interface (stereo I2S input interface).
- Eight audio DACs for six channel loudspeaker outputs and stereo headphones output.
- Audio DACs for stereo SCART output and stereo LINE output.
- Serial data link interface for interfacing with the analog multi-purpose interface IC PNX3000 (MPIF).

9.9 PNX2015: Columbus (Comb Filter)

9.9.1 Introduction

This block provides the following picture improvement functions:

- Enhanced 2D combing for PAL and NTSC.
- 3D field combing for PAL and NTSC.
- 3D frame combing for PAL and NTSC.
- Spatial noise reduction for all component video standards.
- Temporal noise reduction for all component video standards.

The comb filter is controlled via a separate I²C interface on the PNX2015, this is to ensure registers containing measurement information, are accessed at appropriate times. The measurement information is also available as ancillary data within the video stream (ITU-656).

For certain features of the comb filter, access to external memory is required. The PNX2015 has a unified memory that both comb filter and HD subsystem's share concurrently.

9.9.2 Block Diagram

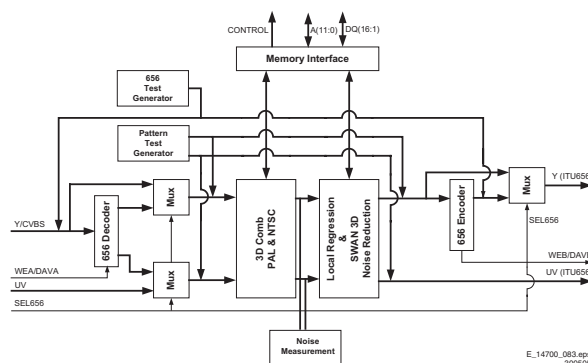


Figure 9-25 COLUMBUS internal block diagram

Figure above, shows a block diagram of the Columbus comb filter in the PNX2015 device. An input video signal is supplied by the AVIP and fed to the Columbus block. The signal is supplied in digitized components of:

- CVBS or Y.
- Uncombed U.
- Uncombed V.

The CVBS signal is combed, extracting the luminance components and rejecting the chroma components. The UV signals are combed, rejecting the left over luminance components, from a previous filtering (normally band pass filtered).

The outputs from the 3D comb filter are:

- Combed luminance signal (Y).
- Combed U signal.
- Combed V signal.

The output from the 3D comb filter feeds the SWAN and LORE noise reduction block, which performs spatial/temporal noise reduction, for both luminance and chrominance components.

Control Register Interface

The control registers are accessed via I²C. Most signals that can be written via I²C are double buffered. The fast I²C interface implemented on the COLUMBUS is a 5V compliant, 400 kHz slave receiver/transmitter. The I²C will not be blocked during voltage shorts or opens.

For the system dependent parameters of the 3D-Comb filter, five register banks are present. Data can be written in one of

the banks via I²C, by programming bits [2:0] of the SYSTEM_SELECT register. The bits [6:4] of the SYSTEM_SELECT register select, which register bank is used by Columbus to define the filter settings.

Bank number	System
0	PAL B, G, H, I, D, K
1	PAL M
2	PAL N
3	NTSC
4	Bypass

Internal Test Generators

There are two test generators inside the COLUMBUS chip:

- The "656 test generator" generates a 656 compliant stream and is used for testing the functionality of the 656 encoder and decoder. The 656 stream can be injected at the front end or the back end of the chip.
- A second internal test pattern generator enables testing of the device and attached external memory (if present). The test pattern generator signal can be inserted at the front end of the chip (passing through the 3D Comb and noise reduction system and external memory) or at the back end of the chip. Test patterns are available for both PAL/SECAM and NTSC systems.

9.10 PNX2015: HD Subsystem

The HD subsystem performs MPEG video decoding on HD/SD transport streams. It interfaces with the PNX8550 and video coprocessor via tunnel interfaces, HD/SD using DV4 and DV5 inputs, and PNX8550 using DV1, DV2 and DV3 outputs. The HD subsystem can also perform horizontal and vertical scaling of video images, and perform a range of video measurements on a transport stream.

9.11 PNX2015: LVDS Transmitter

Low Voltage Differential Signaling (LVDS) is a low-power, low-noise differential technology for high speed data transmission over two PWB traces, or a balanced cable. LVDS allows single-channel data transmission at hundreds, or even up to a thousand Mbps. Low swing and current-mode driver outputs create low noise and provide very low power consumption across frequency ranges. The LVDS transmitter IP provides a connection interface to FPDs.

Differences between standard and LVDS signalling:

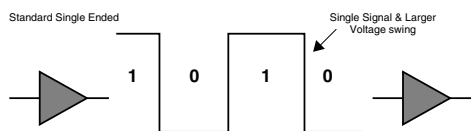
- Standard single ended signal (TTL):
 - Requires 28 signal lines and more than 14 grounds.
 - Single ended signals up to 3 V.
 - Wide flat ribbon cable.
 - EMI/EMC problems.
 - Feasible up to VGA/NTSC resolution (limited to 250 Mb/s).
- LVDS:
 - Five low voltage (350 mV) differential pairs: one clock pair and four data pairs.
 - Five grounds.
 - EMI/EMC friendly.
 - WXGA and HD-1280x720p (up to 1 Gb/s).

LVDS offers superior performance compared to the standard single ended signal (TTL).

It is even "protocol independent" so it requires no software.

- Lower Voltage Swing (only 350 mV vs. 3 V)

- Allows faster Clocking
- Standard open Ended: 250Mbps
- LVDS: >1 Gbps



- Differential Signals (Two Signals) ...Low Noise!

- Receiver reads a 1 or 0 based on the delta of the two signals.
- Noise Impacts both lines and cancels out each others.

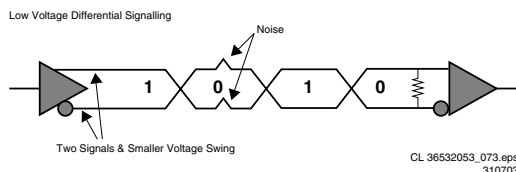


Figure 9-26 LVDS technology

The digital video output from the VIPER is connected to the display via the LVDS interface. This transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signalling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. With every cycle of the transmit clock, 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec.

9.12 PN2015: Stand-by Processor

9.12.1 Introduction

The Stand-by Processor's sub system is isolated from the other sub systems within the PN2015. It has its own power supply (1.2V and 3.3V), together with separate clocking (16MHz) and reset. This allows for it to be active while all other sub systems are either inactive, via clock being disabled, or powered down.

The main tasks of the Stand-by Controller are:

- RC5/RC6 remote control handling.
- P50.
- Keyboard handling (side control, "on/off" switch).
- Detection and protection of the power supplies.
- Status detection on EXTERNALS.
- SAM/SDM entering.
- Provide boot-scripts to the VIPER.
- Start-up behavior of the set; sequentially enabling the power supplies via the ENABLE lines.

9.12.2 TV Start-up Behavior and Fault Detection

1. The Stand-by Controller is powered by the +5V2 voltage (3V3_STBY voltage is derived from the +5V2), which becomes available when the set is connected to the Mains / AC Power.
2. By default, all I/O lines of the controller are "high", this state is also the state that will not trigger protections or cause supplies to rise, since enabling a supply requires that an I/O line is pulled "low". Also all protections are active "low".
3. The 16 MHz crystal starts running.
4. Reset IC 7M03 will generate a RESET_STBY pulse.

5. All I/O lines will be set in default state, as "told" by the software.
 - RESET_SYSTEM will be "low" (this will hold the VIPER in reset).
 - LAMP_ON will be "low".
6. The system waits for an RC or functional switch command: when this command is "low" the set will start-up.

The Stand-by Microprocessor is responsible for the start-up of the VIPER, by providing the correct timing for the DC/DC converted voltages (for timing of DC/DC converter voltages see description in paragraph "Power Supply").

The +12V switch (via POD_MODE) and the DC/DC converters (via ENABLE) are switched "on" (active "low"). Once these voltages are switched "on", the Stand-by Controller is monitoring these voltages via a voltage detector circuit connected to port P2.x. When one of the voltages is missing, the fault detection will be active "low" on port P2.x. An error code will be written in the error buffer.

There is a common SUPPLY_FAULT line; connected to port P1.3 (INT5) that is active "low" when there is a problem detected on one of the DC/DC power supplies driver circuits. One input (P2.6) is used for the Audio Supply protection from the audio amplifier.

The RESET_SYSTEM line (P4.0) is "low" in Stand-by and at Start-up to keep the VIPER in reset state. Once the VIPER core supply is available, the RESET_SYSTEM line will become "high". The VIPER is starting up and will provide a RESET-MIPS active "high" to the Stand-by Processor P3.3, AVIP, and COLUMBUS.

9.12.3 I/O Stand-by Processor

The inputs on the Stand-by Microprocessor are used to detect the AV status from the front inputs (see also the control block diagram in chapter 6 "Block diagrams,...").

An UART communication line via an electronic switch is available on a connector and will be used for Service to communicate with ComPair. The UART line is switched to the Stand-by Processor when the UART_SWITCH line (P0.7) is "high". Otherwise it is switched to the VIPER.

9.13 VIPER 2 (PNX 8550)

9.13.1 Introduction

The PNX8550 is a highly integrated media processor intended for deployment in analog, digital, and hybrid TV receivers. It can be used for 100 Hz interlaced as well as 60 Hz progressive screens. It is fully capable of performing advanced video improvement algorithms, such as Digital Natural Motion™, on Standard Definition analog or digital sources. It includes an HD capable de-interlacer for converting interlaced HD transmission signals to progressive output for driving wide-XGA class Plasma or LCD displays. Two 32-bit 240 MHz VLIW media processors, referred to as the TriMedia TM3260 CPU core, carry out the advanced video improvement processing as well as all audio operations. Fixed hardware functions perform stable core video functions, such as picture level MPEG2 decoding, scaling, image composition and pixel post processing.

The PNX8550 provides a primary digital (YUV or RGB) output to connect to the display specific output processor. In addition, a secondary analog video output (CVBS or S-Video) for a VCR is available. This is the so-called DENC-out. It can operate either in analog PAL/NTSC or digital mode.

9.13.2 Block Diagram

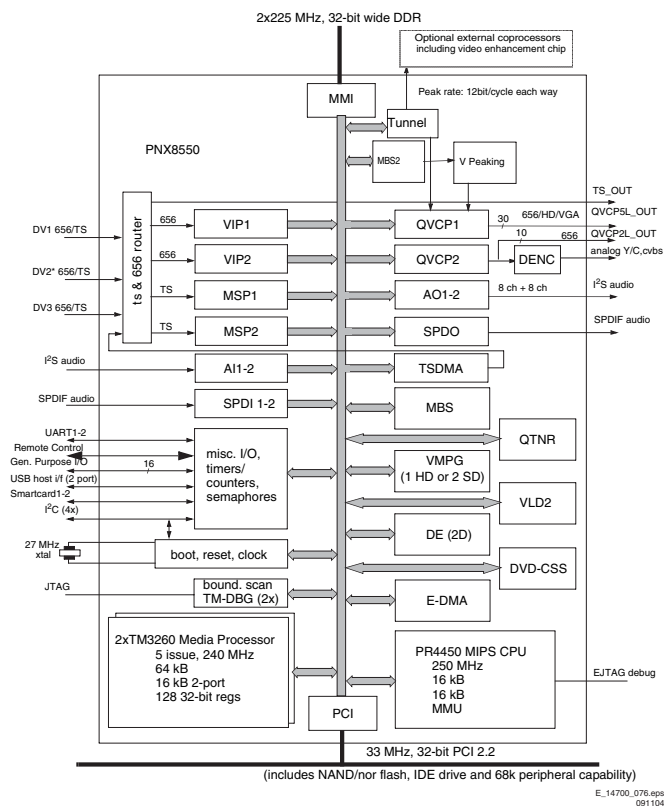


Figure 9-27 VIPER 2 internal block diagram

Control

An embedded MIPS32 processor (PR4450) running at 266 MHz is available to run the Operating System. The PR4450 processor is primarily responsible for running the demand paged graphics-intensive operating system, while the TM3260 media processors are responsible for running all real-time media functions. All hardware resources inside the PNX8550 are accessible by both the MIPS processor and the TM3260 CPUs. A "sandbox" style system protection provision ensures that selected MIPS memory regions and critical peripherals cannot be corrupted or inspected.

VIP (Video Input Processor)

The Video Input Processors (VIP) handles incoming digital video and processes it for use by other components of the PNX8550. It provides the following functions:

- Receives 10-bit YUV4:2:2 digital video data from the selected DVx video port (input signal coming from the AVIP or Columbus IC output). The data is dithered down to in-memory 8-bit data format.
- Performs horizontal down scaling or up scaling by 2x (not available in HD video capture mode).
- Provides an internal Test Pattern Generator with NTSC, PAL, and variable format support.
- Acquire VBI data using a separate acquisition window from the video acquisition window.
- ANC header decoding or window mode for VBI data extraction.
- Interrupt generation for VBI or video written to memory input mode.
- Color space conversion (mutual exclusive with horizontal scaling).
- Raw data mode captures of 8- or 10-bit data.

MBS (Memory Based Scaler)

The PNX8550 contains a Memory Based Scaler that performs operation on images in main memory. The MBS can either be controlled task by task by a TM3260, or it can be given a list of

de-interlacing and scaling tasks. It reads images from memory, performs a transformation, and writes the result back in memory.

The MBS main features are:

- De-interlacing using either a median, 2-field majority select, or 3-field majority select algorithm with an edge detect/correct post-pass (these three provide increasing quality, at expense of increased bandwidth).
- Edge detect/correct on an input frame that has been software de-interlaced (this provides future capabilities in case we develop a better core de-interlacer than 3-field majority select).
- Horizontal and vertical scaling (on the input image, or on the result of edge detect/correct stage).
- Linear and non-linear aspect ratio conversion.
- Anti-flicker filtering.
- Conversions from any input pixel format to any non-indexed pixel format, including conversions between 4:2:0, 4:2:2 and 4:4:4, indexed to true color conversion, color expansion / compression, de-planarisation / planarisation (to convert between planar and packed pixel formats), programmable color space conversion.

Supported video measurement functions during scaling or de-interlacing pass:

- Gather a histogram of luminance values (this data is used by software to control histogram modification).
- Measure noise level inside a rectangular window.
- Measure the lowest level luminance within a rectangular window (used to control black stretch in QVCP).
- Measure UV bandwidth inside a rectangular window.

QTNR (Quality Temporal Noise Reduction and Video Measurement)

The QTNR block has two primary functions: Temporal Noise Reduction: reading two video fields from memory, "current" (noisy) and "previous" (noise reduced) and producing a noise-reduced version of "current" in memory. While doing this, or as a separate "measurement only" pass, perform video measurements:

- Gather a histogram of luminance values (this data is used by software to control histogram modification).
- Measure noise level inside a rectangular window.
- Measure the lowest level luminance within a rectangular window (used to control black stretch in QVCP).
- Measure UV bandwidth inside a rectangular window.
- Measure the position of top and bottom black bars in the image.

QVCP (Quality Video Composition Processor)

The PNX8550 contains two QVCPs, which are responsible for combining and displaying video and graphics images from main memory. The primary QVCP serves as the main display pipeline, the second one is targeted to be connected to a record device (VCR). The primary QVCP allows composition of up to five layers, and can output in ITU-656/HD/VGA format in 10 bits per component up to 81 Mpix/s.

The secondary QVCP allows composition of up to two layers, can output in 656 10-bit component mode up to 81 MHz (40.5 Mpix/s). The secondary QVCP is connected to an on-chip Digital Video Encoder (DENC), allowing direct analog CVBS or S-video output.

In analog output mode, standard definition interlaced NTSC or PAL is supported (SCART2-out signal, for VCR-recording). The encoder has two DACs. DAC1 provides CVBS or luminance for S-video. DAC2 provides chrominance for S-video.

Internal sensors allow software to test loading on the S-video Chrominance line to decide whether to output luminance or CVBS on DAC1.

The primary and secondary QVCP each contain a series of layers and mixers. The QVCP creates a series of display data layers (pixel streams) and mixes them logically from back to front to create the composite output picture.

Some of the features the QVCP provides are:

- Video Quality Enhancement.
- Luminance Transient Improvement.
- Color Dependent Sharpening.
- Horizontal Dynamic Peaking.
- Histogram Modification.
- Digital Color Transient Improvement.
- Black Stretch.
- Skin Tone Correction.
- Blue Stretch and Green Enhancement.
- Video and Graphics horizontal up scaling.
- Color space unification of all the display surfaces.
- Contrast and Brightness Control.
- Screen timing generation adopted to the connected display requirements (SD-TV standards, HD-TV standards, progressive, interlaced formats).

9.14 MOP

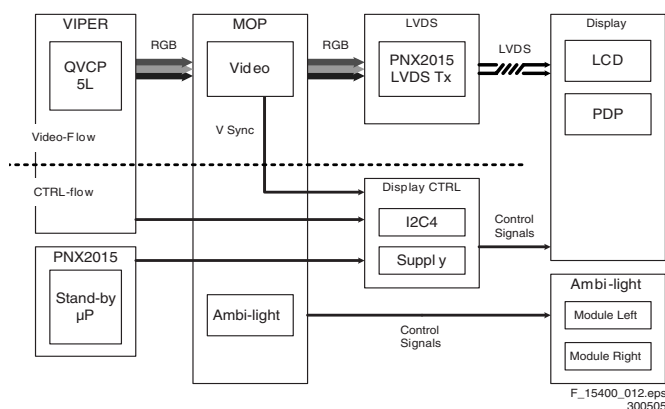


Figure 9-28 Block diagram of video output with MOP

In the BP2.2 chassis an EPLD (or MOP) is used for AmbiLight processing and for some picture enhancements, like blue and green stretch. For sets without AmbiLight (like BP2.3), the picture enhancements are done in the VIPER.

9.15 Ambient Light (if present)

9.15.1 Introduction

At the rear left and right side of the TV-set, three gas discharging lamps are mounted. With the red, green, and blue lamps, each color can be made.

- Ambient light is adjustable with three variables: Hue, Saturation, and Brightness.
- Hue and saturation are controlled via menu control or via smart settings.
- The brightness is controlled via menu or via a cycle generator.
- The light sensor influences the brightness.
- Switching "on" or "off" goes via a ramp up or down.
- The ambient light may be active or passive.

In the user set up menu the following items are added:

- Ambient Light.
- Lights "On/Off".
- Ambient Light: "Personal/Normal/Warm/Cool".

Two extra keys are added on the Remote Control:

- ON/OFF: A (normal) press on this key switches the Ambient Light "On/Off".

- MODE: In case the set is "On", to toggle the smart modes.

Specifications:

- Lamp current frequency= 43 kHz.
- Lamp dimming frequency= 85 Hz.
- PWM duty cycle range= 30%
- Each lamp is only driven one third of the period to avoid crosstalk (drive lamps at 33.3% to have no losses in output).

The difference between the BP2.1 and BP2.2 for AmbiLight is that the BP2.1 has (software driven) stereo Ambilight, while the BP2.2 has the mono version.

9.15.2 Block Diagram

All mentioned blocks (from "Cycle Generator" to "HSV-to-RGB Converter" are implemented in the main software. Via I²C, the RGB values are sent to the MOP (where a selection is made between "active" and "passive" mode) and again via I²C the Inverter board is addressed.

In "passive" mode, the RGB values from the "HSV-to-RGB Converter" are used, while in "active" mode the picture content is used to steer the ambient lights.

Cycle Generator

The Cycle Generator (for fade in/out) starts with a long press on the "On/Off" button on the RC. It stops when the button is released.

Light Sensor

The light sensor influences the Brightness: when the room is darker, the ambient light is reduced. The amount of dimming is set according to an algorithm in the Auto TV software. In "active" Ambient Light mode, the light sensor does not influence the Brightness.

Ramp Up/Down

The Brightness is changing with a speed from min. to max. in 2 s.

HSV to RGB Converter.

The HSV (Hue, Saturation, Value) values are converted to RGB values.

Outputs

The outputs are RGB values and can individually be decreased.

MOP (EPLD)

In "passive" mode, the EPLD sends the info from the OTC directly to the inverter board. In "active" mode, the EPLD calculates the RGB values. Hue and Saturation are not adjustable, Brightness is adjustable.

9.15.3 Inverter Board

This board is for Service a "Black Box". This means that it is not repairable on component level, but when found defective, the board must be swapped. See the Spare Parts List for the order code.

Some specifications:

- There are three inverters to drive the lamps, each inverter drives a lamp for one color.
- DC-to-AC converter: 2.3 kV.
- Able to drive Cold Cathode Fluorescent Lamps (CCFL). There are two lamp units, three lamps (RGB) per unit= six lamps.
- The lamps are driven with Pulse Width Modulation (PWM).
- The inverters and lamps are supplied with 12V from main supply.

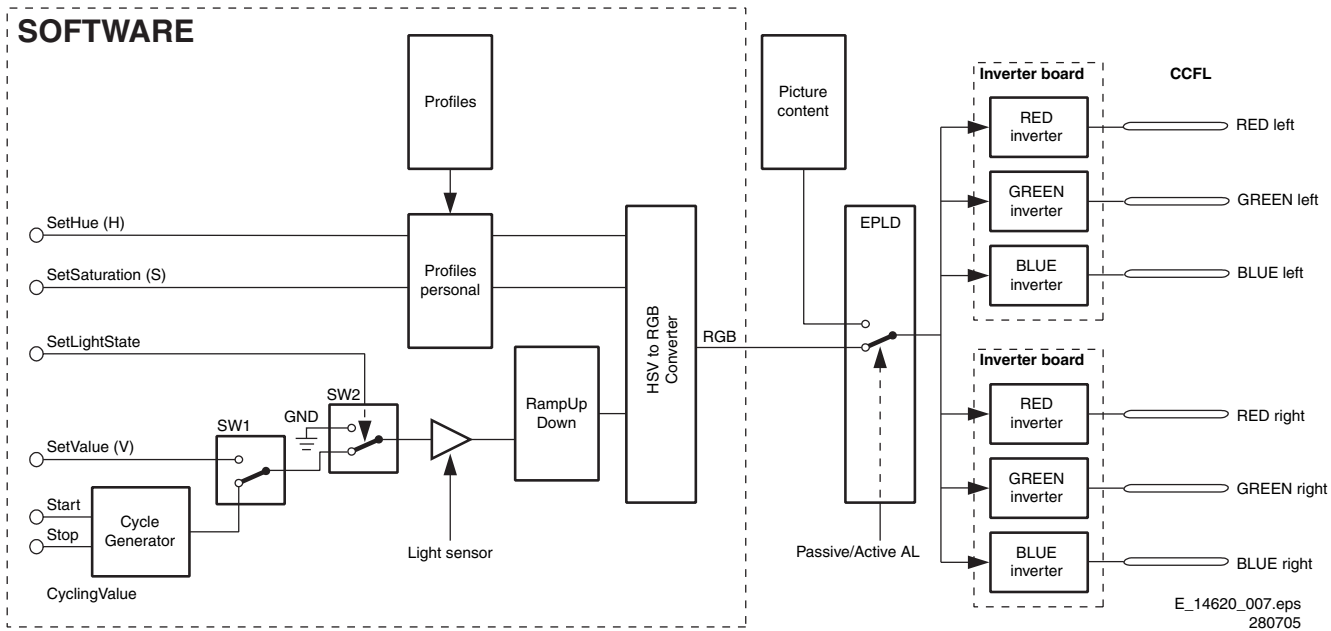


Figure 9-29 Ambient light block diagram

9.16 Abbreviation List

0/6/12	SCART switch control signal on A/V board. 0 = loop through (AUX to TV), 6 = play 16:9 format, 12 = play 4:3 format	CVBS	Composite Video Blanking and Synchronization
2DNR	Spatial (2D) Noise Reduction	DAC	Digital to Analogue Converter
3DNR	Temporal (3D) Noise Reduction	DBE	Dynamic Bass Enhancement: extra low frequency amplification
AARA	Automatic Aspect Ratio Adaptation: algorithm that adapts aspect ratio to remove horizontal black bars; keeps the original aspect ratio	DDC	See "E-DDC"
ACI	Automatic Channel Installation: algorithm that installs TV channels directly from a cable network by means of a predefined TXT page	D/K	Monochrome TV system. Sound carrier distance is 6.5 MHz
ADC	Analogue to Digital Converter	DFU	Directions For Use: owner's manual
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency	DMR	Digital Media Reader: card reader
AGC	Automatic Gain Control: algorithm that controls the video input of the feature box	DNR	Digital Noise Reduction: noise reduction feature of the set
AM	Amplitude Modulation	DRAM	Dynamic RAM
ANR	Automatic Noise Reduction: one of the algorithms of Auto TV	DRM	Digital Rights Management
AP	Asia Pacific	DSP	Digital Signal Processing
AR	Aspect Ratio: 4 by 3 or 16 by 9	DST	Dealer Service Tool: special remote control designed for service technicians
ASF	Auto Screen Fit: algorithm that adapts aspect ratio to remove horizontal black bars without discarding video information	DTCP	Digital Transmission Content Protection; A protocol for protecting digital audio/video content that is traversing a high speed serial bus, such as IEEE-1394
ATSC	Advanced Television Systems Committee, the digital TV standard in the USA	DVD	Digital Versatile Disc
ATV	See Auto TV	DVI(-d)	Digital Visual Interface (d= digital only)
Auto TV	A hardware and software control system that measures picture content, and adapts image parameters in a dynamic way	EAS	Emergency Alert Signalling; A cable TV standard (SCTE18) to signal emergency information to digital terminal devices
AV	External Audio Video	ECM	Entitlement Control Message
AVIP	Audio Video Input Processor	E-DDC	Enhanced Display Data Channel (VESA standard for communication channel and display). Using E-DDC, the video source can read the EDID information from the display.
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz	EDID	Extended Display Identification Data (VESA standard)
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries	EEPROM	Electrically Erasable and Programmable Read Only Memory
B-TXT	Blue TeleTeXT	EMI	Electro Magnetic Interference
C	Centre channel (audio)	EMM	Entitlement Management Message
CA(M)	Conditional Access (Module)	EPLD	Erasable Programmable Logic Device
CEC	Consumer Electronics Control bus: remote control bus on HDMI connections	EU	Europe
CIS	Card Information Structure: Protocol which identifies the card in a POD module	EXT	EXternal (source), entering the set by SCART or by cinches (jacks)
CL	Constant Level: audio output to connect with an external amplifier	FAT	Forward Application Transport channel
COLUMBUS	COlor LUminance Baseband Universal Sub-system	FBL	Fast BLanking: DC signal accompanying RGB signals
ComPair	Computer aided rePair	FDC	
CP	Connected Planet / Copy Protection	FDS	Full Dual Screen (same as FDW)
CSM	Customer Service Mode	FDW	Full Dual Window (same as FDS)
CSS	Content Scrambling System; An encryption method for MPEG-2 video on DVDs. The algorithm and keys required to decode the disc are stored on the DVD-player	FLASH	FLASH memory
CTI	Color Transient Improvement: manipulates steepness of chroma transients	FM	Field Memory or Frequency Modulation
		FTV	Flat TeleVision
		Gb/s	Giga bits per second
		G-TXT	Green TeleTeXT
		H	H_sync to the module
		HD	High Definition
		HDD	Hard Disk Drive
		HDCP	High-bandwidth Digital Content Protection: A "key" encoded into the HDMI/DVI signal that prevents video data piracy. If a source is HDCP coded and connected via HDMI/DVI without the proper HDCP decoding, the picture is put into a "snow vision" mode or changed to a low resolution. For normal content distribution the source and the display device must be enabled for HDCP "software key" decoding.
		HDMI	High Definition Multimedia Interface
		HP	HeadPhone

I	Monochrome TV system. Sound carrier distance is 6.0 MHz	OTC	On screen display Teletext and Control; also called Artistic (SAA5800)
I ² C	Integrated IC bus	P50	Project 50: communication protocol between TV and peripherals
I ² D	Integrated IC Data bus		
I ² S	Integrated IC Sound bus	PAL	Phase Alternating Line. Color system mainly used in West Europe (color carrier= 4.433619 MHz) and South America (color carrier PAL M= 3.575612 MHz and PAL N= 3.582056 MHz)
IB	In Band channel		
IF	Intermediate Frequency		
Interlaced	Scan mode where two fields are used to form one frame. Each field contains half the number of the total amount of lines. The fields are written in "pairs", causing line flicker.	PCB	Printed Circuit Board (same as "PWB")
IR	Infra Red	PCM	Pulse Code Modulation
IRQ	Interrupt Request	PCMCIA	Personal Computer Memory Card International Association
ITU-656	The ITU Radio communication Sector (ITU-R) is a standards body subcommittee of the International Telecommunication Union relating to radio communication. ITU-656 (a.k.a. SDI), is a digitized video format used for broadcast grade video. Uncompressed digital component or digital composite signals can be used. The SDI signal is self-synchronizing, uses 8 bit or 10 bit data words, and has a maximum data rate of 270 Mbit/s, with a minimum bandwidth of 135 MHz.	PDP	Plasma Display Panel
		PFC	Power Factor Corrector (or Pre-conditioner)
		PIP	Picture In Picture
		PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
		POD	Point Of Deployment: A removable CAM module, implementing the CA system for a host (e.g. a TV-set)
		POR	Power On Reset, signal to reset the uP
ITV	Institutional TeleVision; TV sets for hotels, hospitals etc.	Progressive Scan	Scan mode where all scan lines are displayed in one frame at the same time, creating a double vertical resolution.
JOP	Jaguar Output Processor	PSIP	Program and System Information Protocol: A standard for (broadcast) digital television. PSIP consists of channel mapping data, program guide data, information about closed captions and content advisory ratings, and other data related to the current and future programs.
LS	Last Status; The settings last chosen by the customer and read and stored in RAM or in the NVM. They are called at start-up of the set to configure it according to the customer's preferences		
LATAM	Latin America		
LCD	Liquid Crystal Display	PTC	Positive Temperature Coefficient, non-linear resistor
LED	Light Emitting Diode		
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I	PWB	Printed Wiring Board (same as "PCB")
		PWM	Pulse Width Modulation
LORE	LOcal REgression approximation noise reduction	QAM	Quadrature Amplitude Modulation; modulation method
LPL	LG.Philips LCD (supplier)	QTNR	Quality Temporal Noise Reduction
LS	Loudspeaker	QVCP	Quality Video Composition Processor
LVDS	Low Voltage Differential Signalling	RAM	Random Access Memory
Mbps	Mega bits per second	RGB	Red, Green, and Blue. The primary color signals for TV. By mixing levels of R, G, and B, all colors (Y/C) are reproduced.
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz		
MOP	Matrix Output Processor	RC	Remote Control
MOSFET	Metal Oxide Silicon Field Effect Transistor, switching device	RC5 / RC6	Signal protocol from the remote control receiver
MPEG	Motion Pictures Experts Group	RESET	RESET signal
MPIF	Multi Platform InterFace	ROM	Read Only Memory
MUTE	MUTE Line	R-TXT	Red Teletext
NC	Not Connected	SAM	Service Alignment Mode
NICAM	Near Instantaneous Compounded Audio Multiplexing. This is a digital sound system, mainly used in Europe.	S/C	Short Circuit
		SCART	Syndicat des Constructeurs d'Appareils Radiorecepteurs et Televisieurs
NTC	Negative Temperature Coefficient, non-linear resistor	SCL	Serial Clock I ² C
NTSC	National Television Standard Committee. Color system mainly used in North America and Japan. Color carrier NTSC M/N= 3.579545 MHz, NTSC 4.43= 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)	SCL-F	CLock Signal on Fast I ² C bus
		SD	Standard Definition
		SDA	Serial Data I ² C
		SDA-F	DAta Signal on Fast I ² C bus
		SDI	Serial Digital Interface, see "ITU-656"
NVM	Non-Volatile Memory: IC containing TV related data such as alignments	SDRAM	Synchronous DRAM
		SECAM	SEquence Couleur Avec Memoire. Color system mainly used in France and East Europe. Color carriers= 4.406250 MHz and 4.250000 MHz
O/C	Open Circuit		
OOB	Out Of Band channel	SIF	Sound Intermediate Frequency
OSD	On Screen Display	SMPS	Switched Mode Power Supply

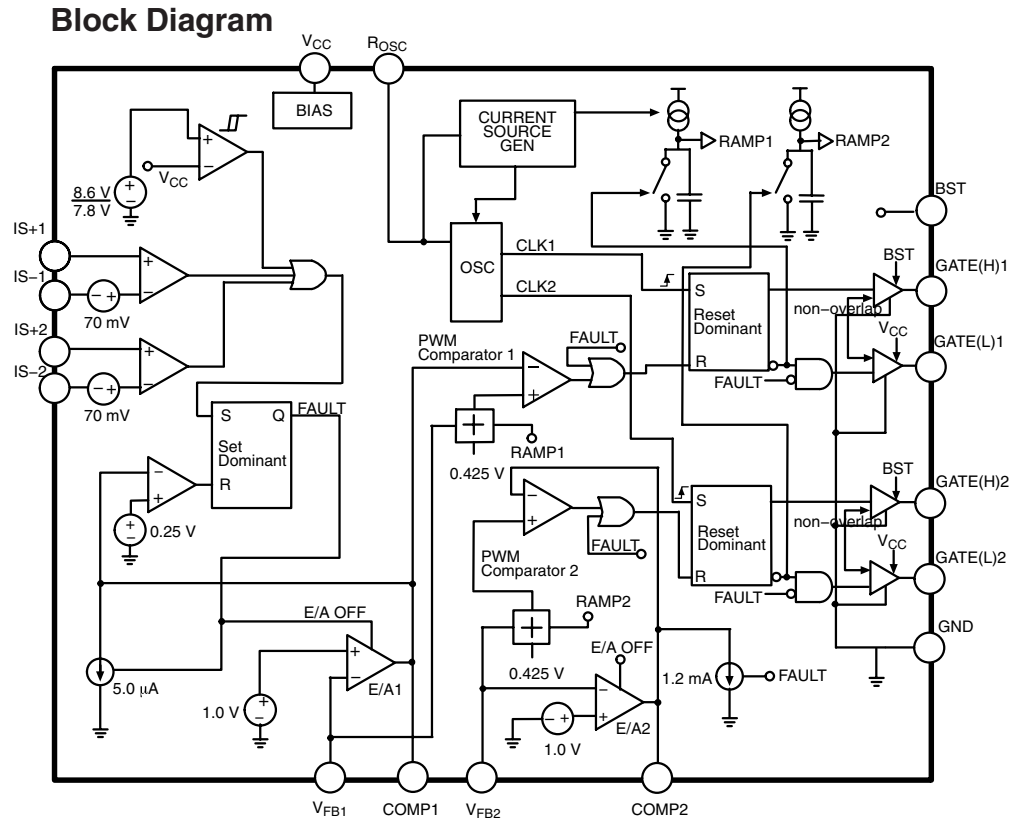
SOG	Sync On Green
SOPS	Self Oscillating Power Supply
S/PDIF	Sony Philips Digital InterFace
SRAM	Static RAM
SSB	Small Signal Board
STBY	STandBY
SOG	Sync On Green
SVGA	800x600 (4:3)
SVHS	Super Video Home System
SW	Software
SWAN	Spatial temporal Weighted Averaging Noise reduction
SXGA	1280x1024
TFT	Thin Film Transistor
THD	Total Harmonic Distortion
TMDs	Transmission Minimized Differential Signalling
TXT	TeleteXT
TXT-DW	Dual Window with TeleteXT
uP	Microprocessor
UXGA	1600x1200 (4:3)
V	V-sync to the module
VCR	Video Cassette Recorder
VESA	Video Electronics Standards Association
VGA	640x480 (4:3)
VL	Variable Level out: processed audio output toward external amplifier
VSb	Vestigial Side Band; modulation method
WYSIWYR	What You See Is What You Record: record selection that follows main picture and sound
WXGA	1280x768 (15:9)
XTAL	Quartz crystal
XGA	1024x768 (4:3)
Y	Luminance signal
Y/C	Luminance (Y) and Chrominance (C) signal
YPbPr	Component video. Luminance and scaled color difference signals (B-Y and R-Y)
YUV	Component video

9.17 IC Data Sheets

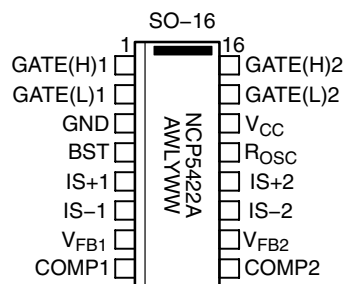
electrical diagrams (with the exception of "memory" and "logic" ICs).

This section shows the internal block diagrams and pin configurations of ICs that are drawn as "black boxes" in the

9.17.1 Diagram B1A, NCP5422AD (IC 7U00)



Pin Configuration



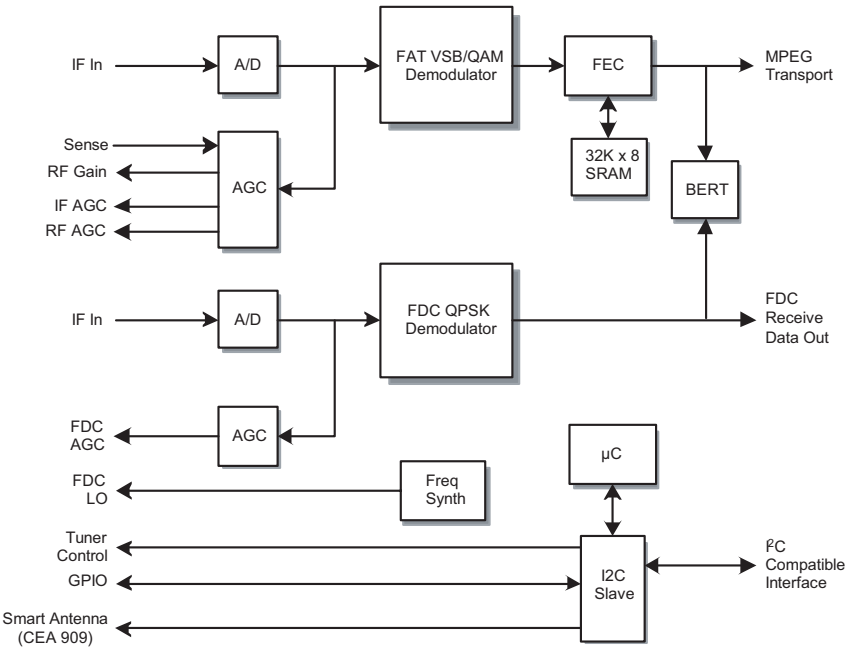
A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week

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Figure 9-30 Internal block diagram and pin configuration

9.17.2 Diagram B2A, NXT2003 (IC 7TG0)

Block Diagram



Pin Configuration

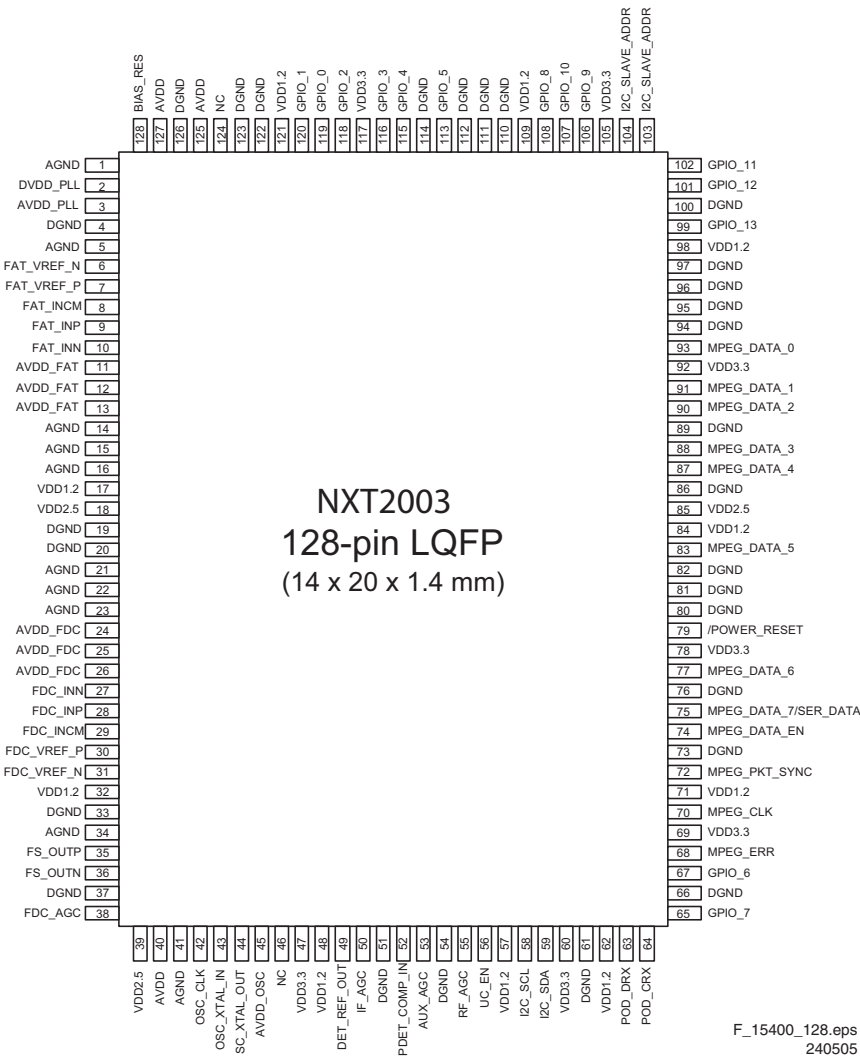
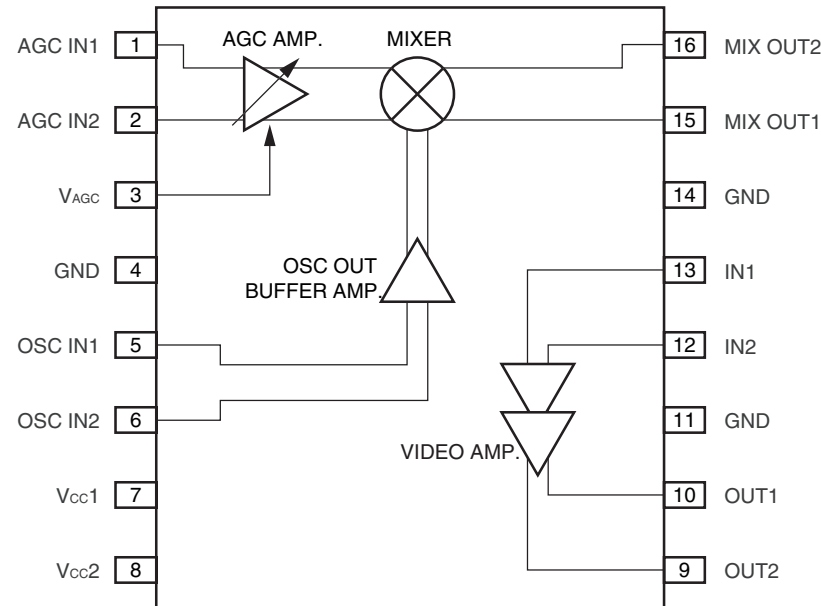


Figure 9-31 Internal block diagram and pin configuration

9.17.3 Diagram B2B, UPC3220GR (IC 7T43)

Block Diagram and Pin Configuration

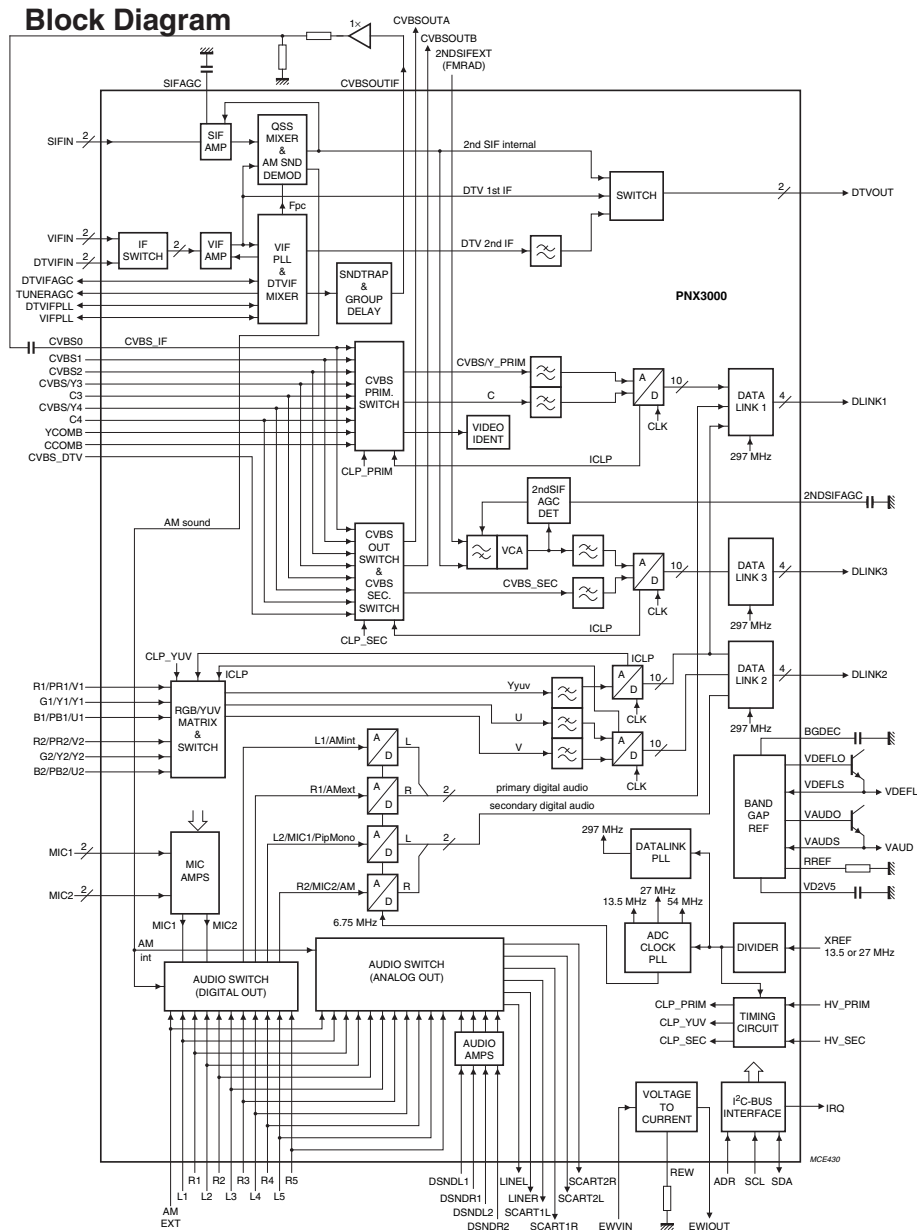
(Top View)



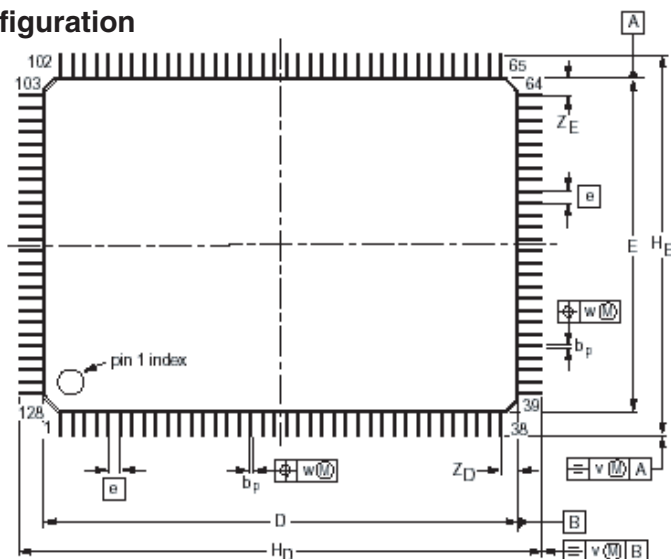
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Figure 9-32 Internal block diagram and pin configuration

Block Diagram

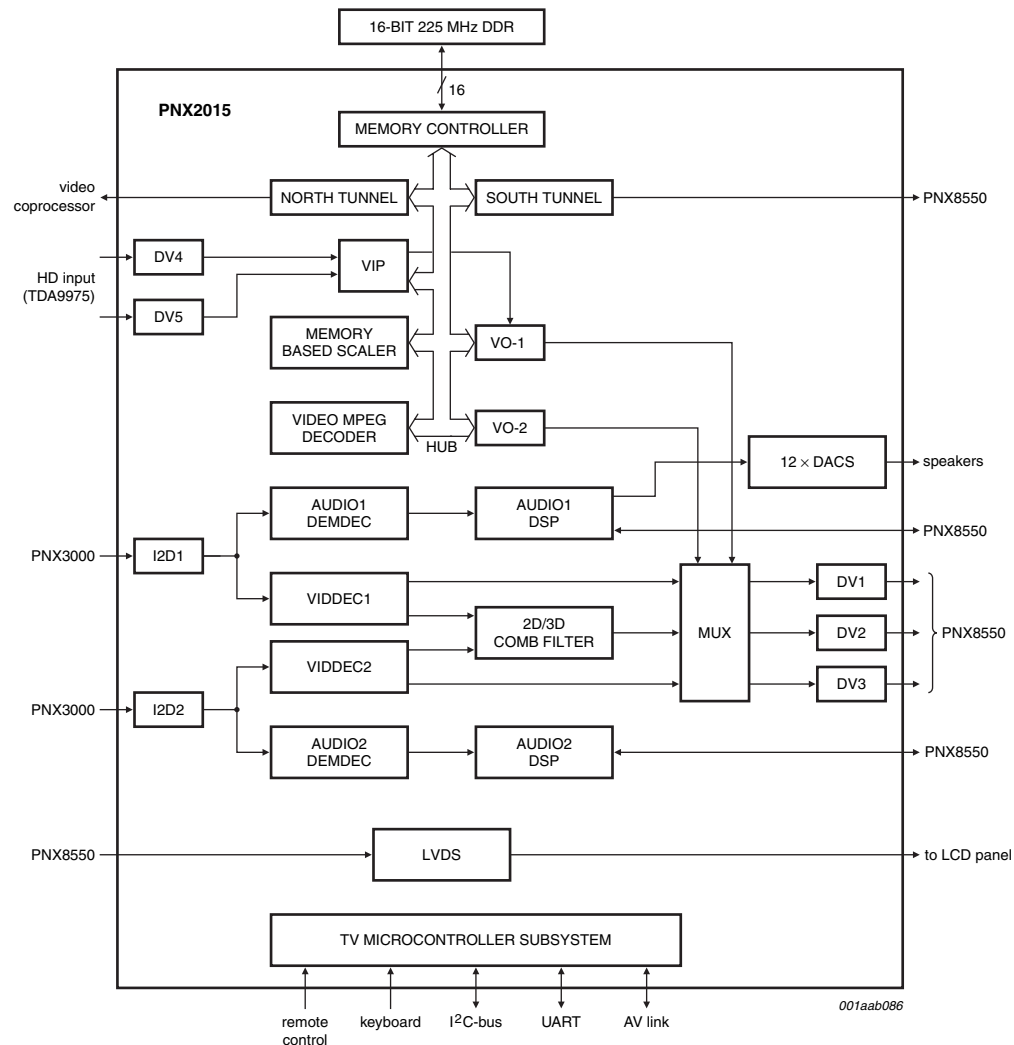


Pin Configuration

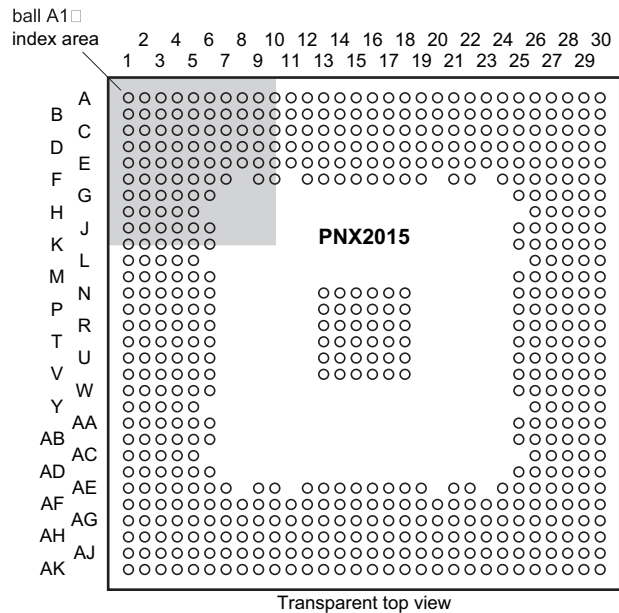


9.17.5 Diagram B4x, PNX2015E (IC 7J00)

Block Diagram



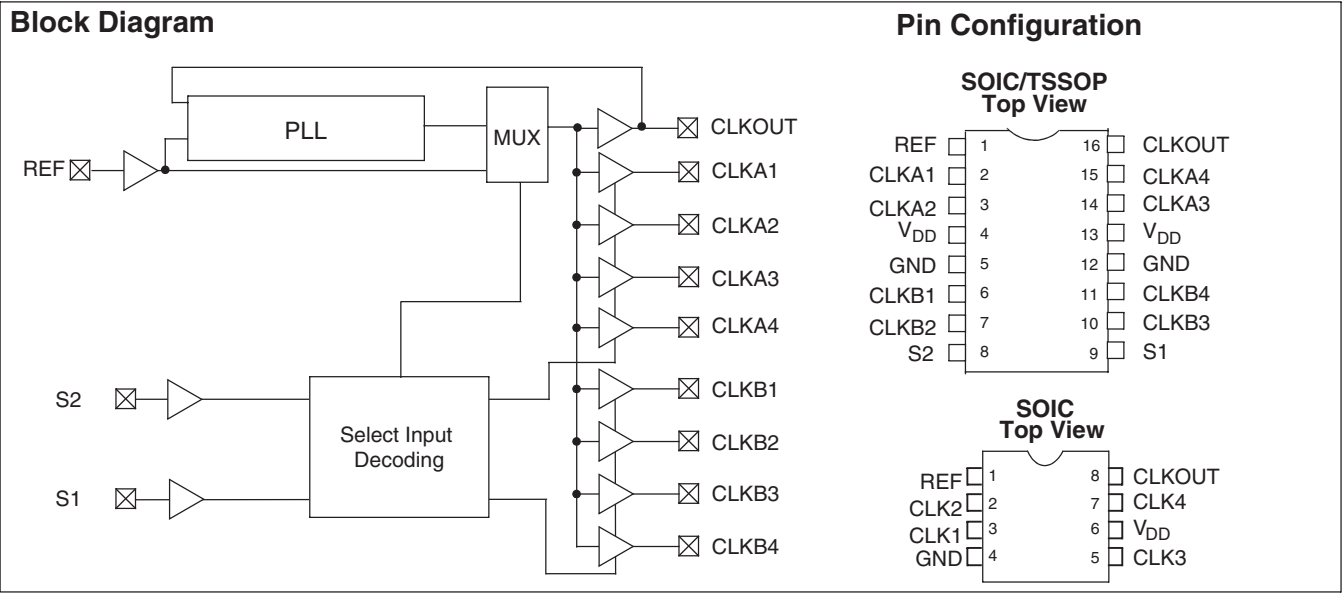
Pin Configuration



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Figure 9-34 Internal block diagram and pin configuration

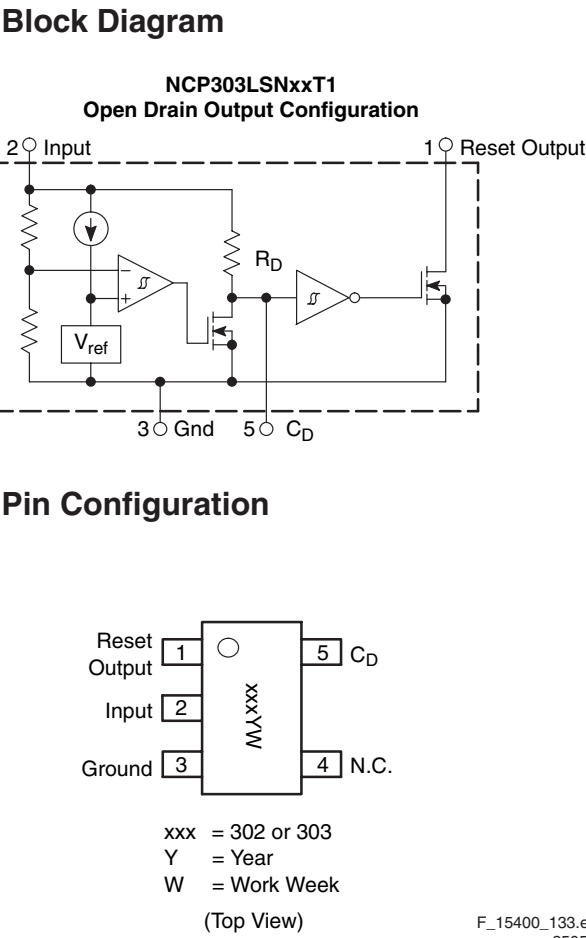
9.17.6 Diagram B4A, CY2305SC-1 (IC 7J08)



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200804

Figure 9-35 Internal block diagram and pin configuration

9.17.7 Diagram B4E, NCP303LSN (IC 7LB0 - 7LB4)

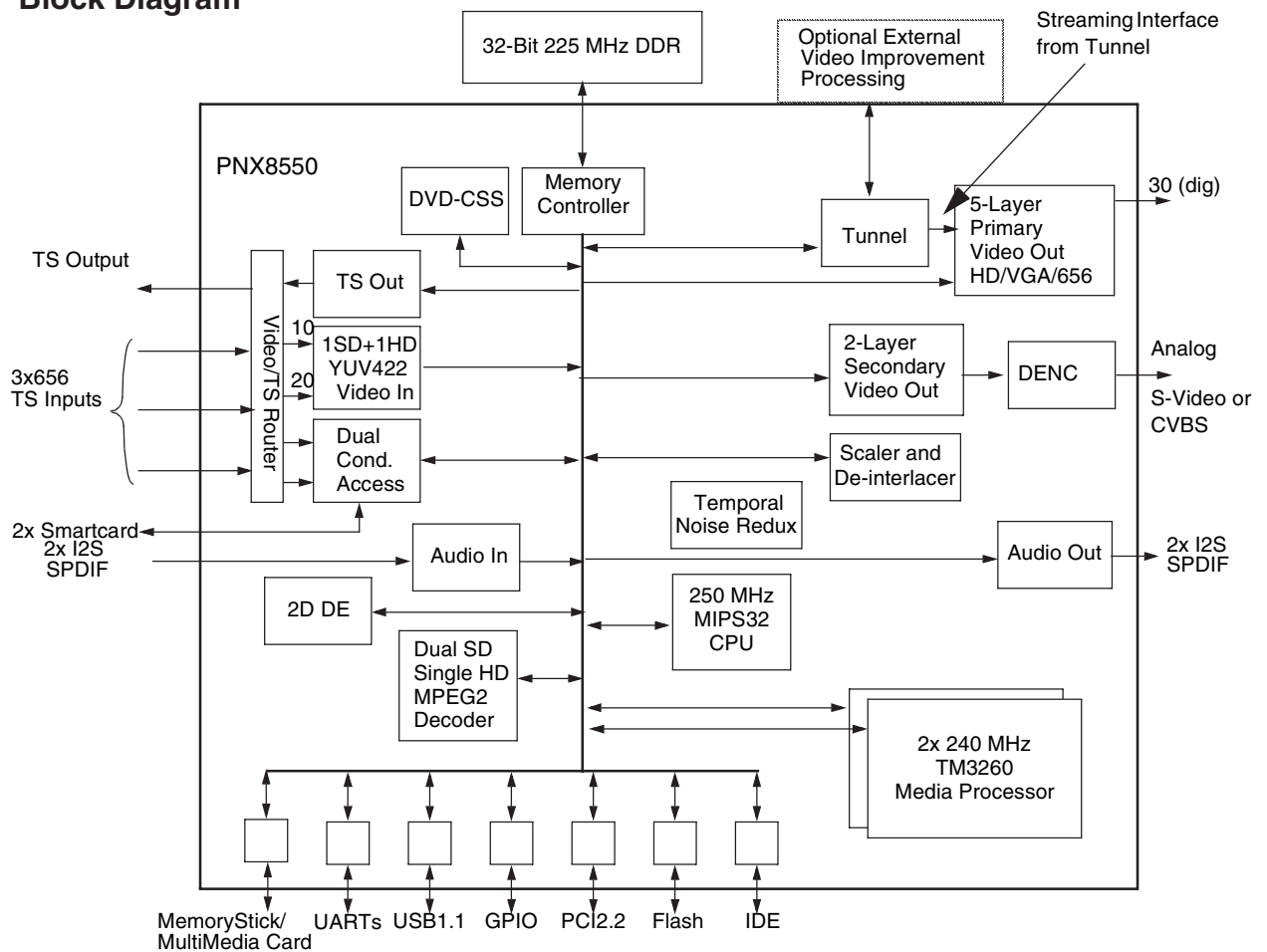


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Figure 9-36 Internal block diagram and pin configuration

9.17.8 Diagram B5x, PNX8550EH (IC 7V00)

Block Diagram



Pin Configuration

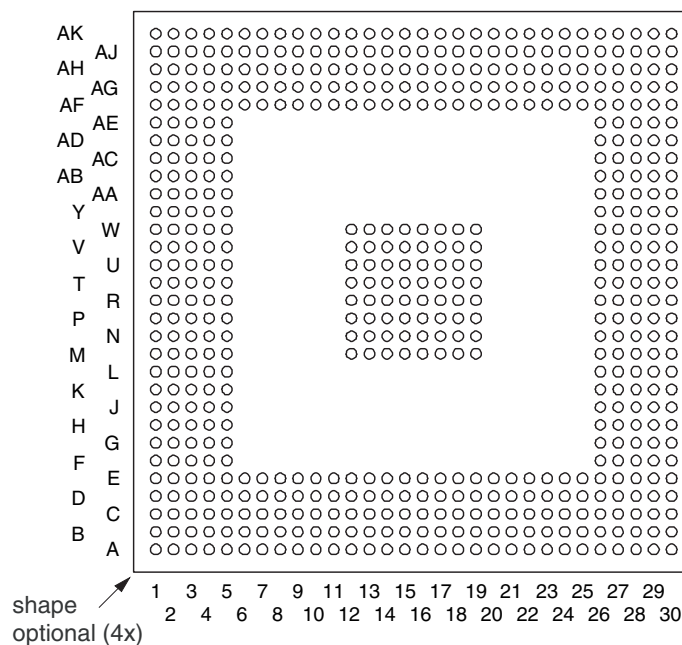
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Figure 9-37 Internal block diagram and pin configuration

9.17.9 Diagram B5A, LM3526MX (IC 7Q01)

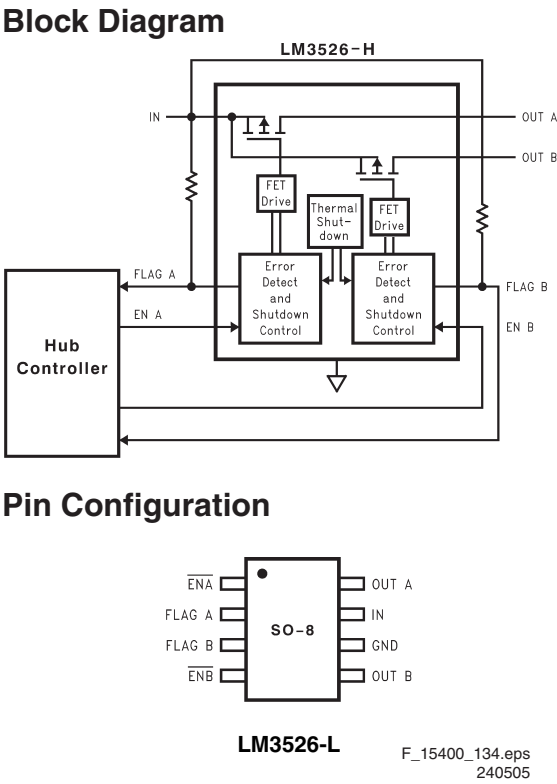
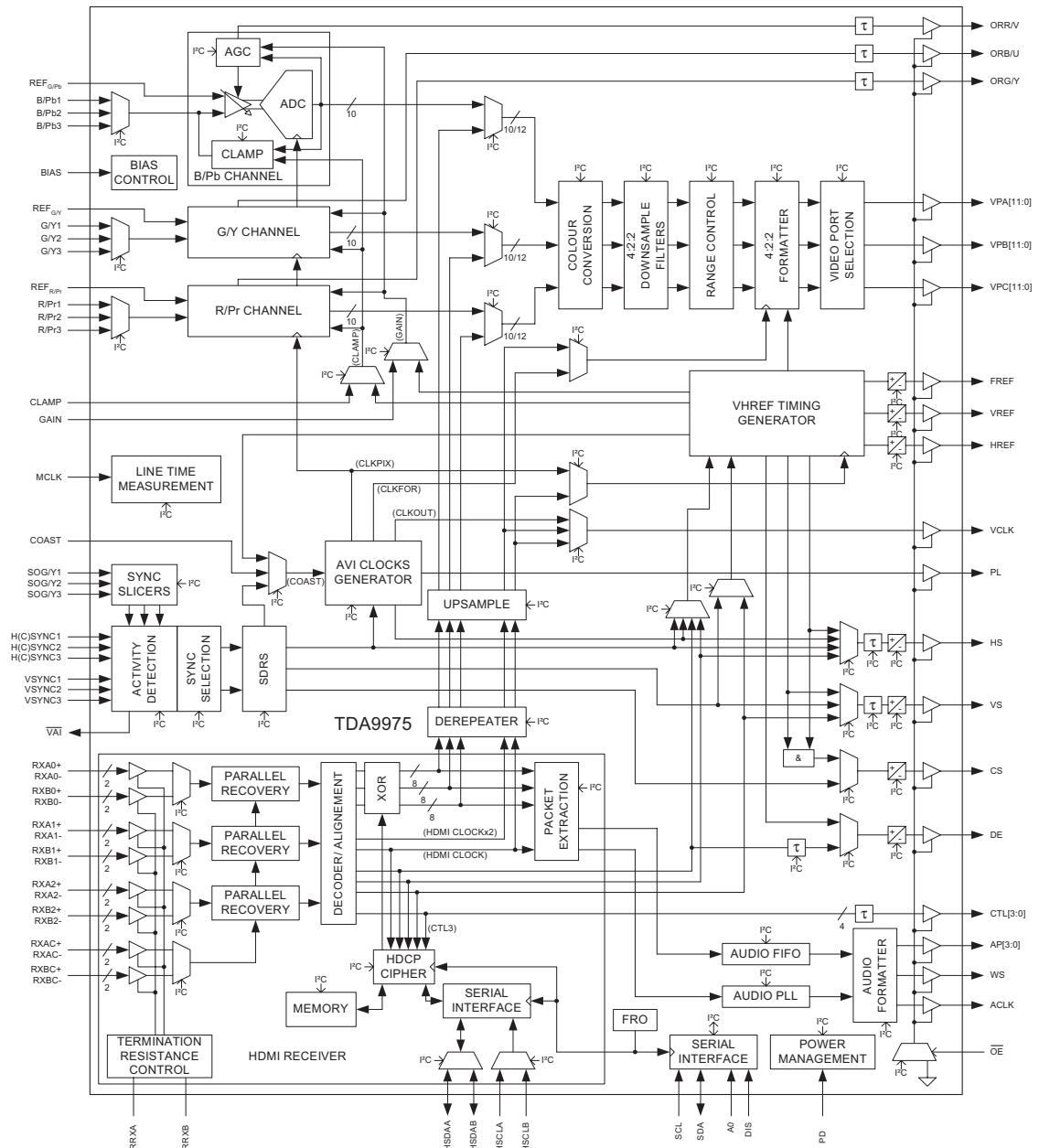


Figure 9-38 Internal block diagram and pin configuration

9.17.10 Diagram B7B & B7C, TDA9975EL (IC 7B11)

Block Diagram



Pin Configuration

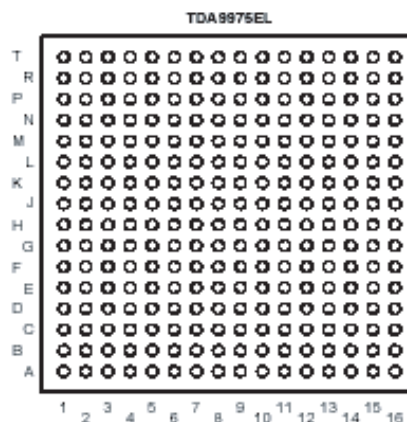
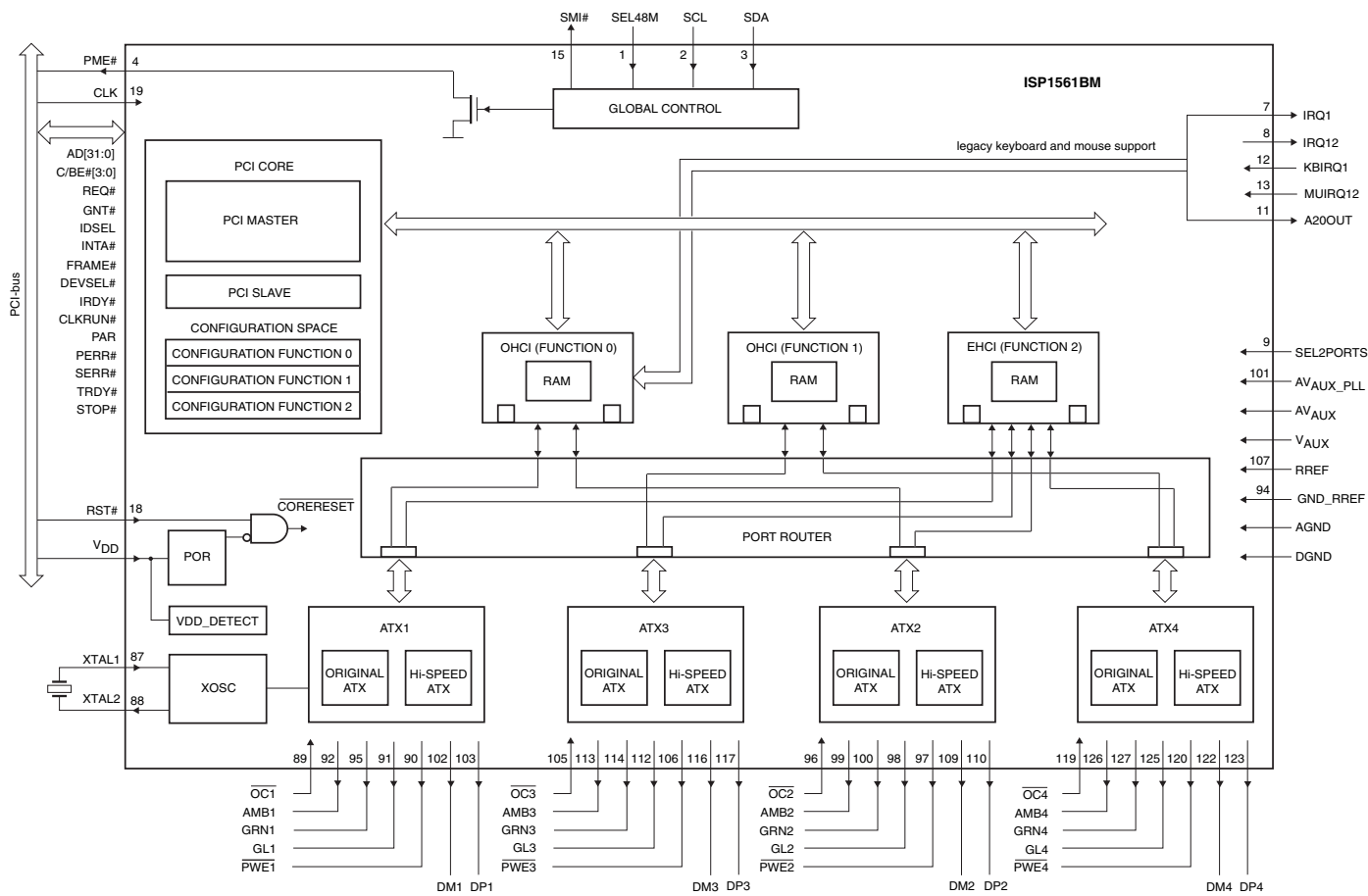
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Figure 9-39 Internal block diagram and pin configuration

9.17.11 Diagram B8, ISP1561BM (IC 7N00)

Block Diagram



Pin Configuration

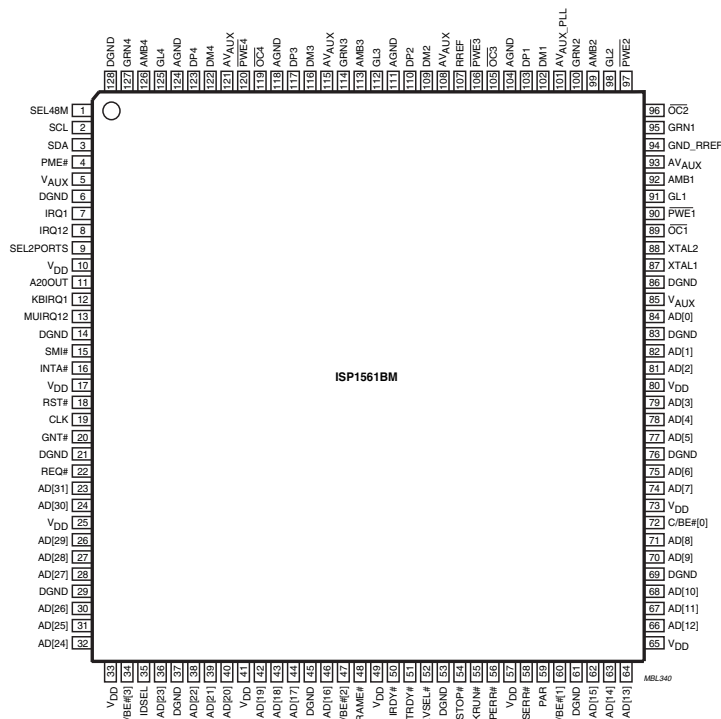
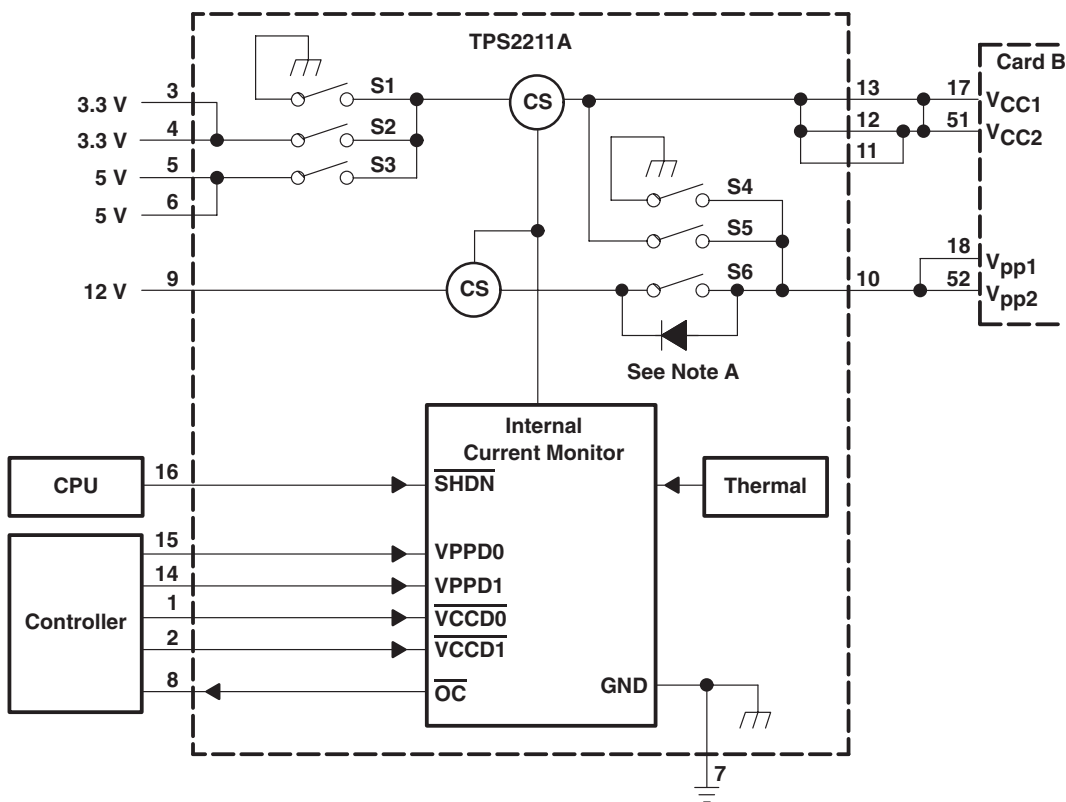


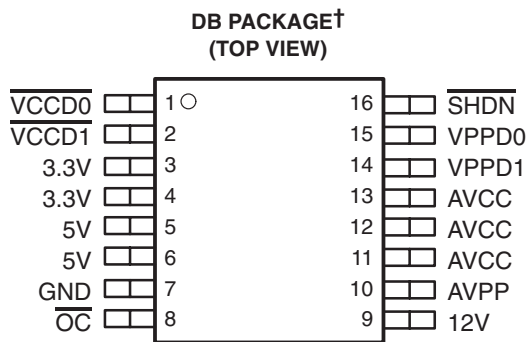
Figure 9-40 Internal block diagram and pin configuration

9.17.12 Diagram B10A, TPS2211AIDB (IC 7P00)

Block Diagram



Pin Configuration

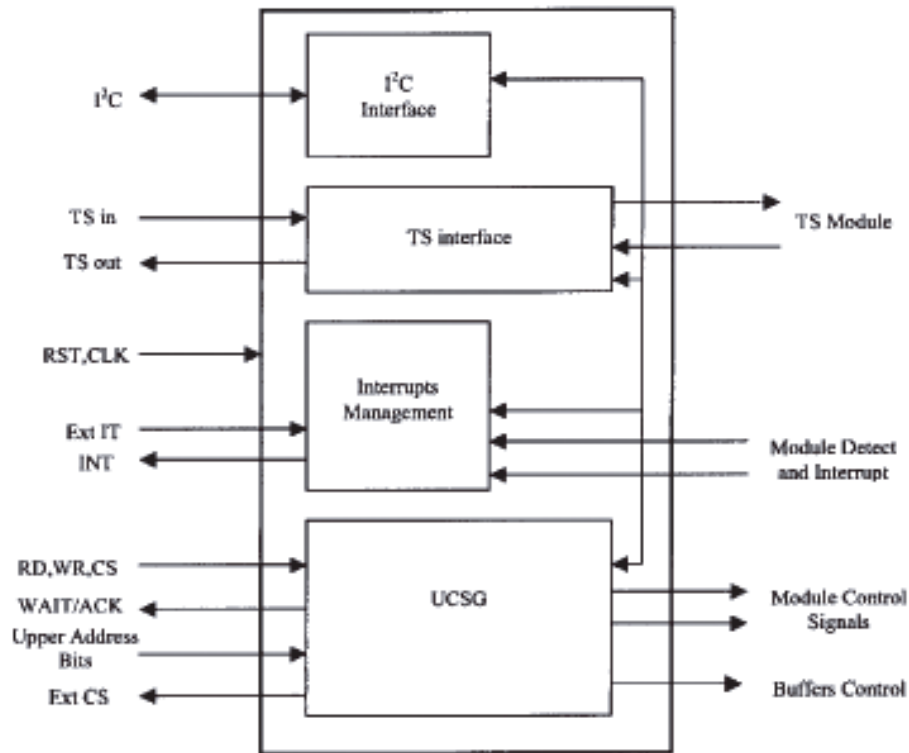


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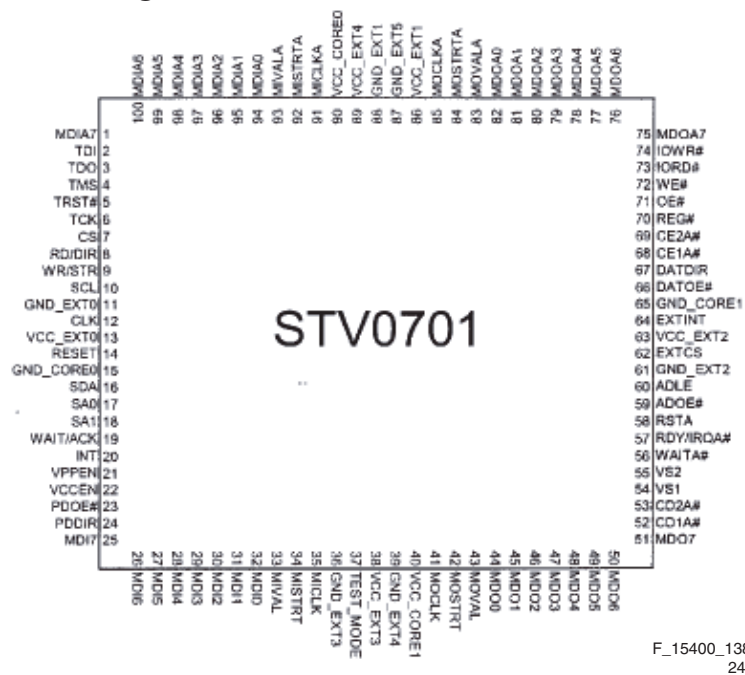
Figure 9-41 Internal block diagram and pin configuration

9.17.13 Diagram B10A, STV0701 (IC 7P03)

Block Diagram



Pin Configuration

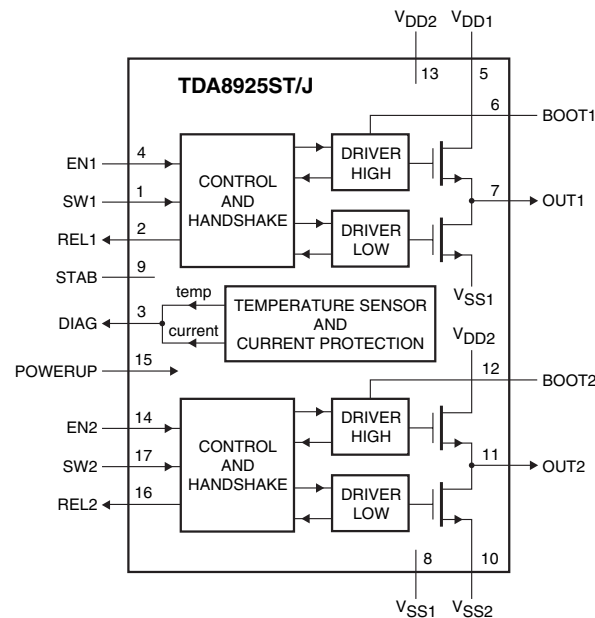


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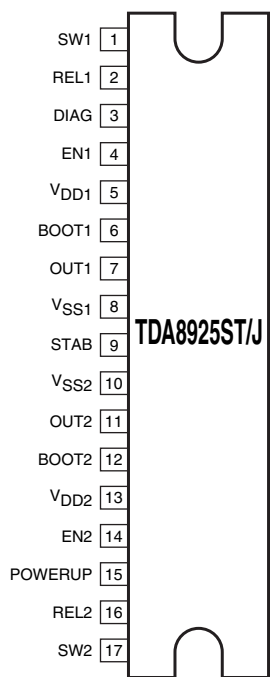
Figure 9-42 Internal block diagram and pin configuration

9.17.14 Diagram C, TDA8925ST (IC 7701)

Block Diagram



Pin Configuration



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Figure 9-43 Internal block diagram and pin configuration

10. Spare Parts List

Set Level								
Various								
0180	3104 328 35431	Cardreader assy	3030	3198 031 04720	4.7kΩ 5% 0402	1U01▲	2422 086 00623	Fuse 3A T 125V
1004▲	9322 225 38682	PDP S42AX-YD01	3031	3198 031 04720	4.7kΩ 5% 0402	1U04▲	2422 086 00623	Fuse 3A T 125V
1004▲	9322 226 54682	PDP S50HW-XD04	3042	4822 053 20105	1MΩ 5% 0.25W	8140	3104 311 10451	Cable FFC 40p/120/40p
1012	3104 328 36781	LED panel assy [J]	3999	4822 051 30103	10kΩ 5% 0.062W	8162	3104 311 10461	Cable FFC 20p/180/20p
1014	3104 328 36671	Control assy [E]				8321	3104 311 08731	Cable POSI/100/POSI
1064	3104 328 39552	Ambil. inverter assy [AL]				8364	3104 311 09871	Cable 4p/220/4p
1066	3104 328 39552	Ambil. inverter assy [AL]						
1101	See table 5-4	SSB w. security keys [B]						
1116	3104 328 39821	Side I/O assy [D]						
1175	2722 171 00256	Ambilight 500R (42")						
1175	2722 171 00262	Ambilight 600R (50")						
1176	2722 171 00258	Ambilight 500L (42")						
1176	2722 171 00264	Ambilight 600L (50")						
8101	3104 311 10561	Cable 3p/1200/3p						
8101	3104 311 10911	Cable 3p/1400/3p						
8102	3104 311 07241	Cable 7p/1000/7p						
8103	3104 311 07391	Cable 10p/220/10p						
8103	3104 311 10981	Cable 10p/280/10p Ferr.						
8108	3104 311 10531	Cable 4p/1400/4p						
8110	3104 311 10712	Cable 4p/1000/4p						
8110	3104 311 10851	Cable 4p/1300/4p						
8120	3104 311 07291	Cable 12p/820/12p						
8136	3104 311 10733	Cable 11p/1000/11p						
8146	3104 311 08621	Cable 11p/220/11p						
8148	3104 311 10521	Cable 3p/1400/3p						
8149	3104 311 10722	Cable 4p/1000/4p						
8149	3104 311 10861	Cabl 4p/1300/4p						
8150	3104 311 08841	Cable 31p/220/31p						
8152	3104 311 07941	Cable 9p/820/9p						
8735	3104 311 10601	Cable 2p3/1400/Posi						
8736	3104 311 10591	Cable 2p3/1000/Posi						
8900	3104 311 07911	Cable ring/180/ring						
Ambilight Inverter Panel [AL]								
Various								
0615	3104 317 09401	SW (see Prod. Survey)						
1010	2422 086 00657	Fuse 3A 125V F SMD						
1050	2422 543 01431	Xtal 20MHz 16pF						
1M08	2422 025 09406	Connector 4p m						
1M10	2422 025 09406	Connector 4p m						
1M11	2422 025 19068	Connector 11p m						
1M12	2422 025 19069	Connector 3p m						
1M48	2422 025 10768	Connector 3p m						
1M49	2422 025 18884	Connector 4p m						
2001	2020 012 00018	1000μF 20% 16V						
2002	2238 586 59812	100nF 20% 50V 0603						
2003	2020 552 96618	1nF 10% 50V 0402						
2004	2020 552 96618	1nF 10% 50V 0402						
2005	3198 034 01590	15pF 1% 50V 0402						
2006	3198 034 01590	15pF 1% 50V 0402						
3003	4822 117 13596	220Ω 5% 0.01W 0402						
3004	4822 051 20471	470Ω 5% 0.1W						
3005	4822 051 20561	560Ω 5% 0.1W						
3006	2322 762 60102	1kΩ 5% 2512						
3007	2322 762 60102	1kΩ 5% 2512						
3008	4822 051 20471	470Ω 5% 0.1W						
3009	4822 051 20561	560Ω 5% 0.1W						
3010	2322 762 60102	1kΩ 5% 2512						
3011	2322 762 60102	1kΩ 5% 2512						
3012	4822 051 20471	470Ω 5% 0.1W						
3013	4822 051 20561	560Ω 5% 0.1W						
3014	2322 762 60102	1kΩ 5% 2512						
3015	2322 762 60102	1kΩ 5% 2512						
3016	3198 031 04720	4.7kΩ 5% 0402						
3017	3198 031 04720	4.7kΩ 5% 0402						
3018	3198 031 04720	4.7kΩ 5% 0402						
3019	3198 031 04720	4.7kΩ 5% 0402						
3020	3198 031 04720	4.7kΩ 5% 0402						
3022	4822 117 13545	100Ω 1% 0402						
3023	4822 117 13545	100Ω 1% 0402						
3024	3198 031 04720	4.7kΩ 5% 0402						
3025	3198 031 04720	4.7kΩ 5% 0402						
3028	4822 117 13606	10kΩ 5% 0.01W 0402						
3029	3198 031 04720	4.7kΩ 5% 0402						

2B64	2238 586 59812	100nF 20% 50V 0603	2G37	2238 586 59812	100nF 20% 50V 0603	2LA1	4822 126 14519	22pF 5% 50V 0402
2B67	4822 124 11131	47µF 6.3V	2G38	2238 586 59812	100nF 20% 50V 0603	2LA2	2238 869 15109	10pF 5% 50V 0402
2B69	2238 586 59812	100nF 20% 50V 0603	2G39	2238 586 59812	100nF 20% 50V 0603	2LA4	2238 586 59812	100nF 20% 50V 0603
2B77	2238 586 59812	100nF 20% 50V 0603	2G40	2238 586 59812	100nF 20% 50V 0603	2LA5	3198 035 03320	3.3nF 5% 50V 0402
2B79	2238 586 59812	100nF 20% 50V 0603	2G41	2022 552 05679	1µF 10% 16V 0805	2LA6	3198 035 03320	3.3nF 5% 50V 0402
2B80	2238 586 59812	100nF 20% 50V 0603	2G42	2020 552 96618	1nF 10% 50V 0402	2LA7	3198 035 03320	3.3nF 5% 50V 0402
2B81	2238 586 59812	100nF 20% 50V 0603	2G43	2238 586 59812	100nF 20% 50V 0603	2LA8	3198 035 03320	3.3nF 5% 50V 0402
2B89	5322 126 11583	10nF 10% 50V 0603	2G44	2020 552 96628	10nF 10% 16V 0402	2LA9	3198 035 03320	3.3nF 5% 50V 0402
2B90	4822 124 81058	47µF 20% 4V	2H00	2238 586 59812	100nF 20% 50V 0603	2LB0	2238 586 59812	100nF 20% 50V 0603
2B92	2238 586 59812	100nF 20% 50V 0603	2H01	2238 586 59812	100nF 20% 50V 0603	2LB1	2238 586 59812	100nF 20% 50V 0603
2BA0	2020 552 96628	10nF 10% 16V 0402	2H02	2238 586 59812	100nF 20% 50V 0603	2LB3	2020 552 96618	1nF 10% 50V 0402
2BA1	3198 035 14720	4.7nF 5% 25V 0402	2H03	2238 586 59812	100nF 20% 50V 0603	2LB4	2238 586 59812	100nF 20% 50V 0603
2BA2	2020 552 96628	10nF 10% 16V 0402	2H06	2020 552 96618	1nF 10% 50V 0402	2LN2	4822 124 81058	47µF 20% 4V
2BA3	3198 035 14720	4.7nF 5% 25V 0402	2H07	2020 552 96618	1nF 10% 50V 0402	2LN3	2238 586 59812	100nF 20% 50V 0603
2BA4	3198 034 01580	1.5pF 1% 50V 0402	2H08	3198 034 02790	47pF 1% 50V 0402	2LN4	2238 586 59812	100nF 20% 50V 0603
2BA5	3198 034 01580	1.5pF 1% 50V 0402	2H09	3198 034 02790	47pF 1% 50V 0402	2LN5	2238 586 59812	100nF 20% 50V 0603
2BA6	3198 034 01580	1.5pF 1% 50V 0402	2H12	3198 034 02790	47pF 1% 50V 0402	2LN6	2238 586 59812	100nF 20% 50V 0603
2BA7	3198 034 01580	1.5pF 1% 50V 0402	2J01	2238 586 59812	100nF 20% 50V 0603	2LN7	2238 586 59812	100nF 20% 50V 0603
2BA8	3198 034 01580	1.5pF 1% 50V 0402	2J03	2238 586 59812	100nF 20% 50V 0603	2LN8	2238 586 59812	100nF 20% 50V 0603
2BA9	3198 034 01580	1.5pF 1% 50V 0402	2J06	2238 586 59812	100nF 20% 50V 0603	2LP0	4822 124 12108	100µF 20% 4V
2C01	2238 787 15641	22nF 5% 16V 0402	2J08	2238 586 59812	100nF 20% 50V 0603	2LP2	2238 586 59812	100nF 20% 50V 0603
2C02	2238 787 15641	22nF 5% 16V 0402	2J10	2238 586 59812	100nF 20% 50V 0603	2LP3	2238 586 59812	100nF 20% 50V 0603
2C04	2238 787 15641	22nF 5% 16V 0402	2J13	2238 586 59812	100nF 20% 50V 0603	2LP4	2238 586 59812	100nF 20% 50V 0603
2C05	2238 787 15641	22nF 5% 16V 0402	2J16	2238 586 59812	100nF 20% 50V 0603	2LP7	4822 124 12108	100µF 20% 4V
2C06	2238 787 15641	22nF 5% 16V 0402	2J18	2238 586 59812	100nF 20% 50V 0603	2LP8	2238 586 59812	100nF 20% 50V 0603
2C07	2238 787 15641	22nF 5% 16V 0402	2J20	2238 586 59812	100nF 20% 50V 0603	2LP9	2238 586 59812	100nF 20% 50V 0603
2C08	2238 787 15641	22nF 5% 16V 0402	2J22	3198 035 03320	3.3nF 5% 50V 0402	2LR0	2238 586 59812	100nF 20% 50V 0603
2C09	2238 787 15641	22nF 5% 16V 0402	2J23	3198 035 03320	3.3nF 5% 50V 0402	2LR2	2238 586 59812	100nF 20% 50V 0603
2C11	2238 787 15641	22nF 5% 16V 0402	2J24	3198 035 03320	3.3nF 5% 50V 0402	2LR4	2238 586 59812	100nF 20% 50V 0603
2C14	2238 787 15641	22nF 5% 16V 0402	2J25	3198 035 03320	3.3nF 5% 50V 0402	2LR5	2238 586 59812	100nF 20% 50V 0603
2C15	2238 787 15641	22nF 5% 16V 0402	2J37	2020 552 96628	10nF 10% 16V 0402	2LR6	2238 586 59812	100nF 20% 50V 0603
2C16	2238 787 15641	22nF 5% 16V 0402	2J40	2238 869 15109	10pF 5% 50V 0402	2LR8	2238 586 59812	100nF 20% 50V 0603
2C17	2238 787 15641	22nF 5% 16V 0402	2J41	2238 869 15109	10pF 5% 50V 0402	2LR9	2238 586 59812	100nF 20% 50V 0603
2C18	2238 787 15641	22nF 5% 16V 0402	2J42	2238 869 15109	10pF 5% 50V 0402	2LS5	2238 586 59812	100nF 20% 50V 0603
2C19	2238 787 15641	22nF 5% 16V 0402	2J43	2238 869 15109	10pF 5% 50V 0402	2LT0	2022 552 05679	1µF 10% 16V 0805
2C20	2238 787 15641	22nF 5% 16V 0402	2J44	2238 869 15109	10pF 5% 50V 0402	2LT1	2238 586 59812	100nF 20% 50V 0603
2C22	2238 787 15641	22nF 5% 16V 0402	2J45	2238 869 15109	10pF 5% 50V 0402	2LT2	2238 586 59812	100nF 20% 50V 0603
2C23	2238 787 15641	22nF 5% 16V 0402	2J46	2238 869 15109	10pF 5% 50V 0402	2LT3	2238 586 59812	100nF 20% 50V 0603
2C27	2238 586 59812	100nF 20% 50V 0603	2J47	2238 869 15109	10pF 5% 50V 0402	2LT4	2238 586 59812	100nF 20% 50V 0603
2C28	2238 586 59812	100nF 20% 50V 0603	2J48	2238 869 15109	10pF 5% 50V 0402	2LT5	2238 586 59812	100nF 20% 50V 0603
2C31	2238 586 59812	100nF 20% 50V 0603	2J49	2238 869 15109	10pF 5% 50V 0402	2LT6	2238 586 59812	100nF 20% 50V 0603
2C32	2020 004 90283	10µF 20% 10V 1206	2J67	2238 869 15101	100pF 5% 50V 0402	2M90	2238 586 59812	100nF 20% 50V 0603
2C33	2238 586 59812	100nF 20% 50V 0603	2J68	2238 869 15101	100pF 5% 50V 0402	2M91	2020 552 96628	10nF 10% 16V 0402
2C34	2022 552 05679	1µF 10% 16V 0805	2J72	2238 869 15109	10pF 5% 50V 0402	2M92	2020 004 90283	10µF 20% 10V 1206
2C35	2238 586 59812	100nF 20% 50V 0603	2J73	2238 869 15109	10pF 5% 50V 0402	2M93	2020 552 96628	10nF 10% 16V 0402
2C36	2022 552 05679	1µF 10% 16V 0805	2K40	2238 586 59812	100nF 20% 50V 0603	2M94	2020 004 90283	10µF 20% 10V 1206
2C37	2022 552 05679	1µF 10% 16V 0805	2K41	2238 586 59812	100nF 20% 50V 0603	2N00	4822 126 14324	33pF 5% 50V 0402
2C39	2238 586 59812	100nF 20% 50V 0603	2K43	2238 586 59812	100nF 20% 50V 0603	2N01	4822 126 14324	33pF 5% 50V 0402
2C40	2238 586 59812	100nF 20% 50V 0603	2K45	2238 586 59812	100nF 20% 50V 0603	2N02	2238 586 59812	100nF 20% 50V 0603
2C42	4822 126 14519	22pF 5% 50V 0402	2K46	2022 552 05679	1µF 10% 16V 0805	2N03	2238 586 59812	100nF 20% 50V 0603
2C43	4822 124 12108	100µF 20% 4V	2K47	2022 552 05679	1µF 10% 16V 0805	2N04	2238 586 59812	100nF 20% 50V 0603
2C44	2238 586 59812	100nF 20% 50V 0603	2K58	2022 552 05679	1µF 10% 16V 0805	2N05	2238 586 59812	100nF 20% 50V 0603
2C45	2020 004 90283	10µF 20% 10V 1206	2K60	2022 552 05679	1µF 10% 16V 0805	2N06	2238 586 59812	100nF 20% 50V 0603
2C46	2022 552 05679	1µF 10% 16V 0805	2K61	2022 552 05679	1µF 10% 16V 0805	2N07	2238 586 59812	100nF 20% 50V 0603
2C50	2020 552 96628	10nF 10% 16V 0402	2K63	2022 552 05679	1µF 10% 16V 0805	2N08	2238 586 59812	100nF 20% 50V 0603
2C52	4822 124 23002	10µF 16V	2K64	2022 552 05679	1µF 10% 16V 0805	2N09	2238 586 59812	100nF 20% 50V 0603
2C53	2020 552 96628	10nF 10% 16V 0402	2K65	2022 552 05679	1µF 10% 16V 0805	2N10	2238 586 59812	100nF 20% 50V 0603
2C55	2238 586 59812	100nF 20% 50V 0603	2K67	2022 552 05679	1µF 10% 16V 0805	2N11	2238 586 59812	100nF 20% 50V 0603
2C57	2020 552 96628	10nF 10% 16V 0402	2K68	2022 552 05679	1µF 10% 16V 0805	2N12	2020 552 96455	22nF 10% 16V 0402
2C58	2020 552 96628	10nF 10% 16V 0402	2K75	2022 552 05679	1µF 10% 16V 0805	2N13	2020 552 96455	22nF 10% 16V 0402
2C60	2020 552 96628	10nF 10% 16V 0402	2K76	2022 552 05679	1µF 10% 16V 0805	2O50	2238 869 15101	100pF 5% 50V 0402
2C63	2238 586 59812	100nF 20% 50V 0603	2L01	2238 586 59812	100nF 20% 50V 0603	2O51	2238 869 15101	100pF 5% 50V 0402
2C65	2020 552 96628	10nF 10% 16V 0402	2L06	2238 586 59812	100nF 20% 50V 0603	2P02	2238 586 59812	100nF 20% 50V 0603
2C67	2022 552 05679	1µF 10% 16V 0805	2L07	2238 586 59812	100nF 20% 50V 0603	2P03	2238 586 59812	100nF 20% 50V 0603
2C68	2022 552 05679	1µF 10% 16V 0805	2L08	2238 586 59812	100nF 20% 50V 0603	2P04	2238 586 59812	100nF 20% 50V 0603
2C70	2020 552 96628	10nF 10% 16V 0402	2L50	2238 586 59812	100nF 20% 50V 0603	2P06	2238 586 59812	100nF 20% 50V 0603
2C75	2022 029 00632	330µF 20% 6.3V	2L51	2238 586 59812	100nF 20% 50V 0603	2P07	2238 586 59812	100nF 20% 50V 0603
2C78	2022 552 05679	1µF 10% 16V 0805	2L52	2238 586 59812	100nF 20% 50V 0603	2P09	2020 552 96618	1nF 10% 50V 0402
2C79	2022 552 05679	1µF 10% 16V 0805	2L53	2238 586 59812	100nF 20% 50V 0603	2P10	2238 586 59812	100nF 20% 50V 0603
2G10	4822 124 81058	47µF 20% 4V	2L54	2238 586 59812	100nF 20% 50V 0603	2P15	2238 586 59812	100nF 20% 50V 0603
2G11	2238 586 59812	100nF 20% 50V 0603	2L55	2238 586 59812	100nF 20% 50V 0603	2P16	2238 586 59812	100nF 20% 50V 0603
2G12	2238 586 59812	100nF 20% 50V 0603	2L56	2238 586 59812	100nF 20% 50V 0603	2P18	2238 586 59812	100nF 20% 50V 0603
2G13	2238 586 59812	100nF 20% 50V 0603	2L57	2238 586 59812	100nF 20% 50V 0603	2P19	2238 586 59812	100nF 20% 50V 0603
2G14	2238 586 59812	100nF 20% 50V 0603	2L58	2238 586 59812	100nF 20% 50V 0603	2P20	2238 586 59812	100nF 20% 50V 0603
2G15	2238 586 59812	100nF 20% 50V 0603	2L59	2238 586 59812	100nF 20% 50V 0603	2P22	2238 586 59812	100nF 20% 50V 0603
2G16	2238 586 59812	100nF 20% 50V 0603	2L60	2238 586 59812	100nF 20% 50V 0603	2P23	2238 586 59812	100nF 20% 50V 0603
2G17	2238 586 59812	100nF 20% 50V 0603	2L61	2020 552 96618	1nF 10% 50V 0402	2P24	2020 552 96628	10nF 10% 16V 0402
2G18	2238 586 59812	100nF 20% 50V 0603	2L62	2020 552 96618	1nF 10% 50V 0402	2P25	2020 552 96628	10nF 10% 16V 0402
2G19	2238 586 59812	100nF 20% 50V 0603	2L63	2238 869 15101	100pF 5% 50V 0402	2P31	2238 586 59812	100nF 20% 50V 0603
2G20	2238 586 59812	100nF 20% 50V 0603	2L64	2238 586 59812	100nF 20% 50V 0603</			

2Q02	4822 124 81058	47µF 20% 4V	2T21	2020 552 96628	10nF 10% 16V 0402	2U38	2238 586 59812	100nF 20% 50V 0603
2Q03	2020 552 96637	10µF 10% 6.3V 0805	2T23	2020 552 96628	10nF 10% 16V 0402	2U39	2238 869 15101	100pF 5% 50V 0402
2Q04	2238 586 59812	100nF 20% 50V 0603	2T24	2238 586 59812	100nF 20% 50V 0603	2U40	2022 552 05679	1µF 10% 16V 0805
2Q05	2238 586 59812	100nF 20% 50V 0603	2T25	2022 029 00646	470µF 20% 6.3V	2U41	2022 552 05679	1µF 10% 16V 0805
2Q06	2238 586 59812	100nF 20% 50V 0603	2T27	2020 552 96628	10nF 10% 16V 0402	2U45	2022 552 05635	22µF 10% 16V
2Q07	2238 586 59812	100nF 20% 50V 0603	2T28	2020 552 96628	10nF 10% 16V 0402	2U46	2022 552 05679	1µF 10% 16V 0805
2Q08	2238 586 59812	100nF 20% 50V 0603	2T30	3198 032 15190	100µF 20% 4V	2U47	2020 552 96618	1nF 10% 50V 0402
2Q09	2238 586 59812	100nF 20% 50V 0603	2T31	2238 586 59812	100nF 20% 50V 0603	2U50	2022 552 05679	1µF 10% 16V 0805
2Q10	2238 586 59812	100nF 20% 50V 0603	2T33	2238 586 59812	100nF 20% 50V 0603	2U55	2238 586 59812	100nF 20% 50V 0603
2Q11	2238 586 59812	100nF 20% 50V 0603	2T35	2238 586 59812	100nF 20% 50V 0603	2U58	2022 552 05679	1µF 10% 16V 0805
2Q12	2238 586 59812	100nF 20% 50V 0603	2T43	2022 552 05679	1µF 10% 16V 0805	2U72	2238 586 59812	100nF 20% 50V 0603
2Q13	2238 586 59812	100nF 20% 50V 0603	2T45	2020 552 96628	10nF 10% 16V 0402	2U73	2020 552 96618	1nF 10% 50V 0402
2Q14	2238 586 59812	100nF 20% 50V 0603	2T48	2020 552 96628	10nF 10% 16V 0402	2U85	3198 035 03320	3.3nF 5% 50V 0402
2Q15	2238 586 59812	100nF 20% 50V 0603	2T51	2020 552 96628	10nF 10% 16V 0402	2V00	2238 586 59812	100nF 20% 50V 0603
2Q16	2238 586 59812	100nF 20% 50V 0603	2T53	2020 552 96628	10nF 10% 16V 0402	2V01	2238 586 59812	100nF 20% 50V 0603
2Q17	2238 586 59812	100nF 20% 50V 0603	2T58	2238 586 59812	10nF 20% 50V 0603	2V02	2238 586 59812	100nF 20% 50V 0603
2Q18	2238 586 59812	100nF 20% 50V 0603	2T98	2020 552 96628	10nF 10% 16V 0402	2V03	2238 586 59812	100nF 20% 50V 0603
2Q19	2238 586 59812	100nF 20% 50V 0603	2TG0	2238 586 59812	100nF 20% 50V 0603	2V04	2020 552 96618	1nF 10% 50V 0402
2Q20	4822 124 81058	47µF 20% 4V	2TG1	3198 032 15190	100µF 20% 4V	2V05	2238 869 15101	100pF 5% 50V 0402
2Q21	2020 552 96637	10µF 10% 6.3V 0805	2TG2	2238 586 59812	100nF 20% 50V 0603	2V16	2238 586 59812	100nF 20% 50V 0603
2Q22	4822 124 81058	47µF 20% 4V	2TG3	2020 552 96628	10nF 10% 16V 0402	2V17	2238 586 59812	100nF 20% 50V 0603
2Q23	2020 552 96637	10µF 10% 6.3V 0805	2TG4	2238 586 59812	100nF 20% 50V 0603	2V18	2238 586 59812	100nF 20% 50V 0603
2Q24	2238 586 59812	100nF 20% 50V 0603	2TG5	2020 552 96628	10nF 10% 16V 0402	2V19	2238 586 59812	100nF 20% 50V 0603
2Q25	3198 034 01290	12pF 1% 50V 0402	2TG6	2238 586 59812	100nF 20% 50V 0603	2V20	2238 586 59812	100nF 20% 50V 0603
2Q26	2238 586 59812	100nF 20% 50V 0603	2TG7	2238 586 59812	100nF 20% 50V 0603	2V21	2238 586 59812	100nF 20% 50V 0603
2Q27	2238 586 59812	100nF 20% 50V 0603	2TG8	2238 586 59812	100nF 20% 50V 0603	2V22	2238 586 59812	100nF 20% 50V 0603
2Q28	2238 586 59812	100nF 20% 50V 0603	2TG9	2238 586 59812	100nF 20% 50V 0603	2V23	2238 586 59812	100nF 20% 50V 0603
2Q29	2238 869 15101	100pF 5% 50V 0402	2TJ0	2238 586 59812	100nF 20% 50V 0603	2V24	2238 586 59812	100nF 20% 50V 0603
2Q30	2238 586 59812	100nF 20% 50V 0603	2TJ1	2238 586 59812	100nF 20% 50V 0603	2V25	2238 586 59812	100nF 20% 50V 0603
2Q31	2238 587 15619	560pF 10% 50V 0402	2TJ2	2238 586 59812	100nF 20% 50V 0603	2V26	2238 586 59812	100nF 20% 50V 0603
2Q32	2238 586 59812	100nF 20% 50V 0603	2TJ3	2238 586 59812	100nF 20% 50V 0603	2V27	2238 586 59812	100nF 20% 50V 0603
2Q33	2238 586 59812	100nF 20% 50V 0603	2TJ4	2238 586 59812	100nF 20% 50V 0603	2V28	2238 586 59812	100nF 20% 50V 0603
2Q34	2238 586 59812	100nF 20% 50V 0603	2TJ5	2238 586 59812	100nF 20% 50V 0603	2V29	2238 586 59812	100nF 20% 50V 0603
2Q35	2238 586 59812	100nF 20% 50V 0603	2TJ6	2238 586 59812	100nF 20% 50V 0603	2V30	2238 586 59812	100nF 20% 50V 0603
2Q37	2238 586 59812	100nF 20% 50V 0603	2TJ7	2020 552 96628	10nF 10% 16V 0402	2V31	2238 586 59812	100nF 20% 50V 0603
2Q38	2238 586 59812	100nF 20% 50V 0603	2TJ8	2020 552 96628	10nF 10% 16V 0402	2V35	4822 124 81058	47µF 20% 4V
2Q39	2238 586 59812	100nF 20% 50V 0603	2TJ9	2020 552 96628	10nF 10% 16V 0402	2Z51	2238 586 59812	100nF 20% 50V 0603
2Q40	4822 124 81058	47µF 20% 4V	2TK0	2020 552 96628	10nF 10% 16V 0402	2Z52	2238 586 59812	100nF 20% 50V 0603
2Q42	4822 124 81058	47µF 20% 4V	2TK1	2020 552 96628	10nF 10% 16V 0402			
2Q43	2020 552 96637	10µF 10% 6.3V 0805	2TK2	2020 552 96628	10nF 10% 16V 0402			
2Q44	2238 586 59812	100nF 20% 50V 0603	2TK3	2020 552 96628	10nF 10% 16V 0402			
2Q45	2238 586 59812	100nF 20% 50V 0603	2TK4	2238 586 59812	100nF 20% 50V 0603			
2Q46	2238 586 59812	100nF 20% 50V 0603	2TK5	2238 586 59812	100nF 20% 50V 0603			
2Q47	2238 586 59812	100nF 20% 50V 0603	2TK6	2022 552 05679	1µF 10% 16V 0805			
2Q48	2238 586 59812	100nF 20% 50V 0603	2TK7	2022 552 05679	1µF 10% 16V 0805			
2Q49	2238 586 59812	100nF 20% 50V 0603	2TK8	2022 552 05679	1µF 10% 16V 0805			
2Q50	2238 586 59812	100nF 20% 50V 0603	2TK9	2022 552 05679	1µF 10% 16V 0805			
2Q51	2238 586 59812	100nF 20% 50V 0603	2TL0	2238 586 59812	100nF 20% 50V 0603			
2Q52	2238 586 59812	100nF 20% 50V 0603	2TL7	4822 126 14324	33pF 5% 50V 0402			
2Q53	2238 586 59812	100nF 20% 50V 0603	2TL9	4822 126 14324	33pF 5% 50V 0402			
2Q54	2238 586 59812	100nF 20% 50V 0603	2TM2	2020 552 96628	10nF 10% 16V 0402			
2Q55	2238 586 59812	100nF 20% 50V 0603	2TM3	2022 552 05679	1µF 10% 16V 0805			
2Q56	2238 586 59812	100nF 20% 50V 0603	2TM4	2020 552 96628	10nF 10% 16V 0402			
2Q57	2238 586 59812	100nF 20% 50V 0603	2TM5	2020 552 96628	10nF 10% 16V 0402			
2Q58	2238 586 59812	100nF 20% 50V 0603	2TM7	2020 552 96628	10nF 10% 16V 0402			
2Q59	2238 586 59812	100nF 20% 50V 0603	2TM8	2022 552 05679	1µF 10% 16V 0805			
2Q60	2238 586 59812	100nF 20% 50V 0603	2TN0	4822 124 11946	22µF 20% 16V			
2Q61	2020 552 96618	1nF 10% 50V 0402	2TN1	4822 124 11946	22µF 20% 16V			
2Q62	2238 869 15101	100pF 5% 50V 0402	2TN3	2238 586 59812	100nF 20% 50V 0603			
2Q63	2238 586 59812	100nF 20% 50V 0603	2U00	2238 869 15101	100pF 5% 50V 0402			
2Q64	2238 586 59812	100nF 20% 50V 0603	2U01	2238 869 15101	100pF 5% 50V 0402			
2Q65	2238 586 59812	100nF 20% 50V 0603	2U02	2238 869 15101	100pF 5% 50V 0402			
2Q66	2238 586 59812	100nF 20% 50V 0603	2U03	2238 869 15101	100pF 5% 50V 0402			
2Q67	2238 586 59812	100nF 20% 50V 0603	2U04	2238 586 59812	100nF 20% 50V 0603			
2Q69	4822 124 11131	47µF 6.3V	2U05	2238 586 59812	100nF 20% 50V 0603			
2Q70	4822 124 11131	47µF 6.3V	2U06	2238 586 59812	100nF 20% 50V 0603			
2Q71	2238 869 15101	100pF 5% 50V 0402	2U07	2238 586 59812	100nF 20% 50V 0603			
2Q72	2238 869 15101	100pF 5% 50V 0402	2U09	2238 869 15101	100pF 5% 50V 0402			
2Q74	2238 869 15101	100pF 5% 50V 0402	2U10	2238 586 59812	100nF 20% 50V 0603			
2Q79	2020 552 96628	10nF 10% 16V 0402	2U11	2022 552 05679	1µF 10% 16V 0805			
2Q80	2238 869 15101	100pF 5% 50V 0402	2U12	2238 586 59812	100nF 20% 50V 0603			
2Q81	2020 552 96628	10nF 10% 16V 0402	2U13	2238 586 59812	100nF 20% 50V 0603			
2Q91	3198 035 04710	470pF 50V 0402	2U14	2238 586 59812	100nF 20% 50V 0603			
2Q92	3198 035 04710	470pF 50V 0402	2U15	2238 586 59812	100nF 20% 50V 0603			
2Q93	2238 869 15101	100pF 5% 50V 0402	2U16	2022 552 05679	1µF 10% 16V 0805			
2T01	2238 586 59812	100nF 20% 50V 0603	2U17	2022 552 05635	22µF 10% 16V			
2T02	2238 586 59812	100nF 20% 50V 0603	2U18	2238 586 59812	100nF 20% 50V 0603			
2T04	3198 034 02280	2.2pF 1% 50V 0402	2U19	2238 586 59812	100nF 20% 50V 0603			
2T05	2238 869 15829	82pF 5% 50V 0402	2U20	2238 586 59812	100nF 20% 50V 0603			
2T06	2238 869 15829	82pF 5% 50V 0402	2U21	3198 035 03320	3.3nF 5% 50V 0402			
2T07	2022 552 05679	1µF 10% 16V 0805	2U22	2022 552 05635	22µF 10% 16V			
2T08	2020 004 90283	10µF 20% 10V 1206	2U23	2238 869 15101	100pF 5% 50V 0402			
2T09	2020 552 96628	10nF 10% 16V 0402	2U24	2022 552 05635	22µF 10% 16V			
2T10	2238 586 59812	100nF 20% 50V 0603	2U25	2022 552 05635	22µF 10% 16V			
2T11	2020 552 96628	10nF 10% 16V 0402	2U26	2238 586 59812	100nF 20% 50V 0603			
2T12	2022 552 05679	1µF 10% 16V 0805	2U27	2020 552 96618	1nF 10% 50V 0402			
2T13	2020 552 96628	10nF 10% 16V 0402	2U28	2020 552 96618	1nF 10% 50V 0402			
2T14	2020 552 96628	10nF 10% 16V 0402	2U29	2020 552 96618	1nF 10% 50V 0402			
2T15	2020 552 96628	10nF 10% 16V 0402	2U30	2020 552 96618	1nF 10% 50V 0402			
2T16	2020 552 96628	10nF 10% 16V 0402	2U31	3198 035 03320	3.3nF 5% 50V 0402			
2T17	2238 586 59812	100nF 20% 50V 0603	2U32	3198 035 03320	3.3nF 5% 50V 0402			
2T18	2238 586 59812	100nF 20% 50V 0603	2U33	2238 869 15101	100pF 5% 50V 0402			
2T19	2020 552 96628	10nF 10% 16V 0402	2U35	2022 552 05679	1µF 10% 16V 0805			

3A62	4822 051 30102	1kΩ 5% 0.062W	3B94	4822 117 13543	470Ω 5% 0402	3G57	2350 033 11689	4x 68Ω 5% Netw.
3A63	4822 117 13606	10kΩ 5% 0.01W 0402	3B95	4822 117 13543	470Ω 5% 0402	3G57	2350 033 91001	4 x Jumper
3A64	4822 117 13606	10kΩ 5% 0.01W 0402	3B96	4822 117 13543	470Ω 5% 0402	3G58	2350 033 11689	4x 68Ω 5% Netw.
3A65	3198 031 02240	220kΩ 5% 0.1W 0402	3B97	4822 117 13543	470Ω 5% 0402	3G58	2350 033 91001	4 x Jumper
3A66	4822 117 11297	100kΩ 5% 0.1W	3B98	4822 117 13543	470Ω 5% 0402	3G59	2350 033 11689	4x 68Ω 5% Netw.
3A67	2322 734 63309	33Ω 1% 0.1W 0805	3B99	4822 117 13543	470Ω 5% 0402	3G59	2350 033 91001	4 x Jumper
3A68	2322 734 63309	33Ω 1% 0.1W 0805	3BA0	2120 550 00054	VDR 90V 1mA 0402	3G60	2350 033 11689	4x 68Ω 5% Netw.
3A69	4822 051 30102	1kΩ 5% 0.062W	3BA1	2120 550 00054	VDR 90V 1mA 0402	3G60	2350 033 91001	4 x Jumper
3A71	3198 031 01510	150Ω 5% 0.01W 0402	3BA2	2120 550 00054	VDR 90V 1mA 0402	3G61	4822 117 13545	100Ω 1% 0402
3A72	3198 031 02240	220kΩ 5% 0.1W 0402	3BA3	2120 550 00054	VDR 90V 1mA 0402	3G62	4822 117 13545	100Ω 1% 0402
3A73	4822 051 30221	220Ω 5% 0.062W	3BA4	2120 550 00054	VDR 90V 1mA 0402	3H01	3198 031 04720	4.7kΩ 5% 0402
3A74	4822 117 13606	10kΩ 5% 0.01W 0402	3BA5	2120 550 00054	VDR 90V 1mA 0402	3H02	4822 117 13545	100Ω 1% 0402
3A75	4822 117 13606	10kΩ 5% 0.01W 0402	3BA6	2120 550 00054	VDR 90V 1mA 0402	3H03	3198 031 04720	4.7kΩ 5% 0402
3A76	3198 031 02240	220kΩ 5% 0.1W 0402	3BA7	2120 550 00054	VDR 90V 1mA 0402	3H04	3198 031 01820	1.8kΩ 5% 0.01W 0402
3A77▲	4822 117 11748	Fuse 2.2Ω 5% 1206	3BA8	2120 550 00054	VDR 90V 1mA 0402	3H05	3198 031 01820	1.8kΩ 5% 0.01W 0402
3A78	4822 117 13601	22kΩ 5% 0402	3BA9	2120 550 00054	VDR 90V 1mA 0402	3H06	3198 031 02290	22Ω 5% 0.1W 0402
3A79	3198 031 04730	47Ω 5% 0402	3BB0	2120 550 00054	VDR 90V 1mA 0402	3H07	3198 031 02290	22Ω 5% 0.1W 0402
3A86	3198 031 06890	68Ω 5% 0402	3C30	2322 704 65601	560Ω 1% 0.063W 0603	3H08	3198 031 04720	4.7kΩ 5% 0402
3A87	4822 117 13606	10kΩ 5% 0.01W 0402	3C31	5322 117 11726	10Ω 5%	3H10	3198 031 04720	4.7kΩ 5% 0402
3A88	4822 117 13548	1kΩ 5% 0402	3C32	5322 117 13036	1.2kΩ 1% 0.063W 0603	3H12	3198 031 02290	22Ω 5% 0.1W 0402
3A89	4822 117 13548	1kΩ 5% 0402	3C33	3198 031 08210	820Ω 5% 0.5W	3H13	3198 031 04720	4.7kΩ 5% 0402
3A91	4822 117 12521	68Ω 1% 0.1W	3C34	5322 117 13036	1.2kΩ 1% 0.063W 0603	3H14	3198 031 02290	22Ω 5% 0.1W 0402
3A92	4822 117 12521	68Ω 1% 0.1W	3C35	4822 117 13548	1kΩ 5% 0402	3H15	4822 117 13545	100Ω 1% 0402
3A93	4822 117 13548	1kΩ 5% 0402	3C36	3198 031 08230	82kΩ 5% 0402	3H16	3198 031 04720	4.7kΩ 5% 0402
3A93	4822 117 13606	10kΩ 5% 0.01W 0402	3C37	4822 117 13597	330Ω 5% 0.01W 0402	3H18	3198 031 04720	4.7kΩ 5% 0402
3A94	4822 117 11297	100kΩ 5% 0.1W	3C38	4822 117 13606	10kΩ 5% 0.01W 0402	3H19	4822 117 13548	1kΩ 5% 0402
3A95	4822 051 20159	15Ω 5% 0.1W	3C39	4822 117 13545	100Ω 1% 0402	3H20	2322 705 70399	39Ω 5% 0402
3A96	4822 117 13606	10kΩ 5% 0.01W 0402	3C40	4822 117 13545	100Ω 1% 0402	3H21	2322 705 70399	39Ω 5% 0402
3A98	4822 117 13605	Jumper 0402	3C41	4822 117 13606	10kΩ 5% 0.01W 0402	3H22	3198 031 04720	4.7kΩ 5% 0402
3AA1	4822 051 30221	220Ω 5% 0.062W	3C42	4822 117 13597	330Ω 5% 0.01W 0402	3H23	3198 031 04720	4.7kΩ 5% 0402
3AA2	4822 051 30221	220Ω 5% 0.062W	3C43	3198 031 01820	1.8kΩ 5% 0.01W 0402	3H25	4822 117 13545	100Ω 1% 0402
3B00	3198 031 04720	4.7kΩ 5% 0402	3C44	3198 031 01220	1.2kΩ 5% 0.01W 0402	3H26	4822 117 13545	100Ω 1% 0402
3B01	3198 031 04720	4.7kΩ 5% 0402	3C45	3198 031 04730	47Ω 5% 0402	3H28	3198 031 04720	4.7kΩ 5% 0402
3B02	4822 117 13545	100Ω 1% 0402	3C46	3198 031 03390	33Ω 1% 0402	3H29	3198 031 04720	4.7kΩ 5% 0402
3B03	4822 117 13545	100Ω 1% 0402	3C47	3198 031 04730	47Ω 5% 0402	3H31	3198 031 04720	4.7kΩ 5% 0402
3B04	4822 117 13606	10kΩ 5% 0.01W 0402	3C51▲	4822 117 11748	Fuse 2.2Ω 5% 1206	3H32	3198 031 04720	4.7kΩ 5% 0402
3B05	3198 031 04730	47Ω 5% 0402	3C53	3198 031 03910	390Ω 1% 0402	3H41	4822 117 13606	10kΩ 5% 0.01W 0402
3B06	3198 031 04730	47Ω 5% 0402	3C55	4822 051 30331	330Ω 5% 0.062W	3H48	3198 031 06890	68Ω 5% 0402
3B07	4822 117 13545	100Ω 1% 0402	3C70	4822 117 13545	100Ω 1% 0402	3H49	3198 031 06890	68Ω 5% 0402
3B08	4822 117 13545	100Ω 1% 0402	3C71	4822 117 13548	1kΩ 5% 0402	3H50	3198 031 08210	820Ω 5% 0.5W
3B09	2120 550 00054	VDR 90V 1mA 0402	3C73	4822 117 13545	100Ω 1% 0402	3H50	4822 117 13606	10kΩ 5% 0.01W 0402
3B10	2120 550 00054	VDR 90V 1mA 0402	3C74	3198 031 01810	180Ω 5% 0402	3H51	2322 706 75601	560Ω 1% 0402
3B11	2120 550 00054	VDR 90V 1mA 0402	3C75	3198 031 01810	180Ω 5% 0402	3H51	4822 117 13606	10kΩ 5% 0.01W 0402
3B12	3198 031 04720	4.7kΩ 5% 0402	3G01	4822 117 11297	100kΩ 5% 0.1W	3H70	3198 031 04720	4.7kΩ 5% 0402
3B13	3198 031 04720	4.7kΩ 5% 0402	3G02	4822 117 13606	10kΩ 5% 0.01W 0402	3H71	3198 031 04720	4.7kΩ 5% 0402
3B14	4822 117 13545	100Ω 1% 0402	3G03	4822 117 13603	33kΩ 5% 0402	3H72	4822 117 13545	100Ω 1% 0402
3B15	4822 117 13545	100Ω 1% 0402	3G04	4822 117 13606	10kΩ 5% 0.01W 0402	3H73	3198 031 02290	22Ω 5% 0.1W 0402
3B16	4822 117 13606	10kΩ 5% 0.01W 0402	3G08	3198 031 06890	68Ω 5% 0402	3H74	3198 031 06890	68Ω 5% 0402
3B17	3198 031 04730	47Ω 5% 0402	3G08	4822 117 13605	Jumper 0402	3H75	4822 117 13545	100Ω 1% 0402
3B18	3198 031 04730	47Ω 5% 0402	3G09	3198 031 06890	68Ω 5% 0402	3H79	3198 031 02290	22Ω 5% 0.1W 0402
3B19	4822 117 13545	100Ω 1% 0402	3G09	4822 117 13605	Jumper 0402	3H80	2350 033 11472	4x 4.7kΩ 5%
3B20	4822 117 13545	100Ω 1% 0402	3G10	3198 031 06890	68Ω 5% 0402	3H81	2350 033 11472	4x 4.7kΩ 5%
3B21	2120 550 00054	VDR 90V 1mA 0402	3G10	4822 117 13605	Jumper 0402	3H82	3198 031 01050	1MΩ 5% 0402
3B22	2120 550 00054	VDR 90V 1mA 0402	3G11	3198 031 06890	68Ω 5% 0402	3H83	3198 031 04720	4.7kΩ 5% 0402
3B23	4822 117 13548	1kΩ 5% 0402	3G11	4822 117 13605	Jumper 0402	3H84	3198 031 04720	4.7kΩ 5% 0402
3B24	4822 117 13548	1kΩ 5% 0402	3G12	3198 031 06890	68Ω 5% 0402	3H85	3198 031 04720	4.7kΩ 5% 0402
3B27	3198 031 03390	33Ω 1% 0402	3G12	4822 117 13605	Jumper 0402	3H86	3198 031 04720	4.7kΩ 5% 0402
3B28	3198 031 03390	33Ω 1% 0402	3G13	3198 031 06890	68Ω 5% 0402	3H87	3198 031 04720	4.7kΩ 5% 0402
3B29	3198 031 03390	33Ω 1% 0402	3G13	4822 117 13605	Jumper 0402	3H88	3198 031 04720	4.7kΩ 5% 0402
3B30	2322 705 70399	39Ω 5% 0402	3G14	3198 031 06890	68Ω 5% 0402	3H90	3198 031 04720	4.7kΩ 5% 0402
3B32	2322 705 70399	39Ω 5% 0402	3G14	4822 117 13605	Jumper 0402	3H92	3198 031 07590	75Ω 5% 0402
3B34	2322 705 70399	39Ω 5% 0402	3G15	3198 031 06890	68Ω 5% 0402	3H93	3198 031 04720	4.7kΩ 5% 0402
3B36	3198 031 01230	12kΩ 5% 0402	3G15	4822 117 13605	Jumper 0402	3H94	3198 031 04720	4.7kΩ 5% 0402
3B37	4822 117 13548	1kΩ 5% 0402	3G16	3198 031 06890	68Ω 5% 0402	3H95	4822 117 13597	330Ω 5% 0.01W 0402
3B38	4822 117 13548	1kΩ 5% 0402	3G16	4822 117 13605	Jumper 0402	3H97	3198 031 04720	4.7kΩ 5% 0402
3B40	4822 117 13548	1kΩ 5% 0402	3G17	3198 031 06890	68Ω 5% 0402	3H98	4822 117 13545	100Ω 1% 0402
3B41	3198 031 03390	33Ω 1% 0402	3G17	4822 117 13605	Jumper 0402	3H99	4822 117 13545	100Ω 1% 0402
3B43	4822 117 13606	10kΩ 5% 0.01W 0402	3G18	3198 031 06890	68Ω 5% 0402	3J02	3198 031 02290	22Ω 5% 0.1W 0402
3B45	4822 117 13606	10kΩ 5% 0.01W 0402	3G18	4822 117 13605	Jumper 0402	3J05	3198 031 02290	22Ω 5% 0.1W 0402
3B48	2322 706 71002	1kΩ 1% 0402	3G19	4822 117 13545	100Ω 1% 0402	3J06	3198 031 02290	22Ω 5% 0.1W 0402
3B49	3198 031 04730	47Ω 5% 0402	3G22	4822 117 13545	100Ω 1% 0402	3J07	4822 117 13605	Jumper 0402
3B50	4822 117 13543	470Ω 5% 0402	3G24	4822 117 13545	100Ω 1% 0402	3J08	4822 117 13605	Jumper 0402
3B51	4822 117 13608	4.7Ω 5% 0603 0.62W	3G28	4822 117 13606	10kΩ 5% 0.01W 0402	3J11	4822 117 13605	Jumper 0402
3B52	2322 706 71002	1kΩ 1% 0402	3G29	4822 117 13606	10kΩ 5% 0.01W 0402	3J42	4822 117 13606	10kΩ 5% 0.01W 0402
3B53	2322 734 63309	33Ω 1% 0.1W 0805	3G30	4822 117 13546	47Ω 5% 0402	3J91	4822 117 13545	100Ω 1% 0402
3B54	2322 734 63309	33Ω 1% 0.1W 0805	3G31	4822 117 13546	47Ω 5% 0402	3L00	4822 117 11297	100kΩ 5% 0.1W
3B55	2322 734 63309	33Ω 1% 0.1W 0805	3G33	4822 117 13546	47Ω 5% 0402	3L01	4822 117 11297	100kΩ 5% 0.1W
3B56	2350 033 11339	4 x 33Ω 5%	3G36	4822 117 13546	47Ω 5% 0402	3L02	4822 117 13606	10kΩ 5% 0.01W 0402
3B57	2350 033 11339	4 x 33Ω 5%	3G37	4822 117 13606	10kΩ 5% 0.01W 0402	3L04▲	4822 117 11748	Fuse 2.2Ω 5% 1206
3B58	2350 033 11339	4 x 33Ω 5%	3G42	4822 117 13546	47Ω 5% 0402	3L05	5322 117 11726	10Ω 5%
3B59	2350 033 11339	4 x 33Ω 5%	3G43	4822 117 13545	100Ω 1% 0402	3L08	4822 117 13546	47Ω 5% 0402
3B60	4822 117 13545	100Ω 1% 0402	3G44	4822 117 13546	47Ω 5% 0402	3L09	4822 117 13546	47Ω 5% 0402
3B61	4822 117 13545	100Ω 1% 0402	3G45	4822 117 13545	100Ω 1% 0402	3L10	4822 117 13546	47Ω 5% 0402
3B62	2350 033 11339	4 x 33Ω 5%	3G46	4822 117 13545	100Ω 1% 0402	3L11	4822 117 13546	47Ω 5% 0402
3B65	4822 117 13548	1kΩ 5% 0402	3G47	4822 117 13545	100Ω 1% 0402	3L12	4822 117 13546	47Ω 5% 0402
3B66	4822 117 13548	1kΩ 5% 0402	3G48	4822 117 11297	100kΩ 5% 0.1W	3L13	4822 117 13546	47Ω 5% 0402
3B67	4822 117 13548	1kΩ 5% 0402						

3L25	4822 117 13546	47Ω 5% 0402	3LG2	4822 117 13606	10kΩ 5% 0.01W 0402	3LT9	3198 031 01090	10Ω 5% 0.01W 0402
3L27	4822 117 13546	47Ω 5% 0402	3LG3	4822 117 13545	100Ω 1% 0402	3LU0	4822 117 11297	100kΩ 5% 0.1W
3L29	4822 117 13546	47Ω 5% 0402	3LG5	4822 117 13545	100Ω 1% 0402	3LU1	3198 031 06830	68kΩ 5% 0.01W 0402
3L31	4822 117 13546	47Ω 5% 0402	3LG6	4822 117 13545	100Ω 1% 0402	3LU2	4822 117 13601	22kΩ 5% 0402
3L33	4822 117 13546	47Ω 5% 0402	3LG7	4822 117 13545	100Ω 1% 0402	3LU3	4822 117 13606	10kΩ 5% 0.01W 0402
3L38	4822 117 13606	10kΩ 5% 0.01W 0402	3LG8	4822 117 13545	100Ω 1% 0402	3LU4	4822 117 13606	10kΩ 5% 0.01W 0402
3L39	4822 117 13606	10kΩ 5% 0.01W 0402	3LG9	4822 117 13545	100Ω 1% 0402	3LU5	4822 117 13601	22kΩ 5% 0402
3L40	3198 031 03390	33Ω 1% 0402	3LH0	4822 117 13545	100Ω 1% 0402	3LU6	3198 031 06830	68kΩ 5% 0.01W 0402
3L41	3198 031 03390	33Ω 1% 0402	3LH1	4822 117 13545	100Ω 1% 0402	3LU7	2322 705 70184	180Ω 5% 0402
3L42	3198 031 03390	33Ω 1% 0402	3LH2	4822 117 11373	100Ω 1% 0805	3LU8	3198 031 01090	10Ω 5% 0.01W 0402
3L43	3198 031 03390	33Ω 1% 0402	3LH3	4822 117 13545	100Ω 1% 0402	3LU9	3198 031 04730	47Ω 5% 0402
3L44	3198 031 03390	33Ω 1% 0402	3LH4	4822 117 13545	100Ω 1% 0402	3LV0	3198 031 03340	330kΩ 5% 0402
3L45	3198 031 03390	33Ω 1% 0402	3LH5	4822 117 13606	10kΩ 5% 0.01W 0402	3LV1	3198 031 06830	68kΩ 5% 0.01W 0402
3L46	3198 031 03390	33Ω 1% 0402	3LH6	4822 117 13606	10kΩ 5% 0.01W 0402	3LV2	4822 117 13601	22kΩ 5% 0402
3L47	3198 031 03390	33Ω 1% 0402	3LH7	4822 117 11373	100Ω 1% 0805	3LV3	4822 117 13606	10kΩ 5% 0.01W 0402
3L48	3198 031 03390	33Ω 1% 0402	3LH8	4822 117 13545	100Ω 1% 0402	3LV4	4822 117 13606	10kΩ 5% 0.01W 0402
3L49	3198 031 03390	33Ω 1% 0402	3LH9	4822 117 13545	100Ω 1% 0402	3LV5	4822 117 13601	22kΩ 5% 0402
3L50	3198 031 02290	22Ω 5% 0.1W 0402	3LJ0	4822 117 13545	100Ω 1% 0402	3LV6	3198 031 06830	68kΩ 5% 0.01W 0402
3L51	4822 117 13545	100Ω 1% 0402	3LJ1	4822 117 13545	100Ω 1% 0402	3LV7	2322 705 70564	560kΩ 5% 0402
3L52	3198 031 02290	22Ω 5% 0.1W 0402	3LJ2	4822 117 13606	10kΩ 5% 0.01W 0402	3LV8	3198 031 01090	10Ω 5% 0.01W 0402
3L56	3198 031 02290	22Ω 5% 0.1W 0402	3LJ3	4822 117 13606	10kΩ 5% 0.01W 0402	3M00	4822 117 13606	10kΩ 5% 0.01W 0402
3L57	3198 031 02290	22Ω 5% 0.1W 0402	3LJ4	4822 117 13545	100Ω 1% 0402	3M01	4822 117 13606	10kΩ 5% 0.01W 0402
3L58	3198 031 02290	22Ω 5% 0.1W 0402	3LJ5	4822 117 13545	100Ω 1% 0402	3M02	4822 117 13606	10kΩ 5% 0.01W 0402
3L59	3198 031 02290	22Ω 5% 0.1W 0402	3LJ6	4822 117 13545	100Ω 1% 0402	3M03	4822 117 13603	33kΩ 5% 0402
3L60	3198 031 02290	22Ω 5% 0.1W 0402	3LJ7	4822 117 13545	100Ω 1% 0402	3M04	3198 031 01830	18kΩ 5% 0.01W 0402
3L61	3198 031 02290	22Ω 5% 0.1W 0402	3LJ8	4822 117 13545	100Ω 1% 0402	3M05	4822 117 13548	1kΩ 5% 0402
3L62	3198 031 02290	22Ω 5% 0.1W 0402	3LJ9	4822 117 13545	100Ω 1% 0402	3M09	4822 117 13606	10kΩ 5% 0.01W 0402
3L63	3198 031 02290	22Ω 5% 0.1W 0402	3LK0	4822 117 13545	100Ω 1% 0402	3M14	4822 117 13608	4.7Ω 5% 0603 0.62W
3L64	3198 031 02290	22Ω 5% 0.1W 0402	3LK1	4822 117 13545	100Ω 1% 0402	3M70	4822 117 13602	2.2kΩ 5% 0.01W 0402
3L65	3198 031 02290	22Ω 5% 0.1W 0402	3LK2	4822 117 13545	100Ω 1% 0402	3M71	3198 031 01220	1.2kΩ 5% 0.01W 0402
3L66	3198 031 02290	22Ω 5% 0.1W 0402	3LK3	4822 117 13545	100Ω 1% 0402	3M72	4822 117 13606	10kΩ 5% 0.01W 0402
3L67	3198 031 02290	22Ω 5% 0.1W 0402	3LK4	4822 117 13545	100Ω 1% 0402	3M73	4822 117 13543	470Ω 5% 0402
3L68	3198 031 02290	22Ω 5% 0.1W 0402	3LK5	4822 117 13545	100Ω 1% 0402	3M74	4822 117 10353	150Ω 1% 0.1W
3L69	3198 031 02290	22Ω 5% 0.1W 0402	3LK6	4822 117 13545	100Ω 1% 0402	3M75	4822 117 10353	150Ω 1% 0.1W
3L70	3198 031 02290	22Ω 5% 0.1W 0402	3LK7	4822 117 13545	100Ω 1% 0402	3M76	4822 117 13548	1kΩ 5% 0402
3L71	3198 031 02290	22Ω 5% 0.1W 0402	3LK8	4822 117 13545	100Ω 1% 0402	3M77	3198 031 01520	1.2kΩ 5% 0.01W 0402
3L89	3198 031 02290	22Ω 5% 0.1W 0402	3LK9	4822 117 13545	100Ω 1% 0402	3M78	4822 117 13548	1kΩ 5% 0402
3L90	4822 117 13548	1kΩ 5% 0402	3LL0	4822 117 13545	100Ω 1% 0402	3M79	4822 117 13548	1kΩ 5% 0402
3L91	3198 031 03390	33Ω 1% 0402	3LL1	4822 117 13545	100Ω 1% 0402	3M80	4822 117 10353	150Ω 1% 0.1W
3L92	3198 031 03390	33Ω 1% 0402	3LL2	4822 117 13545	100Ω 1% 0402	3M81	4822 117 10353	150Ω 1% 0.1W
3L93	3198 031 03390	33Ω 1% 0402	3LL3	4822 117 13545	100Ω 1% 0402	3M82	4822 117 10353	150Ω 1% 0.1W
3L94	3198 031 03390	33Ω 1% 0402	3LL4	4822 117 13545	100Ω 1% 0402	3N08	2322 706 71203	12kΩ 5% 0402
3L95	3198 031 03390	33Ω 1% 0402	3LL5	4822 117 13545	100Ω 1% 0402	3N09	4822 117 13545	100Ω 1% 0402
3L96	3198 031 03390	33Ω 1% 0402	3LL6	4822 117 13545	100Ω 1% 0402	3N12	3198 031 01530	15kΩ 5% 0.01W 0402
3L97	3198 031 03390	33Ω 1% 0402	3LL7	4822 117 13545	100Ω 1% 0402	3N13	3198 031 01530	15kΩ 5% 0.01W 0402
3L98	3198 031 03390	33Ω 1% 0402	3LL8	4822 117 13597	330Ω 5% 0.01W 0402	3N14	3198 031 01530	15kΩ 5% 0.01W 0402
3L99	3198 031 02290	22Ω 5% 0.1W 0402	3LL9	4822 117 13596	220Ω 5% 0.01W 0402	3N15	3198 031 01530	15kΩ 5% 0.01W 0402
3LA0	4822 117 13606	10kΩ 5% 0.01W 0402	3LM0	4822 117 11373	100Ω 1% 0805	3N25	3198 031 04720	4.7kΩ 5% 0402
3LA1	4822 117 13606	10kΩ 5% 0.01W 0402	3LM1	4822 117 11373	100Ω 1% 0805	3N30	4822 117 10353	150Ω 1% 0.1W
3LA2	4822 117 13606	10kΩ 5% 0.01W 0402	3LM2	4822 117 11373	100Ω 1% 0805	3N31	4822 117 10353	150Ω 1% 0.1W
3LA3	4822 117 13606	10kΩ 5% 0.01W 0402	3LM3	4822 117 11373	100Ω 1% 0805	3N32	4822 117 10353	150Ω 1% 0.1W
3LA4	4822 117 13606	10kΩ 5% 0.01W 0402	3LM4	4822 117 11373	100Ω 1% 0805	3N33	4822 117 13608	4.7Ω 5% 0603 0.62W
3LA5	4822 117 13548	1kΩ 5% 0402	3LM5	4822 117 11373	100Ω 1% 0805	3N90	3198 031 04720	4.7kΩ 5% 0402
3LA6	4822 117 13606	10kΩ 5% 0.01W 0402	3LM6	4822 117 11373	100Ω 1% 0805	3N92	3198 031 04720	4.7kΩ 5% 0402
3LA7	4822 117 13606	10kΩ 5% 0.01W 0402	3LM7	4822 117 11373	100Ω 1% 0805	3O15	4822 117 13545	100Ω 1% 0402
3LA9	4822 117 13606	10kΩ 5% 0.01W 0402	3LN0	4822 117 11373	100Ω 1% 0805	3O16	4822 117 13545	100Ω 1% 0402
3LB4	4822 117 13606	10kΩ 5% 0.01W 0402	3LN1	4822 117 11373	100Ω 1% 0805	3P10	4822 117 13606	10kΩ 5% 0.01W 0402
3LB5	4822 117 13606	10kΩ 5% 0.01W 0402	3LN2	4822 117 11373	100Ω 1% 0805	3P11	4822 117 13606	10kΩ 5% 0.01W 0402
3LB7	4822 117 13606	10kΩ 5% 0.01W 0402	3LN3	4822 117 11373	100Ω 1% 0805	3P12	4822 117 13545	100Ω 1% 0402
3LB8	4822 117 13606	10kΩ 5% 0.01W 0402	3LN4	4822 117 11373	100Ω 1% 0805	3P13	4822 117 13545	100Ω 1% 0402
3LB9	4822 117 13606	10kΩ 5% 0.01W 0402	3LN5	4822 117 11373	100Ω 1% 0805	3P14	4822 117 13545	100Ω 1% 0402
3LC0	4822 117 13606	10kΩ 5% 0.01W 0402	3LN6	4822 117 11373	100Ω 1% 0805	3P15	4822 117 13606	10kΩ 5% 0.01W 0402
3LC1	4822 117 13606	10kΩ 5% 0.01W 0402	3LN7	4822 117 11373	100Ω 1% 0805	3P16	4822 117 13606	10kΩ 5% 0.01W 0402
3LC2	4822 117 13606	10kΩ 5% 0.01W 0402	3LQ6	4822 117 11373	100Ω 1% 0805	3P17	4822 117 13606	10kΩ 5% 0.01W 0402
3LC3	4822 117 13606	10kΩ 5% 0.01W 0402	3LQ7	4822 117 13545	100Ω 1% 0402	3P18	4822 117 13606	10kΩ 5% 0.01W 0402
3LC4	4822 117 13606	10kΩ 5% 0.01W 0402	3LQ8	4822 117 13545	100Ω 1% 0402	3P19	4822 117 13606	10kΩ 5% 0.01W 0402
3LC5	4822 117 11297	100kΩ 5% 0.1W	3LR0	3198 031 03390	33Ω 1% 0402	3P20	4822 117 13606	10kΩ 5% 0.01W 0402
3LC6	3198 031 04720	4.7kΩ 5% 0402	3LR1	3198 031 03390	33Ω 1% 0402	3P21	4822 117 13606	10kΩ 5% 0.01W 0402
3LC7	3198 031 04720	4.7kΩ 5% 0402	3LR2	4822 117 13606	10kΩ 5% 0.01W 0402	3P22	4822 117 13606	10kΩ 5% 0.01W 0402
3LC8	4822 117 13606	10kΩ 5% 0.01W 0402	3LR3	2350 033 11339	4 x 33Ω 5%	3P23	4822 117 13606	10kΩ 5% 0.01W 0402
3LC9	4822 117 13606	10kΩ 5% 0.01W 0402	3LR4	2350 033 11339	4 x 33Ω 5%	3P24	4822 117 13606	10kΩ 5% 0.01W 0402
3LD0	4822 117 13606	10kΩ 5% 0.01W 0402	3LR5	2350 033 11339	4 x 33Ω 5%	3P25	4822 117 13606	10kΩ 5% 0.01W 0402
3LD1	4822 117 13606	10kΩ 5% 0.01W 0402	3LR6	2350 033 11339	4 x 33Ω 5%	3P26	4822 117 13606	10kΩ 5% 0.01W 0402
3LD2	4822 117 13606	10kΩ 5% 0.01W 0402	3LR7	2350 033 11339	4 x 33Ω 5%	3P27	4822 117 13606	10kΩ 5% 0.01W 0402
3LD3	4822 117 13606	10kΩ 5% 0.01W 0402	3LR8	2350 033 11339	4 x 33Ω 5%	3P28	4822 117 13606	10kΩ 5% 0.01W 0402
3LD4	4822 117 13606	10kΩ 5% 0.01W 0402	3LR9	2350 033 11339	4 x 33Ω 5%	3P29	4822 117 13606	10kΩ 5% 0.01W 0402
3LD5	4822 117 13606	10kΩ 5% 0.01W 0402	3LS0	2350 033 11339	4 x 33Ω 5%	3P30	4822 117 13606	10kΩ 5% 0.01W 0402
3LD6	4822 117 13606	10kΩ 5% 0.01W 0402	3LS1	2350 033 11339	4 x 33Ω 5%	3P31	4822 117 13606	10kΩ 5% 0.01W 0402
3LD7	4822 117 13606	10kΩ 5% 0.01W 0402	3LS2	3198 031 06810	680Ω 5% 0.01W 0402	3P32	4822 117 13606	10kΩ 5% 0.01W 0402
3LD8	4822 117 13606	10kΩ 5% 0.01W 0402	3LS3	4822 117 13606	10kΩ 5% 0.01W 0402	3P33	4822 117 11297	100kΩ 5% 0.1W
3LD9	4822 117 13606	10kΩ 5% 0.01W 0402	3LS4	4822 117 13606	10kΩ 5% 0.01W 0402	3P35	3198 031 02290	22Ω 5% 0.1W 0402
3LE0	4822 117 13606	10kΩ 5% 0.01W 0402	3LS5	4822 117 13606	10kΩ 5% 0.01W 0402	3P36	4822 117 13606	10kΩ 5% 0.01W 0402
3LE1	4822 117 11373	100Ω 1% 0805	3LS6	4822 117 13606	10kΩ 5% 0.01W 0402	3P37	4822 117 11297	100kΩ 5% 0.1W
3LE2	4822 117 13545	100Ω 1% 0402	3LS7	4822 117 13597	330Ω 5% 0.01W 0402	3P38	4822 117 13606	10kΩ 5% 0.01W 0402
3LE3	3198 031 04720	4.7kΩ						

3P75	3198 031 04730	47Ω 5% 0402	3T19	2350 033 11689	4x 68Ω 5% Netw.	3UA4	2322 706 71002	1kΩ 1% 0402
3P76	4822 117 13548	1kΩ 5% 0402	3T20	2350 033 11689	4x 68Ω 5% Netw.	3UA5	4822 117 13546	47Ω 5% 0402
3P77	4822 117 13548	1kΩ 5% 0402	3T21	2350 033 11689	4x 68Ω 5% Netw.	3UA7	2322 706 71002	1kΩ 1% 0402
3P78	4822 117 13606	10kΩ 5% 0.01W 0402	3T22	3198 031 06890	68Ω 5% 0402	3UA8	3198 031 06890	68Ω 5% 0402
3P79	3198 031 02710	270Ω 5% 0.1W 0402	3T23	3198 031 06890	68Ω 5% 0402	3UA9	3198 031 06890	68Ω 5% 0402
3P80	4822 117 13606	10kΩ 5% 0.01W 0402	3T26	4822 117 13545	100Ω 1% 0402	3V00	3198 031 02290	22Ω 5% 0.1W 0402
3P81	4822 117 13602	2.2kΩ 5% 0.01W 0402	3T28	4822 117 13596	220Ω 5% 0.01W 0402	3V01	3198 031 02290	22Ω 5% 0.1W 0402
3P82	4822 117 13606	10kΩ 5% 0.01W 0402	3TG3	4822 117 13596	220Ω 5% 0.01W 0402	3V02	3198 031 02290	22Ω 5% 0.1W 0402
3P83	4822 117 13545	100Ω 1% 0402	3TG4	4822 117 13596	220Ω 5% 0.01W 0402	3V03	3198 031 02290	22Ω 5% 0.1W 0402
3P84	4822 117 13545	100Ω 1% 0402	3TG5	4822 117 13548	1kΩ 5% 0402	3V04	3198 031 02290	22Ω 5% 0.1W 0402
3P85	4822 117 13545	100Ω 1% 0402	3TG6	4822 117 13596	220Ω 5% 0.01W 0402	3V05	3198 031 02290	22Ω 5% 0.1W 0402
3P86	4822 117 13545	100Ω 1% 0402	3TG8	4822 117 13545	100Ω 1% 0402	3V06	3198 031 02290	22Ω 5% 0.1W 0402
3P88	4822 117 13606	10kΩ 5% 0.01W 0402	3TG9	4822 117 13545	100Ω 1% 0402	3V07	3198 031 02290	22Ω 5% 0.1W 0402
3Q00	4822 117 13546	47Ω 5% 0402	3TH0	4822 117 13548	1kΩ 5% 0402	3V08	3198 031 02290	22Ω 5% 0.1W 0402
3Q02	2350 033 10101	4 x 100Ω 5%	3TH3	2322 706 73303	33kΩ 5% 0402	3V09	3198 031 02290	22Ω 5% 0.1W 0402
3Q03	3198 031 04720	4.7kΩ 5% 0402	3TH4	4822 117 13548	1kΩ 5% 0402	3V10	3198 031 02290	22Ω 5% 0.1W 0402
3Q04	3198 031 04720	4.7kΩ 5% 0402	3TH5	2322 706 73303	33kΩ 5% 0402	3V11	3198 031 02290	22Ω 5% 0.1W 0402
3Q05	2350 033 10101	4 x 100Ω 5%	3TH6	3198 031 04720	4.7kΩ 5% 0402	3V12	3198 031 02290	22Ω 5% 0.1W 0402
3Q06	2322 705 70399	39Ω 5% 0402	3TH7	3198 031 04720	4.7kΩ 5% 0402	3V13	3198 031 02290	22Ω 5% 0.1W 0402
3Q07	2350 033 10101	4 x 100Ω 5%	3TH9	3198 031 04730	47Ω 5% 0402	3V14	3198 031 02290	22Ω 5% 0.1W 0402
3Q08	2350 033 10101	4 x 100Ω 5%	3TJ0	3198 031 04730	47Ω 5% 0402	3V15	3198 031 02290	22Ω 5% 0.1W 0402
3Q09	3198 031 03390	33Ω 1% 0402	3TJ1	3198 031 04730	47Ω 5% 0402	3V16	3198 031 02290	22Ω 5% 0.1W 0402
3Q10	4822 117 13545	100Ω 1% 0402	3TJ2	3198 031 08220	8.2kΩ 5% 0.5W	3V17	3198 031 02290	22Ω 5% 0.1W 0402
3Q11	4822 117 13545	100Ω 1% 0402	3TJ3	3198 031 04730	47Ω 5% 0402	3V18	3198 031 02290	22Ω 5% 0.1W 0402
3Q12	4822 117 13545	100Ω 1% 0402	3TJ5	4822 117 13548	1kΩ 5% 0402	3V19	3198 031 02290	22Ω 5% 0.1W 0402
3Q13	4822 117 13545	100Ω 1% 0402	3TJ6	4822 117 13548	1kΩ 5% 0402	3V20	3198 031 02290	22Ω 5% 0.1W 0402
3Q14	4822 117 13545	100Ω 1% 0402	3TJ7	4822 117 13548	1kΩ 5% 0402	3V21	3198 031 02290	22Ω 5% 0.1W 0402
3Q15	4822 117 13545	100Ω 1% 0402	3U00	4822 117 13603	33kΩ 5% 0402	3V22	3198 031 02290	22Ω 5% 0.1W 0402
3Q16	3198 031 01530	15kΩ 5% 0.01W 0402	3U01	4822 117 13603	33kΩ 5% 0402	3V23	3198 031 02290	22Ω 5% 0.1W 0402
3Q17	3198 031 01530	15kΩ 5% 0.01W 0402	3U02	4822 117 13596	220Ω 5% 0.01W 0402	3V32	3198 031 02290	22Ω 5% 0.1W 0402
3Q18	3198 031 01530	15kΩ 5% 0.01W 0402	3U03	4822 117 13606	10kΩ 5% 0.01W 0402	3V33	3198 031 02290	22Ω 5% 0.1W 0402
3Q19	3198 031 02290	22Ω 5% 0.1W 0402	3U04	4822 117 13601	22kΩ 5% 0402	3V34	3198 031 02290	22Ω 5% 0.1W 0402
3Q20	3198 031 02290	22Ω 5% 0.1W 0402	3U05	4822 117 13596	220Ω 5% 0.01W 0402	3V35	3198 031 02290	22Ω 5% 0.1W 0402
3Q21	3198 031 02290	22Ω 5% 0.1W 0402	3U06	3198 031 03930	39kΩ 5% 0402	3V36	3198 031 02290	22Ω 5% 0.1W 0402
3Q22	3198 031 02290	22Ω 5% 0.1W 0402	3U07	3198 031 06820	6.8kΩ 5% 0.01W 0402	3V37	3198 031 02290	22Ω 5% 0.1W 0402
3Q23	3198 031 01530	15kΩ 5% 0.01W 0402	3U08	3198 031 03320	3.3kΩ 5% 0402	3V38	3198 031 02290	22Ω 5% 0.1W 0402
3Q24	4822 117 13606	10kΩ 5% 0.01W 0402	3U09	3198 031 06820	6.8kΩ 5% 0.01W 0402	3V39	3198 031 02290	22Ω 5% 0.1W 0402
3Q25	2350 033 10101	4 x 100Ω 5%	3U10	3198 031 03320	3.3kΩ 5% 0402	3V40	3198 031 02290	22Ω 5% 0.1W 0402
3Q26	2350 033 10101	4 x 100Ω 5%	3U11	4822 051 30221	220Ω 5% 0.062W	3V41	3198 031 02290	22Ω 5% 0.1W 0402
3Q27	3198 031 04720	4.7kΩ 5% 0402	3U12	4822 117 13548	1kΩ 5% 0402	3V42	3198 031 02290	22Ω 5% 0.1W 0402
3Q28	2350 033 10101	4 x 100Ω 5%	3U13	3198 031 06820	6.8kΩ 5% 0.01W 0402	3V43	3198 031 02290	22Ω 5% 0.1W 0402
3Q29	4822 117 13602	2.2kΩ 5% 0.01W 0402	3U14	3198 031 06820	6.8kΩ 5% 0.01W 0402	3V44	4822 117 13545	100Ω 1% 0402
3Q30	4822 117 13602	2.2kΩ 5% 0.01W 0402	3U15	4822 117 13548	1kΩ 5% 0402	3V78	4822 117 13548	1kΩ 5% 0402
3Q31	4822 117 13606	10kΩ 5% 0.01W 0402	3U16	3198 031 04720	4.7kΩ 5% 0402	3Z53	4822 117 13545	100Ω 1% 0402
3Q32	4822 117 13606	10kΩ 5% 0.01W 0402	3U17	2322 706 71002	1kΩ 1% 0402	3Z54	4822 117 13545	100Ω 1% 0402
3Q33	4822 117 13546	47Ω 5% 0402	3U18	4822 117 13596	220Ω 5% 0.01W 0402	9A01	4822 051 20008	Jumper 0805
3Q34	2350 033 10101	4 x 100Ω 5%	3U19	4822 117 13601	22kΩ 5% 0402	9A06	4822 051 20008	Jumper 0805
3Q35	4822 117 13546	47Ω 5% 0402	3U20	4822 051 30109	10Ω 5% 0.062W	9A29	4822 117 13605	Jumper 0402
3Q37	4822 117 13546	47Ω 5% 0402	3U21	4822 051 30109	10Ω 5% 0.062W	9A71	4822 117 13605	Jumper 0402
3Q38	2350 033 10101	4 x 100Ω 5%	3U22	5322 117 11726	10Ω 5%	9A78	4822 117 13545	100Ω 1% 0402
3Q39	4822 117 13546	47Ω 5% 0402	3U24	4822 051 30109	10Ω 5% 0.062W	9A79	4822 117 13605	Jumper 0402
3Q40	2350 033 10101	4 x 100Ω 5%	3U25	4822 117 13613	2.2Ω 5% 0603	9B11	4822 117 13605	Jumper 0402
3Q41	4822 117 13546	47Ω 5% 0402	3U27	4822 051 30109	10Ω 5% 0.062W	9B13	4822 117 13605	Jumper 0402
3Q43	4822 117 13546	47Ω 5% 0402	3U28	4822 117 13613	2.2Ω 5% 0603	9B14	4822 117 13605	Jumper 0402
3Q44	2350 033 10101	4 x 100Ω 5%	3U29	4822 117 13548	1kΩ 5% 0402	9B16	4822 117 13605	Jumper 0402
3Q45	4822 117 13546	47Ω 5% 0402	3U30	4822 117 13602	2.2kΩ 5% 0.01W 0402	9B19	4822 117 13605	Jumper 0402
3Q47	4822 117 13546	47Ω 5% 0402	3U32	4822 117 13606	10kΩ 5% 0.01W 0402	9B30	4822 117 13606	10kΩ 5% 0.01W 0402
3Q48	4822 117 13545	100Ω 1% 0402	3U33	4822 117 13606	10kΩ 5% 0.01W 0402	9B31	4822 117 13606	10kΩ 5% 0.01W 0402
3Q49	4822 117 13546	47Ω 5% 0402	3U37	2322 706 74701	470Ω 1% 0402	9C49	4822 117 13605	Jumper 0402
3Q50	4822 117 13545	100Ω 1% 0402	3U38	3198 031 04720	4.7kΩ 5% 0402	9C50	4822 051 20008	Jumper 0805
3Q51	4822 117 13546	47Ω 5% 0402	3U41	2322 706 73303	33kΩ 5% 0402	9C53	4822 117 13605	Jumper 0402
3Q52	4822 117 13545	100Ω 1% 0402	3U42	3198 031 01090	10Ω 5% 0.01W 0402	9C57	4822 117 13605	Jumper 0402
3Q53	4822 117 13546	47Ω 5% 0402	3U45	3198 031 01050	1MΩ 5% 0402	9C60	4822 117 13605	Jumper 0402
3Q55	4822 117 13546	47Ω 5% 0402	3U46	2322 706 71203	12kΩ 5% 0402	9C61	4822 117 13605	Jumper 0402
3Q57	4822 117 13546	47Ω 5% 0402	3U54	3198 031 01090	10Ω 5% 0.01W 0402	9G10	4822 117 13605	Jumper 0402
3Q59	4822 117 13546	47Ω 5% 0402	3U55	4822 117 13606	10kΩ 5% 0.01W 0402	9G11	4822 117 13605	Jumper 0402
3Q61	4822 117 13546	47Ω 5% 0402	3U56	4822 117 13548	1kΩ 5% 0402	9G12	4822 117 13605	Jumper 0402
3Q63	4822 117 13546	47Ω 5% 0402	3U62	4822 117 13548	1kΩ 5% 0402	9G13	4822 117 13605	Jumper 0402
3Q64	3198 031 06890	68Ω 5% 0402	3U64	4822 117 10353	150Ω 1% 0.1W	9G14	4822 117 13605	Jumper 0402
3Q66	4822 117 13546	47Ω 5% 0402	3U65	4822 117 10353	150Ω 1% 0.1W	9G15	4822 117 13605	Jumper 0402
3Q67	4822 117 13546	47Ω 5% 0402	3U71	4822 117 13548	1kΩ 5% 0402	9G16	4822 117 13605	Jumper 0402
3Q68	4822 117 13546	47Ω 5% 0402	3U79	4822 117 13545	100Ω 1% 0402	9G17	4822 117 13605	Jumper 0402
3Q72	4822 117 13545	100Ω 1% 0402	3U80	4822 117 13606	10kΩ 5% 0.01W 0402	9G18	4822 117 13605	Jumper 0402
3Q73	4822 117 13545	100Ω 1% 0402	3U81	4822 117 13545	100Ω 1% 0402	9G19	4822 117 13605	Jumper 0402
3Q75	4822 117 13545	100Ω 1% 0402	3U82	3198 031 06820	6.8kΩ 5% 0.01W 0402	9G20	4822 117 13605	Jumper 0402
3Q79	4822 117 13545	100Ω 1% 0402	3U83	3198 031 06820	6.8kΩ 5% 0.01W 0402	9G21	2350 033 91001	4 x Jumper
3Q81	3198 031 03320	3.3kΩ 5% 0402	3U85	4822 117 13606	10kΩ 5% 0.01W 0402	9G22	2350 033 91001	4 x Jumper
3Q82	3198 031 05620	5.6kΩ 5% 0.01W 0402	3U86	4822 117 13606	10kΩ 5% 0.01W 0402	9G23	2350 033 91001	4 x Jumper
3Q97	3198 031 04720	4.7kΩ 5% 0402	3U87	4822 117 13606	10kΩ 5% 0.01W 0402	9G24	2350 033 91001	4 x Jumper
3Q98	3198 031 04720	4.7kΩ 5% 0402	3U88	4822 117 13545	100Ω 1% 0402	9G25	2350 033 91001	4 x Jumper
3T02	4822 117 13548	1kΩ 5% 0402	3U89	4822 117 13606	10kΩ 5% 0.01W 0402	9G26	2350 033 91001	4 x Jumper
3T04	3198 031 01090	10Ω 5% 0.01W 0402	3U90	4822 117 13606	10kΩ 5% 0.01W 0402	9H03	4822 117 13605	Jumper 0402
3T05	3198 031 01090	10Ω 5% 0.01W 0402	3U91	4822 117 13606	10kΩ 5% 0.01W 0402	9H05	4822 117 13605	Jumper 0402
3T06	4822 117 13548	1kΩ 5% 0402	3U92	4822 117 13606	10kΩ 5% 0.01W 0402	9H06	4822 117 13605	Jumper 0402
3T09	3198 031 04720	4.7kΩ 5% 0402	3U93	4822 117 13606	10kΩ 5% 0.01W 0402	9H07	4822 117 13605	Jumper 0402
3T10	3198 031 04720	4.7kΩ 5% 0402	3U94	3198 031 03320	3.3kΩ 5% 0402	9H08	4822 117 13605	Jumper 0402
3T11	3198 031 04720	4.7kΩ 5%						

9H29	4822 117 13605	Jumper 0402
9H30	4822 117 13605	Jumper 0402
9H32	4822 117 13605	Jumper 0402
9H33	4822 117 13605	Jumper 0402
9H34	4822 117 13605	Jumper 0402
9H40	4822 117 13605	Jumper 0402
9J16	4822 117 13605	Jumper 0402
9J17	4822 117 13605	Jumper 0402
9J24	4822 117 13605	Jumper 0402
9LA0	4822 117 13605	Jumper 0402
9LA1	4822 117 13605	Jumper 0402
9LA7	4822 117 13605	Jumper 0402
9LA8	4822 117 13605	Jumper 0402
9LA9	4822 117 13605	Jumper 0402
9LC7	4822 117 13605	Jumper 0402
9M01	4822 117 13605	Jumper 0402
9M02	4822 117 13605	Jumper 0402
9M04	4822 117 13605	Jumper 0402
9M05	4822 117 13605	Jumper 0402
9P01	4822 117 13605	Jumper 0402
9P06	4822 117 13605	Jumper 0402
9P07	4822 117 13605	Jumper 0402
9P08	4822 117 13605	Jumper 0402
9P09	4822 117 13605	Jumper 0402
9P17	4822 117 13605	Jumper 0402
9P33	4822 117 13605	Jumper 0402
9P35	4822 117 13605	Jumper 0402
9P41	4822 117 13605	Jumper 0402
9P79	4822 117 13605	Jumper 0402
9Q14	4822 117 13605	Jumper 0402
9Q16	4822 117 13605	Jumper 0402
9Q19	4822 117 13605	Jumper 0402
9TG2	4822 117 13605	Jumper 0402
9TG3	4822 117 13605	Jumper 0402
9U01	4822 117 13605	Jumper 0402
9U02	4822 117 13605	Jumper 0402
9U03	4822 117 13605	Jumper 0402
9U04	4822 051 20008	Jumper 0805
9U05	4822 051 20008	Jumper 0805
9U10	4822 051 20008	Jumper 0805
9U12	4822 051 20008	Jumper 0805
9U13	4822 117 13605	Jumper 0402
9U14	4822 117 13605	Jumper 0402
9U15	4822 117 13605	Jumper 0402
9U16	4822 117 13605	Jumper 0402

5A01	2422 549 43062	Bead 600Ω at 100MHz
5A02	2422 549 43062	Bead 600Ω at 100MHz
5A03	2422 549 43062	Bead 600Ω at 100MHz
5A04	2422 549 43062	Bead 600Ω at 100MHz
5A05	2422 549 43062	Bead 600Ω at 100MHz
5A06	2422 549 42896	Bead 120Ω 100MHz
5A07	2422 549 42896	Bead 120Ω 100MHz
5A08	2422 549 43062	Bead 600Ω at 100MHz
5A10	2422 549 43062	Bead 600Ω at 100MHz
5B00	2422 549 43769	Bead 30Ω at 100MHz
5B01	2422 549 43769	Bead 30Ω at 100MHz
5B02	2422 549 44197	Bead 220Ω at 100MHz
5B10	2422 549 44197	Bead 220Ω at 100MHz
5B11	2422 549 44197	Bead 220Ω at 100MHz
5B12	2422 549 44197	Bead 220Ω at 100MHz
5B17	2422 549 44197	Bead 220Ω at 100MHz
5B18	2422 549 44197	Bead 220Ω at 100MHz
5C01	2422 549 44197	Bead 220Ω at 100MHz
5C03	2422 549 44197	Bead 220Ω at 100MHz
5C33	2422 549 44197	Bead 220Ω at 100MHz
5C34	2422 549 44197	Bead 220Ω at 100MHz
5C35	2422 549 44197	Bead 220Ω at 100MHz
5C36	2422 549 44197	Bead 220Ω at 100MHz
5C37	2422 549 42896	Bead 120Ω 100MHz
5C52	2422 549 44197	Bead 220Ω at 100MHz
5C53	2422 549 44197	Bead 220Ω at 100MHz
5C54	2422 549 44197	Bead 220Ω at 100MHz
5C57	3198 018 54770	0.47μF 10% 0603
5G01	2422 549 42896	Bead 120Ω 100MHz
5H01	2422 549 45325	Bead 67Ω at 100MHz
5H02	2422 549 45325	Bead 67Ω at 100MHz
5H03	2422 549 44197	Bead 220Ω at 100MHz
5H04	2422 549 44197	Bead 220Ω at 100MHz
5H05	3198 018 90050	Bead 1kΩ at 100MHz
5J00	2422 549 42896	Bead 120Ω 100MHz
5J01	2422 549 42896	Bead 120Ω 100MHz
5J02	2422 549 42896	Bead 120Ω 100MHz
5J03	2422 549 42896	Bead 120Ω 100MHz
5J04	2422 549 42896	Bead 120Ω 100MHz
5J05	2422 549 42896	Bead 120Ω 100MHz
5J06	2422 549 42896	Bead 120Ω 100MHz
5J07	2422 549 42896	Bead 120Ω 100MHz
5J13	2422 549 44197	Bead 220Ω at 100MHz
5J50	2422 549 45325	Bead 67Ω at 100MHz
5J52	2422 549 45325	Bead 67Ω at 100MHz

5J54	2422 549 45325	Bead 67Ω at 100MHz
5J56	2422 549 45325	Bead 67Ω at 100MHz
5J58	2422 549 45325	Bead 67Ω at 100MHz
5J60	2422 549 45325	Bead 67Ω at 100MHz
5L01	2422 549 43062	Bead 600Ω at 100MHz
5L50	2422 549 43769	Bead 30Ω at 100MHz
5L51	2422 549 44197	Bead 220Ω at 100MHz
5L52	2422 549 44197	Bead 220Ω at 100MHz
5LA1	2422 549 43769	Bead 30Ω at 100MHz
5LA2	2422 549 43062	Bead 600Ω at 100MHz
5LA3	2422 549 43769	Bead 30Ω at 100MHz
5LN0	2422 549 43062	Bead 600Ω at 100MHz
5LN1	2422 549 43769	Bead 30Ω at 100MHz
5LN2	2422 549 43062	Bead 600Ω at 100MHz
5LN3	2422 549 43062	Bead 600Ω at 100MHz
5LN4	2422 549 43062	Bead 600Ω at 100MHz
5N00	2422 549 44197	Bead 220Ω at 100MHz
5N01	2422 549 43769	Bead 30Ω at 100MHz
5N02	2422 549 43769	Bead 30Ω at 100MHz
5P02	2422 549 43769	Bead 30Ω at 100MHz
5P08	2422 549 43769	Bead 30Ω at 100MHz
5Q01	2422 549 43769	Bead 30Ω at 100MHz
5Q02	2422 549 43769	Bead 30Ω at 100MHz
5Q03	2422 549 43769	Bead 30Ω at 100MHz
5Q04	2422 549 43769	Bead 30Ω at 100MHz
5Q06	3198 018 52280	2.2μF 10% 1008
5Q07	2422 549 44197	Bead 220Ω at 100MHz
5T10	2422 549 44197	Bead 220Ω at 100MHz
5T11	2422 549 43062	Bead 600Ω at 100MHz
5T45	4822 157 71206	Bead 600Ω 100MHz
5T47	3198 018 90050	Bead 1kΩ at 100MHz
5T48	3198 018 90050	Bead 1kΩ at 100MHz
5T49	2422 549 43062	Bead 600Ω at 100MHz
5T50	4822 157 71206	Bead 600Ω 100MHz
5T51	4822 157 71206	Bead 600Ω 100MHz
5T55	4822 051 20008	Jumper 0805
5TG0	2422 549 43062	Bead 600Ω at 100MHz
5TG1	2422 549 42896	Bead 120Ω 100MHz
5TG2	2422 549 42896	Bead 120Ω 100MHz
5TG3	2422 549 43062	Bead 600Ω at 100MHz
5TG4	2422 549 43062	Bead 600Ω at 100MHz
5TG5	2422 549 43062	Bead 600Ω at 100MHz
5TG6	2422 549 43062	Bead 600Ω at 100MHz
5TG7	2422 549 43062	Bead 600Ω at 100MHz
5TG8	2422 549 44197	Bead 220Ω at 100MHz
5U00	2422 536 00671	10μH 20%
5U01	4822 051 20008	Jumper 0805
5U02	2422 536 00779	10μH 20%
5U03	2422 536 00671	10μH 20%
5U04	4822 051 20008	Jumper 0805
5U05	4822 051 20008	Jumper 0805
5U06	4822 051 20008	Jumper 0805
5U07	4822 051 20008	Jumper 0805
5U08	4822 051 20008	Jumper 0805
5U10	4822 051 20008	Jumper 0805
5U11	4822 051 20008	Jumper 0805
5U12	4822 051 20008	Jumper 0805
5U13	4822 051 20008	Jumper 0805
5U14	4822 051 20008	Jumper 0805
5V01	2422 549 44197	Bead 220Ω at 100MHz
5Z50	2422 549 43769	Bead 30Ω at 100MHz



6A00	4822 130 80622	BAT54
6A01	4822 130 80622	BAT54
6A02	4822 130 11397	BAS316
6B20	4822 130 11397	BAS316
6B21	4822 130 11397	BAS316
6B22	4822 130 11397	BAS316
6B23	4822 130 11397	BAS316
6C59	4822 130 11397	BAS316
6H00	9322 134 46685	SML-310MT
6H01	4822 130 11397	BAS316
6H03	4822 130 11397	BAS316
6H06	9340 566 10115	BAV99S
6H07	9340 566 10115	BAV99S
6J07	4822 130 11397	BAS316
6J08	4822 130 80622	BAT54
6L00	4822 130 11397	BAS316
6L01	4822 130 11397	BAS316
6L02	4822 130 11397	BAS316
6L03	4822 130 11397	BAS316
6M10	4822 130 11397	BAS316
6M11	4822 130 11397	BAS316
6O02	9340 566 10115	BAV99S
6P00	4822 130 11397	BAS316
6U05	9322 165 17668	STPS2L30A
6U07	9322 165 17668	STPS2L30A
6U17	4822 130 10838	UDZ3.3B
6U21	4822 130 11152	UDZ18B
6U22	4822 130 11397	BAS316
6U23	4822 130 11397	BAS316



7???		SW no's not available yet
7A01	9340 425 20115	BC847BS
7A02	3198 010 42310	BC847BW
7A04	9322 187 67668	TS482IS
7A05	9322 185 74668	LM324P
7A06	9340 219 30115	BC817-25W
7A07	9340 219 30115	BC817-25W
7A08	9340 425 30115	BC847BPN
7A09	3198 010 44350	BC807-25W
7A10	9340 425 30115	BC847BPN
7A11	3198 010 44350	BC807-25W
7A12	9340 425 30115	BC847BPN
7A13	9351 875 80118	74HCU04PW
7A15	3198 010 42320	BC857BW
7A16	9340 425 20115	BC847BS
7A18	9340 425 30115	BC847BPN
7A20	9340 425 20115	BC847BS
7A21	3198 010 42310	BC847BW
7B00	9340 560 35235	BSH112
7B01	9340 560 35235	BSH112
7B02	9322 206 25668	M24C02-WDW6P
7B03	9322 206 25668	M24C02-WDW6P
7B04	9340 560 35235	BSH112
7B05	9340 560 35235	BSH112
7B11	9352 774 45557	TDA9975EL/8/C1
7B12	9322 146 75685	TS431L
7B13	4822 130 42804	BC817-25
7B30	3198 010 42310	BC847BW
7B31	3198 010 42310	BC847BW
7B38	4822 209 17398	LD1117DT33
7C00	9352 767 55557	PNX3000HL/N3
7C31	9340 425 20115	BC847BS
7C32	9340 425 30115	BC847BPN
7C56	3198 010 42310	BC847BW
7C57	3198 010 42310	BC847BW
7G00	9322 221 66668	XC3S200-4TQG144C
7G01	9322 222 49668	XCF01SVOG20C
7G02	9322 214 08685	LD2985BM25
7G03	9322 215 24668	LD1117DT12
7G32	3198 010 42310	BC847BW
7G35	9340 425 20115	BC847BS
7H01	3198 010 44310	PDTC114EU
7J00	9352 783 31557	PNX2015E/M1C03
7J01	9340 425 30115	BC847BPN
7J02	9340 425 30115	BC847BPN
7J08	9322 212 46668	CY2305SXC-1
7L50	9322 204 09671	K4D261638F-LC40
7LA2	9340 425 30115	BC847BPN
7LA3	9340 425 30115	BC847BPN
7LA7	9322 206 45668	M25P05-AVMN6P
7LB0	9322 204 63685	NCP303LSN10
7LB1	9322 204 63685	NCP303LSN10
7LB2	9322 204 63685	NCP303LSN10
7LB3	9322 204 63685	NCP303LSN10
7LB4	9322 204 63685	NCP303LSN10
7LB5	3198 010 42310	BC847BW
7M01	3198 010 44310	PDTC114EU
7M03	9322 204 63685	NCP303LSN10
7M04	5322 130 60159	BC846B
7M05	9322 213 50685	TS431AIL
7M06	9322 213 50685	TS431AIL
7M07	5322 130 60159	BC846B
7M10	5322 130 60159	BC846B
7M11	5322 130 60159	BC846B
7M12	5322 130 60159	BC846B
7N00	9352 698 49518	ISP1561BM
7N10	5322 130 60159	BC846B
7P00	9322 173 43668	TPS2211AIDB
7P03	9322 160 60668	STV0701
7P10	9352 104 20118	74LVC244APW
7P13	9352 606 80118	74LVC257APW
7P14	9322 206 22668	M24C64-WDW6P
7P15	9351 750 00118	74HC4066PW
7P16	3198 010 44310	PDTC114EU
7P17	3198 010 44310	PDTC114EU
7P18	3198 010 42320	BC857BW
7P31	9352 190 20118	74LVC573APW
7P32	9352 190 20118	74LVC573APW
7P34	9352 115 40118	74LVC245APW
7P74	9340 269 20115	PMST3904
7P76	9352 115 40118	74LVC245APW
7P77	9352 115 40118	74LVC245APW
7P80	9322 206 62671	TC58DVMM92F1TGIO
7P81	9352 115 40118	74LVC245APW
7Q01	9322 204 86668	LM3526M-LNOPB
7Q05	9340 425 20115	BC847BS
7T00	9322 202 58668	LD1117DT50
7T10	9352 759 98118	PCA9515ADP
7T11	9340 425 30115	BC847BPN
7T12	3198 010 42310	BC847BW

7T41	9322 210 84685	UPC3218GV-A
7T43	9322 211 45668	UPC3220GR-A
7TG0	9322 211 46668	NXT2003
7TG1	9322 163 75685	SI2306DS
7TG3	9340 425 30115	BC847BPN
7U00	9322 207 46668	NCP5422AD
7U01	9322 218 27668	SI4944DY
7U03	9322 218 27668	SI4944DY
7U05	9340 425 20115	BC847BS
7U07	9340 425 30115	BC817-25W
7U10	9340 425 10115	BC857BS
7U11	9322 192 16685	TS2431AI
7U13	9340 425 30115	BC847BPN
7U15	9340 425 20115	BC847BS
7U17	9322 192 16685	TS2431AI
7U18	5322 130 60159	BC846B
7U27	9322 192 16685	TS2431AI
7U28	9340 575 87118	PHD38N02LT
7U29	9340 425 10115	BC857BS
7V00	9352 787 87557	PNX8550EH/M1/S1
7V01	9322 221 77671	K4D551638F-LC40
7V01	9322 225 58671	K4H511638C-UCCC
7V02	9322 221 77671	K4D551638F-LC40
7V02	9322 225 58671	K4H511638C-UCCC
7Z11	9352 115 40118	74LVC245APW
7Z12	9352 115 40118	74LVC245APW

External I/O Panel [BE]**Various**

1001	2422 026 05607	Socket CINCH 1pf bk
1002	2422 026 05697	Socket CINCH 3p f whrdye
1010	2422 026 05548	Socket phone 1p f
1020	2422 026 05778	Socket CHINCH 3p f YeBkBk
1030	2422 026 05779	Socket CHINCH 3p f GnBuRd
1040	2422 026 05781	Socket CHINCH 3p f BkRdWh
1050	2422 026 05779	Socket CHINCH 3p f GnBuRd
1060	2422 026 05782	Socket CHINCH 3p f RdWhYe
1070	4822 265 11391	Connector SVHS 4p f
1080	4822 265 11391	Connector SVHS 4p f
1E40	2422 025 17601	Connector 40p f
1E62	2422 025 17759	Connector 20p f
1M20	2422 025 10772	Connector 12p m
1M36	2422 025 10655	Connector 11p m



2002	2020 552 94427	100pF 5% 50V
2004	2238 586 59812	100nF 20% 50V 0603
2005	2020 552 94427	100pF 5% 50V
2007	5322 124 41945	22μF 20% 35V
2010	2020 552 94427	100pF 5% 50V
2012	2020 552 94427	100pF 5% 50V
2014	2238 586 59812	100nF 20% 50V 0603
2015	5322 124 41945	22μF 20% 35V
2016	2238 586 59812	100nF 20% 50V 0603
2017	5322 124 41945	22μF 20% 35V
2018	4822 126 11785	47pF 5% 50V 0603
2019	4822 124 23002	10μF 16V
2020	4822 126 11785	47pF 5% 50V 0603
2021	2020 552 94427	100pF 5% 50V
2022	4822 124 23002	10μF 16V
2023	2020 552 94427	100pF 5% 50V
2030	2020 552 94427	100pF 5% 50V
2035	5322 124 41945	22μF 20% 35V
2036	2238 586 59812	100nF 20% 50V 0603
2037	2238 586 59812	100nF 20% 50V 0603
2038	5322 124 41945	22μF 20% 35V
2039	2238 586 59812	100nF 20% 50V 0603
2040	5322 124 41945	22μF 20% 35V
2042	2422 549 43062	Bead 600Ω at 100MHz
2124	2238 586 59812	100nF 20% 50V 0603
2125	4822 124 12095	100μF 20% 16V
2126	2022 552 05679	1μF 10% 16V 0805
2127	4822 124 12313	22μF 10V 20%
2128	2238 586 59812	100nF 20% 50V 0603
2129	2238 586 59812	100nF 20% 50V 0603
2130	4822 124 12095	100μF 20% 16V
2131	4822 124 23002	10μF 16V
2132	2238 869 15101	100pF 5% 50V 0402
2133	2238 869 15101	100pF 5% 50V 0402
2134	2238 869 15101	100pF 5% 50V 0402
2135	2238 869 15101	100pF 5% 50V 0402
2136	2238 869 15101	100pF 5% 50V 0402

2137	2238 869 15101	100pF 5% 50V 0402
2138	2238 869 15101	100pF 5% 50V 0402
2139	2020 552 94427	100pF 5% 50V
2140	2020 552 94427	100pF 5% 50V
2141	2020 552 94427	100pF 5% 50V
2247	2020 552 94427	100pF 5% 50V
2248	2020 552 94427	100pF 5% 50V
2249	2020 552 94427	100pF 5% 50V
2250	2020 552 94427	100pF 5% 50V
2251	2020 552 94427	100pF 5% 50V
2252	2238 869 15101	100pF 5% 50V 0402
2I24	4822 126 11663	12pF 5% 50V 0603



3000	4822 051 30101	100Ω 5% 0.062W
3002	4822 051 30101	100Ω 5% 0.062W
3004	4822 117 13632	100kΩ 1% 0603 0.62W
3005	4822 117 13632	100kΩ 1% 0603 0.62W
3006	4822 117 13601	22kΩ 5% 0402
3007	4822 117 13545	100Ω 1% 0402
3008	4822 051 30101	100Ω 5% 0.062W
3010	4822 051 30101	100Ω 5% 0.062W
3011	4822 051 30759	75Ω 5% 0.062W
3012	4822 051 30101	100Ω 5% 0.062W
3014	4822 051 30561	560Ω 5% 0.062W
3015	4822 117 13632	100kΩ 1% 0603 0.62W
3016	4822 117 13632	100kΩ 1% 0603 0.62W
3017	4822 117 13601	22kΩ 5% 0402
3018	4822 051 30759	75Ω 5% 0.062W
3020	4822 117 13545	100Ω 1% 0402
3022	4822 051 30101	100Ω 5% 0.062W
3023	4822 051 30759	75Ω 5% 0.062W
3027	4822 117 13601	22kΩ 5% 0402
3028	4822 051 30759	75Ω 5% 0.062W
3029	4822 051 30759	75Ω 5% 0.062W
3030	4822 117 13545	100Ω 1% 0402
3031	4822 051 30101	100Ω 5% 0.062W
3032	4822 051 30759	75Ω 5% 0.062W
3037	4822 051 30759	75Ω 5% 0.062W
3038	4822 051 30101	100Ω 5% 0.062W
3039	4822 051 30102	1kΩ 5% 0.062W
3040	4822 051 30689	68Ω 5% 0.063W 0603
3042	4822 051 30561	560Ω 5% 0.062W
3043	4822 051 30103	10kΩ 5% 0.062W
3044	4822 051 30151	150Ω 5% 0.062W
3045	4822 051 30102	1kΩ 5% 0.062W
3046	4822 051 30101	100Ω 5% 0.062W
3047	4822 051 30102	1kΩ 5% 0.062W
3048	4822 117 13632	100kΩ 1% 0603 0.62W
3049	4822 051 30151	150Ω 5% 0.062W
3050	4822 051 30101	100Ω 5% 0.062W
3051	4822 051 30102	1kΩ 5% 0.062W
3052	4822 117 13632	100kΩ 1% 0603 0.62W
3060	4822 126 11785	47pF 5% 50V 0603
3070	4822 117 13601	22kΩ 5% 0402
3071	4822 117 13545	100Ω 1% 0402
3072	4822 051 30101	100Ω 5% 0.062W
3074	4822 051 30759	75Ω 5% 0.062W
3075	4822 051 30759	75Ω 5% 0.062W
3076	4822 117 13601	22kΩ 5% 0402
3077	4822 117 13545	100Ω 1% 0402
3078	4822 051 30101	100Ω 5% 0.062W
3080	4822 051 30759	75Ω 5% 0.062W
3081	4822 051 30223	22kΩ 5% 0.062W
3082	4822 051 30101	100Ω 5% 0.062W
3083	4822 051 30561	560Ω 5% 0.062W
3084	4822 051 30101	100Ω 5% 0.062W
3153▲	4822 117 11151	1Ω 5%
3154	4822 117 10361	680Ω 1% 0.1W
3156▲	4822 117 11151	1Ω 5%
3157	3198 031 04720	4.7kΩ 5% 0402
3158	3198 031 04720	4.7kΩ 5% 0402
3159	3198 031 01090	10Ω 5% 0.01W 0402
3160	4822 117 13596	220Ω 5% 0.01W 0402
3161	4822 117 13596	220Ω 5% 0.01W 0402
3999	4822 051 30101	100Ω 5% 0.062W
9100	4822 117 13605	Jumper 0402
9101	4822 117 13605	Jumper 0402
9104	4822 117 13605	Jumper 0402
9105	4822 117 13605	Jumper 0402
9106	4822 117 13605	Jumper 0402
9107	4822 117 13605	Jumper 0402
9210	4822 117 13605	Jumper 0402
9222	4822 117 13605	Jumper 0402



5000	2422 549 42896	Bead 120Ω 100MHz
5100	2422 549 43769	Bead 30Ω at 100MHz



6000	4822 130 11416	PDZ6.8B
6001	4822 130 11416	PDZ6.8B
6002	4822 130 11416	PDZ6.8B
6003	4822 130 11416	PDZ6.8B
6004	4822 130 10328	BAV99W
6005	4822 130 11416	PDZ6.8B
6006	4822 130 11416	PDZ6.8B
6007	4822 130 11416	PDZ6.8B
6008	4822 130 11416	PDZ6.8B
6009	4822 130 11416	PDZ6.8B
6010	4822 130 10328	BAV99W
6011	4822 130 11416	PDZ6.8B
6012	4822 130 11416	PDZ6.8B
6013	4822 130 11416	PDZ6.8B
6014	4822 130 10328	BAV99W
6015	4822 130 11416	PDZ6.8B
6017	4822 130 11416	PDZ6.8B
6018	4822 130 11416	PDZ6.8B
6019	4822 130 11416	PDZ6.8B
6020	4822 130 11416	PDZ6.8B
6021	4822 130 11416	PDZ6.8B
6022	4822 130 11416	PDZ6.8B
6023	4822 130 11416	PDZ6.8B
6024	4822 130 11416	PDZ6.8B
6025	4822 130 11416	PDZ6.8B
6026	4822 130 11416	PDZ6.8B
6027	4822 130 11416	PDZ6.8B
6029	4822 130 11416	PDZ6.8B
6030	4822 130 11416	PDZ6.8B
6040	4822 130 11416	PDZ6.8B
6041	4822 130 11416	PDZ6.8B
6045	4822 130 10328	BAV99W
6046	4822 130 11416	PDZ6.8B
6047	4822 130 10328	BAV99W
6048	4822 130 11416	PDZ6.8B
6049	4822 130 10328	BAV99W
6050	4822 130 11416	PDZ6.8B
6100	4822 130 11422	PLVA2650A
6101	4822 130 11422	PLVA2650A
6102	9322 102 64685	UDZ2.7B



7000	3198 010 42310	BC847BW
7001	3198 010 42310	BC847BW
7002	3198 010 42310	BC847BW
7003	3198 010 42310	BC847BW
7004	9340 425 20115	BC847BS
7010	3198 010 42310	BC847BW
7011	3198 010 42310	BC847BW
7012	3198 010 42310	BC847BW
7106	3198 010 42320	BC857BW
7107	3198 010 44310	PDTTC114EU

Audio Amplifier Panel [C]**Various**

1735	4822 267 10918	Connector 3p
1736	2422 025 10768	Connector 3p m
1M02	4822 267 10618	Connector 7p
1M06	2422 025 11244	Connector 7p m
1M52	2422 025 10769	Connector 9p m



2700	4822 126 14247	1.5nF 50V 0603
2701	4822 126 14249	560pF 10% 50V 0603
2703	2020 552 96683	220nF 10% 50V
2704	4822 124 11767	470μF 20% 25V
2705	4822 126 14249	560pF 10% 50V 0603
2706	5322 126 11579	3.3nF 10% 63V
2707	2222 580 15649	100nF 10% 50V 0805
2709	2020 552 96683	220nF 10% 50V
2710	2020 552 96683	220nF 10% 50V
2711	2022 552 05679	1μF 10% 16V 0805
2712	4822 126 14583	470nF 10% 16V 0805
2713	4822 126 13193	4.7nF 10% 63V
2715	4822 121 51252	470nF 5% 63V
2716	3198 017 31530	15nF 20% 50V 0603
2717	2022 552 05679	1μF 10% 16V 0805
2718	2222 580 15649	100nF 10% 50V 0805
2719	4822 126 14583	470nF 10% 16V 0805
2720	2020 021 91431	22μF 20% 100V
2721	2222 580 15649	100nF 10% 50V 0805
2722	4822 126 14583	470nF 10% 16V 0805
2723	2022 552 05679	1μF 10% 16V 0805
2726	4822 126 13193	4.7nF 10% 63V

2727	4822 126 14249	560pF 10% 50V 0603
2731	4822 126 14249	560pF 10% 50V 0603
2732	4822 126 14583	470nF 10% 16V 0805
2736	4822 121 51252	470nF 5% 63V
2737	3198 017 31530	15nF 20% 50V 0603
2739	2222 580 15649	100nF 10% 50V 0805
2741	4822 126 13883	220pF 5% 50V
2743	3198 016 31020	1nF 25V 0603
2744	2222 580 15649	100nF 10% 50V 0805
2745	2020 552 96683	220nF 10% 50V
2746	4822 124 11767	470μF 20% 25V
2747	2022 552 05679	1μF 10% 16V 0805
2748	4822 126 14247	1.5nF 50V 0603
2749	5322 126 11579	3.3nF 10% 63V
2751	4822 124 40433	47μF 20% 25V
2754	2020 021 91431	22μF 20% 100V
2770	3198 017 41050	1μF 10V 0603
2776	2020 021 91431	22μF 20% 100V
2780	4822 126 14583	470nF 10% 16V 0805
2789	4822 126 14583	470nF 10% 16V 0805
2790	2222 580 15649	100nF 10% 50V 0805
2791	4822 126 13879	220nF +80-20% 16V

—WW—

3700	4822 051 30561	560Ω 5% 0.062W
3701	4822 051 30479	47Ω 5% 0.062W
3702	3198 021 38220	8.2kΩ 5% 0.062W 0603
3703	3198 021 38220	8.2kΩ 5% 0.062W 0603
3704	4822 117 13632	100kΩ 1% 0603 0.62W
3705	4822 051 30222	2.2kΩ 5% 0.062W
3706	4822 051 30392	3.9Ω 5% 0.063W 0603
3707	4822 051 30393	39kΩ 5% 0.062W
3708	4822 051 30479	47Ω 5% 0.062W
3709	4822 051 30472	4.7Ω 5% 0.062W
3710	4822 051 30393	39kΩ 5% 0.062W
3711	2322 762 60568	5.6Ω 5% 5% 2512
3712	4822 051 30472	4.7Ω 5% 0.062W
3713	4822 051 30332	3.3Ω 5% 0.062W
3714	4822 051 30392	3.9Ω 5% 0.063W 0603
3715	2322 762 60568	5.6Ω 5% 5% 2512
3716	4822 117 13632	100kΩ 1% 0603 0.62W
3717	4822 051 30222	2.2kΩ 5% 0.062W
3718	4822 051 30561	560Ω 5% 0.062W
3719	4822 051 30124	120kΩ 5% 0.062W
3720	4822 051 30479	47Ω 5% 0.062W
3721	4822 051 30471	47Ω 5% 0.062W
3722	4822 051 30124	120kΩ 5% 0.062W
3723	4822 051 30471	47Ω 5% 0.062W
3724	4822 051 30102	1kΩ 5% 0.062W
3725	4822 117 12925	47kΩ 1% 0.063W 0603
3726	4822 051 30153	15kΩ 5% 0.062W
3727	4822 051 30103	10kΩ 5% 0.062W
3728	4822 051 30153	15kΩ 5% 0.062W
3729	4822 117 12925	47kΩ 1% 0.063W 0603
3730	4822 051 30223	22kΩ 5% 0.062W
3731	4822 051 30102	1kΩ 5% 0.062W
3732	4822 051 30223	22kΩ 5% 0.062W
3733	4822 051 30562	5.6kΩ 5% 0.063W 0603
3734	4822 051 30223	22kΩ 5% 0.062W
3735	4822 117 12889	270kΩ 1% 0.063W 0603
3736	4822 117 12925	47kΩ 1% 0.063W 0603
3737	4822 117 12925	47kΩ 1% 0.063W 0603
3738	4822 117 13632	100kΩ 1% 0603 0.62W
3740	4822 117 13632	100kΩ 1% 0603 0.62W
3742	4822 117 13632	100kΩ 1% 0603 0.62W
3746	4822 051 30222	2.2kΩ 5% 0.062W
3748	4822 117 13632	100kΩ 1% 0603 0.62W
3751	4822 051 30222	2.2kΩ 5% 0.062W
3752	4822 051 30103	10kΩ 5% 0.062W
3760	4822 051 30223	22kΩ 5% 0.062W
3764	4822 117 13632	100kΩ 1% 0603 0.62W
3765	4822 117 13632	100kΩ 1% 0603 0.62W
3777	4822 051 30102	1kΩ 5% 0.062W
3778	4822 051 30479	47Ω 5% 0.062W
3999	4822 051 30102	1kΩ 5% 0.062W
9710	4822 051 20008	Jumper 0805
9711	4822 051 20008	Jumper 0805
9712	4822 051 20008	Jumper 0805
9713	4822 051 20008	Jumper 0805
9748	4822 051 20008	Jumper 0805
9757	4822 051 20008	Jumper 0805
9758	4822 051 20008	Jumper 0805
9759	4822 051 20008	Jumper 0805
9760	4822 051 20008	Jumper 0805
9761	4822 051 20008	Jumper 0805
9762	4822 051 20008	Jumper 0805
9763	4822 051 20008	Jumper 0805
9764	4822 051 20008	Jumper 0805
9765	4822 051 20008	Jumper 0805
9766	4822 051 20008	Jumper 0805
9768	4822 051 20008	Jumper 0805
9770	4822 051 20008	Jumper 0805

9790	4822 051 20008	Jumper 0805
9795	4822 051 20008	Jumper 0805
9796	4822 051 20008	Jumper 0805
9806	4822 051 20008	Jumper 0805
9807	4822 051 20008	Jumper 0805
9808	4822 051 20008	Jumper 0805



5700	2422 536 00942	33μH 20%
5701	4822 157 11716	Bead 30Ω at 100MHz
5702	2422 536 00942	33μH 20%
5705	4822 157 11411	Bead 80Ω at 100MHz
5708	4822 157 11411	Bead 80Ω at 100MHz



6700	4822 130 11522	UDZ15B
6702	9322 150 18685	BZX384-C47
6703	4822 130 10838	UDZ3.3B
6704	4822 130 11551	UDZS10B
6705	4822 130 11551	UDZS10B



7700	9322 202 89668	LM393P
7701	9352 729 65112	TDA8925ST/N1
7702	3198 010 42310	BC847BW
7705	3198 010 42310	BC847BW
7706	3198 010 42310	BC847BW
7707	3198 010 42310	BC847BW
7708	3198 010 42320	BC857BW
7709	3198 010 42310	BC847BW
7710	3198 010 42310	BC847BW
7711	3198 010 42320	BC857BW
7712	3198 010 42310	BC847BW
7713	3198 010 42310	BC847BW
7715	3198 010 42310	BC847BW
7716	3198 010 42310	BC847BW
7717	3198 010 42310	BC847BW
7720	3198 010 42310	BC847BW

Side I/O Panel [D]

See 12nc on “Set Level”

Control Panel [E]

See 12nc on “Set Level”

LED Panel [J]

See 12nc on “Set Level”

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

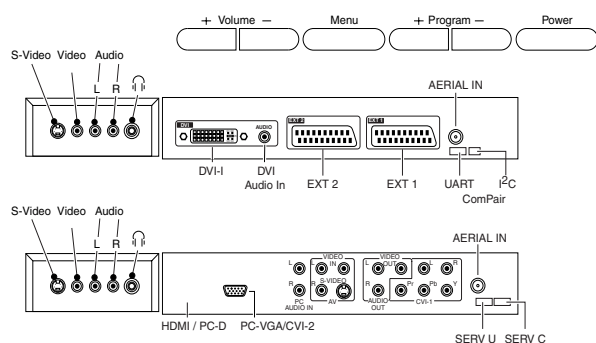
Manual xxxx xxx xxxx.1

- Manual expanded with the BP2.1U chassis.
- All chapters: small textual and graphical improvements.
- Ch. 1.2: Side connection figure updated.
- Ch. 5.4: Information about “LVDS tool” added.
- Ch. 5.8: Information about leaving “Factory mode” added.
- Ch. 9.1: Chassis feature overview added.
- Ch. 10: Spare Parts List updated.

Service Service Service

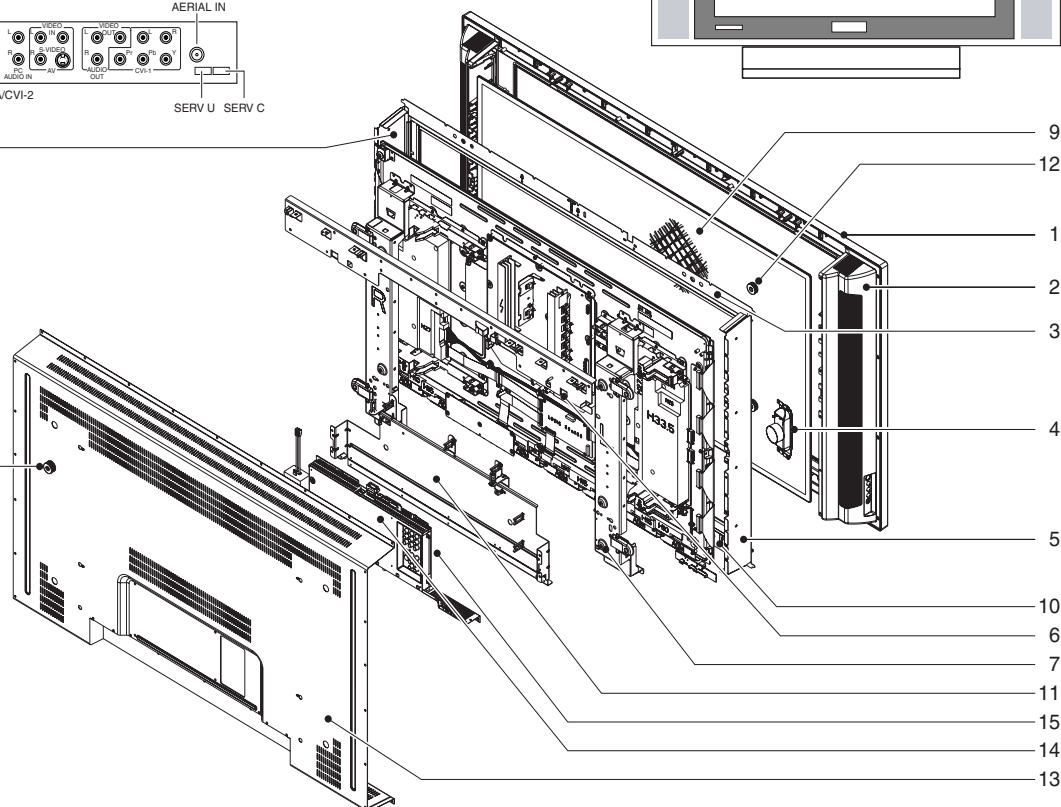
42PF5320/10
42PF5520D/10
42PF7320/10
42PF7320/79
42PF7320/98
42PF7320A/37
42PF7520D/10
42PF9630A/37
50PF7320/79
50PF7320/98
50PF7320A/37
50PF9630A/37
50PF9830A/37

Styling Sheet



17

12



STYLING 560.eps
150805

8 June 2007

560 new entryplus PDP_2007_23_A_IM.fm



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Safety regulations require that the set is restored to its original condition and that parts which are identical with those specified are used.

PHILIPS

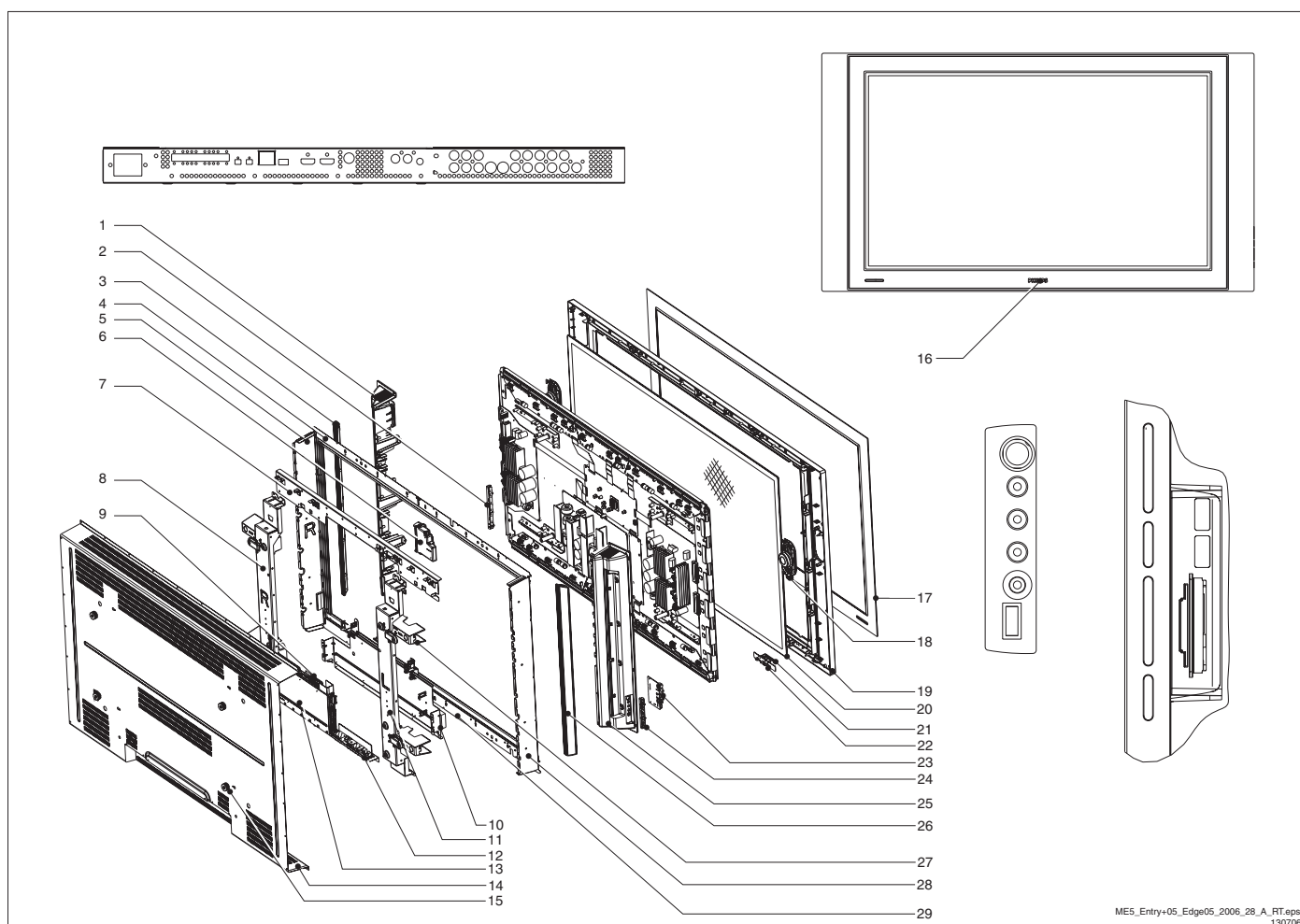
Mechanical Parts List

Styling 560 ENTRY+ 05				42PF7320/79	42PF7320/98	50PF7320/79	50PF7320/98	42PF7320A/37	50PF7320A/37	42PF5320/10	42PF7320/10	42PF5520D/10	42PF7520D/10	42PF9630A/37	50PF9630A/37	50PF9830A/37
Pos. Number	Item number	12NC	Material description													
1	0006	3104 328 40551	Front assy 42"	x	x			x								
1	0006	3104 328 40861	Front assy 42"							x		x				
1	0006	3104 328 40851	Front assy 42"								x		x			
1	0006	3104 328 42191	Front assy 42"											x		
1	0006	3104 328 40522	Front assy 50"			x	x									
1	0006	3104 328 42181	Front assy 50"						x							
1	0006	3104 328 42201	Front assy 50"												x	
1	0006	3104 328 39961	Front assy 50"													x
2	0224	3104 328 40771	Cover left 42"	x	x					x	x	x	x			
2	0224	3104 328 40781	Cover left 42"					x								
2	0224	3104 328 40791	Cover left 42"											x		
2	0224	3104 328 40811	Cover left 50"			x	x									
2	0224	3104 328 40821	Cover left 50"						x							
2	0224	3104 328 40831	Cover left 50"													x
3	0237	3104 308 13632	Upper shielding frame 42"	x	x			x		x	x	x	x	x		x
3	0237	3104 308 13692	Upper shielding frame 50"			x	x		x						x	x
4	5213	2441 257 30020	Loudspeaker L/R	x	x	x	x	x	x	x	x	x	x	x	x	x
4	5214	2441 257 30020	Loudspeaker L/R	x	x	x	x	x	x	x	x	x	x	x	x	x
5	0239	3104 308 13642	Left shielding frame 42"	x	x			x		x	x	x	x	x		
5	0239	3104 308 13702	Left shielding frame 50"			x	x		x						x	x
6	0058	3104 308 13781	Audio standby plate 42" + 50"	x	x	x	x	x	x	x	x	x	x			x
6	0058	Not applicable	Audio standby plate 42" + 50" (BP2.2 only)											x	x	
7	0164	3104 308 14712	Fixation bracket 42"	x	x			x		x	x	x	x	x		
7	0164	3104 308 14722	Fixation bracket 50"			x	x		x						x	x
8	1116	3104 328 40501	Side I/O (LC4.9A only)	x	x	x	x									
8	1016	3104 328 28892	Side I/O					x	x							
8	1016	3104 328 28881	Side I/O							x	x	x	x	x	x	x
9	0007	3104 304 90511	Glass plate 42"	x	x						x		x			
9	0007	3104 304 90571	Glass plate 42"					x						x		
9	0007	3104 304 90501	Glass plate 42"						x	x	x					
9	0007	3104 304 90551	Glass plate 50"			x	x		x						x	x
10	0238	3104 308 13622	Lower shielding frame 42"	x	x			x		x	x	x	x	x		
10	0238	3104 308 13682	Lower shielding frame 50"			x	x		x						x	x
11	0231	3104 308 14411	SSB plate 42"	x	x			x		x	x	x	x	x		
11	0231	3104 308 14581	SSB plate 50"			x	x		x							x
11	0231	Not applicable	SSB plate 50"												x	
12	0160	3104 308 12071	Mushroom assy	x	x	x	x	x	x	x	x	x	x	x	x	x
13	0009	3104 308 14531	Back cover 42"	x	x											
13	0009	3104 308 14151	Back cover 42"							x	x					
13	0009	3104 308 15411	Back cover 42"									x	x			
13	0009	3104 308 15621	Back cover 50"					x						x		
13	0009	3104 308 15641	Back cover 50"						x						x	
13	0009	3104 308 14241	Back cover 50"													x
13	0009	3104 308 14231	Back cover 50"			x	x									
14	0070	3104 308 14741	Top shielding	x	x	x	x			x	x					
14	0070	3104 308 13411	Top shielding					x	x			x		x	x	x
14	0070	3139 267 16311	Top shielding										x			
15	0071	3104 308 12321	Bottom shielding	x	x	x	x	x			x	x	x			
15	0071	3104 308 13422	Bottom shielding						x						x	x
16	1004	9322 225 38682	Screen PDP 42" S42AX-YD01					x					x	x		
16	1004	9322 226 37682	Screen PDP 42" S42SD-YD07	x	x						x					
16	1004	9322 224 88682	Screen PDP 42" PDP42V7A062						x							
16	1004	9322 226 61682	Screen PDP 42" PDP42V7K062									x				
16	1004	8204 000 78201	Screen PDP 50" S50HW-XD04						x							x
16	1004	9322 226 54682	Screen PDP 50" S50HW-XD04			x	x									x
17	0240	3104 308 13652	Right shielding frame 42"													
17	0240	3104 308 13712	Right shielding frame 50"													
18	1014	3104 328 39561	Side control (LC4.9)	x	x	x	x			x	x	x	x			
18	1014	3104 328 36671	Side control (Jaguar)					x	x						x	x
19	0041	3x04 304 28141	Light guide 42"	x	x					x	x	x	x	x		
19	0163	3122 124 36081	Light guide 50"			x	x		x							x
20	0227	3104 304 28241	Cover right 42"	x	x			x		x	x	x	x			
20	0227	3104 328 40801	Cover right 42"											x		
20	0227	3104 304 28301	Cover right 50"			x	x		x							
20	0227	3104 304 40841	Cover right 50"												x	x
	0097	3104 308 14591	Vesa plate 42" (Jaguar)						x	x					x	x
	0097	Not applicable	Vesa plate 42"	x	x	x	x			x	x	x	x			
	1850	3139 238 10231	Remote control RC1683701/01 (LC4.9)	x	x	x	x			x	x					
	1850	3139 238 10301	Remote control RC1683701/01 (LC4.9x AB)									x	x			
	8195	3139 238 11631	Remote control RC4345/01B (BP2.3)					x	x							
	1850	2422 549 00635	Remote control RC4318/US (BP2.2)												x	x
	1850	2422 549 00486	Remote control RC4308/US (BP2.1)													x
	0211, 0212	3104 308 14601	Upright stand	x	x	x	x	x	x	x						
	0212, 0213	3104 308 14621	Base stand	x	x	x	x	x	x	x	x	x	x		x	
	0213	3104 308 15061	Stand													x
		4622 001 50945	Mains cord /79 /98 /10	x	x	x	x			x	x	x	x			
		4622 004 00393	Mains cord /79 /98 /10	x	x	x	x			x	x	x	x			
		2422 070 00015	Mains cord /79	x	x	x	x									
		2422 070 00064	Mains cord /12													
		2422 070 98258	Mains cord UK													
	8195	2422 070 00054	Mains cord US					x	x					x	x	x

Service Service Service

32PF9630A/37	42PF7420/98
42PF5320/79	42PF7520D/79
42PF5620/10	42PF7520Z/93
42PF7320/93	42PF9630A/96
42PF7320Z/93	50PF7220A/37
42PF7420/10	50PF7320/10
42PF7420/79	50PF7320/93
42PF7420/93	50PF9630A/96

Styling Sheet



13 July 2006

ME5_Entry+05_Edge05_2006_28_A_RT.fm



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Safety regulations require that the set is restored to its original condition and that parts which are identical with those specified are used.

PHILIPS

Mechanical Parts List

ME5/Entry+05/Edge05 (16:9)				32PF9630A/37	42PF5320/79	42PF5620/10	42PF7320/93	42PF7320Z/93	42PF7420/10	42PF7420/79	42PF7420/93	42PF7420/98	42PF7520D/79	42PF7520Z/93	42PF9630A/96	50PF7220A/37	50PF7320/10	50PF7320/93	50PF9630A/96
Pos. number	Item number	12NC	Description																
1	0227	310430428241	Right cabinet cover		x	x	x	x					x	x					
1	0227	310430428301	Right cabinet cover													x	x	x	
1	0227	310432840801	Right cabinet cover												x				
1	0227	310432840841	Right cabinet cover																x
2	0052	313917788002	Control knob	x															
2	0014	310430814421	Side control bracket		x	x	x	x		x	x	x	x	x	x	x	x	x	
2	1014	310432836671	Side control																x
2	1014	310432839561	Side control		x	x	x	x	x				x	x			x	x	
2	1114	310432839561	Side control						x										
2+17+18+19+21+22+23+24	0006	310432842241	Front cabinet 32"	x															
2+17+18+19+21+22+23+24	0006	310432842973	Front cabinet 42"					x											
2+17+18+19+21+22+23+24	0006	310432839943	Front cabinet 42"			x		x						x					
2+17+18+19+21+22+23+24	0006	310432840551	Front cabinet 42"				x						x						
2+17+18+19+21+22+23+24	0006	310432842191	Front cabinet 42"												x				
2+17+18+19+21+22+23+24	0006	310432842963	Front cabinet 42"						x	x	x								
2+17+18+19+21+22+23+24	0006	310432843711	Front cabinet 42"		x														
2+17+18+19+21+22+23+24	0006	310432840561	Front cabinet 50"															x	
2+17+18+19+21+22+23+24	0006	310432842201	Front cabinet 50"																x
2+17+18+19+21+22+23+24	0006	310432842722	Front cabinet 50"														x		
3	1175	272217100297	Ambient light right												x				
3	1175	272217100304	Ambient light right																x
4	0237	310430813632	Upper display shielding 42"		x	x	x						x	x	x				
4	0237	310430813692	Upper display shielding 50"					x								x	x	x	x
5	0240	310430813652	Right display shielding 42"		x	x	x	x					x	x	x				
5	0240	310430813712	Right display shielding 50"													x	x	x	x
6	0180	310432835431	Card reader												x				x
6	0151	310430427791	Cardreader bottom bracket																x
6	0152	310430427801	Cardreader top bracket																x
6	0153	310430429091	Cardreader connection bracket																x
7	0058	310430813781	Audio support plate		x	x	x	x					x	x		x	x	x	x
7	1174	310432840301	Audio support plate												x	x			
7	1174	310432840303	Audio support plate																x
7	1174	313926722281	Audio support plate		x														
7	1174	310432840312	Audio support plate		x	x	x						x	x			x		
7	1174	310432840313	Audio support plate			x								x					
8	0167	310430813612	Fixation bracket R 42"		x														
8	0167	310430814881	Fixation bracket R 42"									x							
8	0167	310430816601	Fixation bracket R 42"			x							x						
8	0167	310430813672	Fixation bracket R 50"														x	x	
8+11	0164	310430814712	Fixation bracket L+R 42"		x		x	x							x				
8+11	0164	310430814722	Fixation bracket L+R 50"													x	x	x	x
8+11	0164	310430816521	Fixation bracket L+R 42"					x	x	x	x								
8+11	0164	310430816611	Fixation bracket L+R 42"			x							x	x					
9	0260	242201500192	LVDS locking part										x						
9	0260	310430427151	LVDS locking part		x														
9	0260	310430428841	LVDS locking part												x	x			x
10	0071	310430813422	SSB bottom shielding													x	x		x
10	0073	310430125151	SSB bottom shielding			x	x	x		x		x	x	x			x		
10	0231	310430814411	SSB plate		x	x	x	x					x	x	x				
10	0231	310430814581	SSB plate													x	x	x	x
11	0166	310430813602	Fixation bracket L 42"		x	x							x						
11	0166	310430816511	Fixation bracket L 42"									x							
11	0166	310430813662	Fixation bracket L 50"													x	x		
12	0037	310430813431	Connector plate												x	x			x
12	0037	310430814461	Connector plate		x														
12	0037	310430814651	Connector plate			x											x		
12	0037	310430814662	Connector plate		x		x	x		x				x				x	
12	0037	310430814682	Connector plate						x										
12	0037	310430814692	Connector plate						x		x								
12	0037	313917793241	Connector plate										x						
13	0070	310430813411	SSB top shielding																x
13	0070	310430814741	SSB top shielding		x	x	x	x	x	x	x	x		x			x	x	
13	0070	313926716311	SSB top shielding										x						
14	0009	310430815671	Rear cover 32"		x														
14	0008	310430429041	Rear cover 42"						x		x								
14	0009	310430814531	Rear cover 42"			x		x	x					x					
14	0009	310430815411	Rear cover 42"			x								x					
14	0009	310430815621	Rear cover 42"												x				
14	0009	310430814231	Rear cover 50"														x	x	
14	0009	310430815641	Rear cover 50"													x			x
15	0160	310430812071	Mushroom		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
16	0050	313912001861	Wordmark		x														
17	0004	310430814832	Inner front 42"						x										
17	0004	310430814792	Inner front 42"			x		x						x					
17	0004	310430814822	Inner front 42"						x	x	x								
17	0004	310430815762	Inner front 42"				x						x		x				
17	0004	310430814801	Inner front 50"															x	
17	0004	310430815771	Inner front 50"														x		x
17	0004	310430818191	Inner front 50"												x				

ME5/Entry+05/Edge05 (16:9)

Pos. number	Item number	12NC	Description	32PF9630A/37	42PF5320/79	42PF5620/10	42PF7320/93	42PF7320/93	42PF7420/10	42PF7420/79	42PF7420/93	42PF7420/98	42PF7520/79	42PF7520/93	42PF9630A/96	50PF7220A/37	50PF7320/10	50PF7320/93	50PF9630A/96
17+19	0005	310430815531	Outer+Inner front 42"		x														
17+19	0005	310432839883	Outer+Inner front 42"			x							x						
17+19	0005	310432840511	Outer+Inner front 42"				x						x						
17+19	0005	310432842132	Outer+Inner front 42"												x				
17+19	0005	310432842942	Outer+Inner front 42"							x		x							
17+19	0005	310432842141	Outer+Inner front 50"																x
17+19	0005	310432842712	Outer+Inner front 50"														x		
18	5213/5214	244125730020	Loudspeaker 8R 10W				x	x		x								x	
18	5213/5214	242226400539	Loudspeaker 8R 10W	x															
18	5213/5214	244125730020	Loudspeaker 8R 10W			x	x		x	x	x	x	x	x	x	x	x	x	
19	0003	310430815152	Outer front 42"					x			x								
19	0003	310430814141	Outer front 42"				x								x				
19	0003	310430815152	Outer front 42"						x		x								
19	0003	310430816262	Outer front 42"			x	x	x				x	x						
19	0003	310430814221	Outer front 50"														x		x
19	0003	310430815851	Outer front 50"															x	
19	0003	310430818181	Outer front 50"													x			
20	0007	310430490511	Glass plate 42"		x		x	x											
20	0007	310430490571	Glass plate 42"												x				
20	0007	310430490591	Glass plate 42"			x							x	x					
20	0007	310430490551	Glass plate 50"														x	x	x
21	0163	312212436081	Daylight filter		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
21	0200	313912010171	Light sensor holder	x															
21	0041	310430428141	Lightguide		x	x	x	x		x	x	x	x	x	x	x	x	x	x
21	0041	313912462171	Lightguide	x															
23+24	1116	310432840501	Side AV					x											
23+24	1116	310432841731	Side AV						x	x	x	x						x	
23+24	1016	310432828881	Side AV		x							x	x						
23+24	1018	310432840951	Side AV	x															
23+24	1116	310432839821	Side AV												x				x
23+24	1116	310432840501	Side AV		x	x	x					x	x				x		
23+24	1116	310432840611	Side AV														x		
24	0022	310432844951	Side AV bracket														x		
24	0187	310430426531	Side AV bracket							x		x							
24	0188	313912462881	Side AV door	x															
25	0224	310432840771	Left cabinet cover		x	x	x	x					x	x					
25	0224	310432840791	Left cabinet cover												x				
25	0224	310432840811	Left cabinet cover														x	x	
25	0224	310432840821	Left cabinet cover													x			
25	0224	310432840831	Left cabinet cover																x
26	1176	272217100303	Ambient light left																x
27	0162	310430814171	Interface bracket 42"		x		x	x							x				
27	0162	310430814181	Interface bracket 42"			x						x	x						
27	0162	310430814251	Interface bracket 50"														x	x	x
28	0239	310430813642	Left display shielding 42"		x	x	x	x				x	x	x					
28	0239	310430813702	Left display shielding 50"														x	x	x
29	0238	310430813622	Lower display shielding 42"		x	x	x	x				x	x	x					
29	0238	310430813682	Lower display shielding 50"														x	x	x
	0093	310430815391	Vesa plate	x															
	0094	310430124731	Wall mount bracket		x	x	x	x		x	x	x	x	x					x
	0096	310430427131	Wall spacer		x		x	x		x	x	x	x	x					x
	0210	313912877501	Stand	x															
	0211	310430814601	Upright stand		x	x	x	x	x	x	x	x	x	x			x	x	
	0212	310430814601	Upright stand													x	x		x
	0212	310430814621	Base stand		x	x	x	x	x	x	x	x	x	x			x	x	
	0213	310430814621	Base stand																x
	0213	310430816731	Base stand																
	1004	932221744682	LCD display 32" LC320W01-A6K1	x															
	1004	932222639682	LCD display 42" TFT-LCD LC420W02-A6 LPL						x	x	x	x							
	1004	932222720682	PDP display 42" FPF42C128128UE-52 (FHP)			x							x	x					
	1004	932222695682	PDP display 42" S42AX-YD01 PP42AX008A													x			
	1004	932222696682	PDP display 42" S42SD-YD07 PP42SD015B SDI				x	x											
	1004	932223381682	PDP display 42" S42SD-YD07 PP42SD015F SDI		x			x											
	1004	932223379682	PDP display 50" S50HW-XD04 PP50H-005E SDI														x	x	x
	1004	932222697682	PDP display 50" S50HW-XD04 PP50HW-005B SDI															x	x
	1850	313923811832	Remote control RC1683701/01H					x	x		x								
	1850	313923811832	Remote control RC1683701/01H				x	x		x	x			x					
	1850	313923811381	Remote control RC1683705/01		x														
	1850	313923810301	Remote control RC4343/01										x						
	1850	313923811631	Remote control RC4345/01B		x														
	8191	242207000064	Mains cord EU		x	x											x		
	8191	462200150945	Mains cord EU						x	x		x							
	8192	242207098258	Mains cord UK		x	x											x		
	8192	462200400393	Mains cord UK						x	x		x							
	8193	242207000017	Mains chord CH				x	x						x				x	
	8193	242207098146	Mains chord CH							x									
	8194	242207000015	Mainscord AUS/NZ		x								x						
	8194	242207000016	Mainscord AUS/NZ									x							
	8195	242207000054	Mainscord US													x	x		x
	8195	242207098208	Mainscord	x															

Service Service Service

FHP PDP Repair Manual

FPF32C106128UA-51, -52, -62 (32" H1)

FPF32C106128UA-72 (32" H2)

FPF37C128128UA-72 (37" H2)

FPF37C128128UB-72 (37" A1)

FPF42C128128UB-54 (42" H1)

FPF42C128128UB-72 (42" H2)

FPF42C128128UC-52 (42" A1)

FPF42C128128UD-52 (42" A2)

FPF42C128128UE-52 (42" A3)

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1. Technical Specifications

Index of this chapter:

- 1.1 Specifications
- 1.2 Serial Numbers
- 1.3 Chassis overview

1.1 Specifications

1.1.1 32" H1

No	Item	Spec. FPF32C106128UA-51,-52,-62
1	Pixel	Information not available
2	Number of Cells	
3	Pixel Pitch	
4	Cell Pitch	
5	Display size	
6	Screen size	
7	Screen aspect	
8	Dimensions	
9	Weight	
10	H sync, V sync, data	

1.1.2 32" H2

No	Item	Spec. FPF32C106128UA-72
1	Pixel	Information not available
2	Number of Cells	
3	Pixel Pitch	
4	Cell Pitch	
5	Display size	
6	Screen size	
7	Screen aspect	
8	Dimensions	
9	Weight	
10	H sync, V sync, data	

1.1.3 37" H2

No	Item	Spec. FPF37C128128UA-72
1	Pixel	852 (H) x 480(V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	2556 (H) x 480 (V)
3	Pixel Pitch	1.08 mm (H) x 1.08 mm (V)
4	Cell Pitch	0.36 mm (H) x 1.08 mm (V)
5	Display size	920.16 (H) x 518.40 mm (V)
6	Screen size	
7	Screen aspect	
8	Dimensions	
9	Weight	
10	H sync, V sync, data	

1.1.4 37" A1

No	Item	Spec. FPF37C128128UB-72
1	Pixel	1024 (H) x 1024 (V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	3072 (H) x 1024 (V)
3	Pixel Pitch	0.795 mm (H) x 0.435 mm (V)
4	Cell Pitch	0.265 mm (H) x 0.435 mm (V)
5	Display size	814.08 (H) x 454.44 mm (V)
6	Screen size	Diagonal 37"
7	Screen aspect	16:9

No	Item	Spec. FPF37C128128UB-72
8	Dimensions	903 (W) x 498 (H) x 66 (D) mm
9	Weight	About 13.5 kg
10	H sync, V sync, data	50 kHz (H), 50/60 Hz (V), LVDS

1.1.5 42" H1

No	Item	Spec. FPF42C128128UB-54
1	Pixel	Information not available
2	Number of Cells	
3	Pixel Pitch	
4	Cell Pitch	
5	Display size	
6	Screen size	
7	Screen aspect	
8	Dimensions	
9	Weight	
10	H sync, V sync, data	

1.1.6 42" H2

No	Item	Spec. FPF42C128128UB-72
1	Pixel	Information not available
2	Number of Cells	
3	Pixel Pitch	
4	Cell Pitch	
5	Display size	
6	Screen size	
7	Screen aspect	
8	Dimensions	
9	Weight	
10	H sync, V sync, data	

1.1.7 42" A1

No	Item	Spec. FPF42C128128UC-52
1	Pixel	1024 (H) x 1024 (V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	3072 (H) x 1024 (V)
3	Pixel Pitch	0.90 mm (H) x 0.51 mm (V)
4	Cell Pitch	0.30 mm (H) x 0.51 mm (V)
5	Display size	921.60 (H) x 522.24 mm (V)
6	Screen size	Diagonal 42"
7	Screen aspect	16:9
8	Dimensions	994 (W) x 585 (H) x 66 (D) mm
9	Weight	About 16 kg
10	H sync, V sync, data	50 kHz (H), 50/60 Hz (V), LVDS

1.1.8 42" A2

No	Item	Spec. FPF42C128128UD-52
1	Pixel	1024 (H) x 1024 (V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	3072 (H) x 1024 (V)
3	Pixel Pitch	0.90 mm (H) x 0.51 mm (V)
4	Cell Pitch	0.30 mm (H) x 0.51 mm (V)
5	Display size	921.60 (H) x 522.24 mm (V)
6	Screen size	Diagonal 42"
7	Screen aspect	16:9
8	Dimensions	994 (W) x 587 (H) x 66 (D) mm

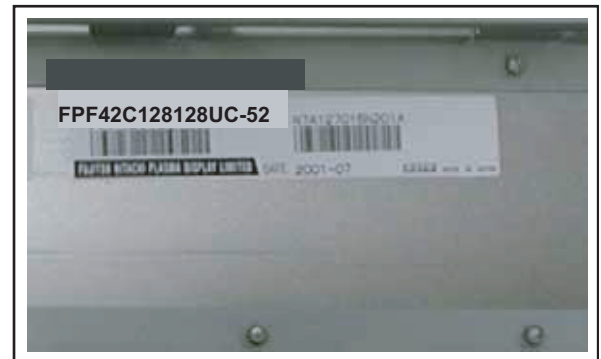
No	Item	Spec. FPF42C128128UD-52
9	Weight	About 16 kg
10	H sync, V sync, data	50kHz (H), 50/60/70Hz (V), LVDS

1.1.9 42" A3

No	Item	Spec. FPF42C128128UE-52
1	Pixel	1024 (H) x 1024 (V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	3072 (H) x 1024 (V)
3	Pixel Pitch	0.90 mm (H) x 0.51 mm (V)
4	Cell Pitch	0.30 mm (H) x 0.51 mm (V)
5	Display size	921.60 (H) x 522.24 mm (V)
6	Screen size	Diagonal 42"
7	Screen aspect	16:9
8	Dimensions	994 (W) x 587 (H) x 66 (D) mm
9	Weight	About 16 kg
10	H sync, V sync, data	50 kHz (H), 50/60 Hz (V), LVDS

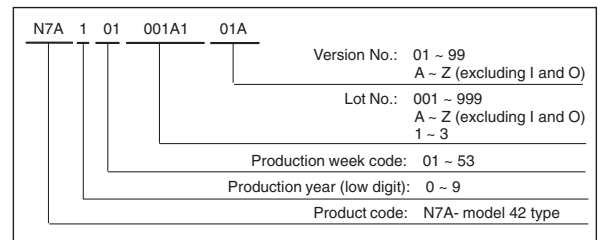
1.2 Serial Numbers

Check the serial ID number of the product requested for repair, before starting the problem analysis and repair.



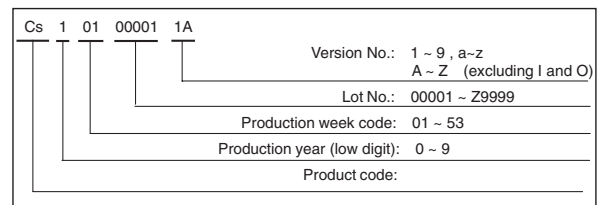
F_14582_002.eps
300905

Figure 1-1 Module product number



F_14582_001.eps
300905

Figure 1-2 Module serial number



F_14582_004.eps
300905

Figure 1-3 Panel serial number

Note: The module serial number and the serial number of the completed chassis (product requested for repair) are usually the same when the product is brought in for repair the first time.

1.3 Chassis overview

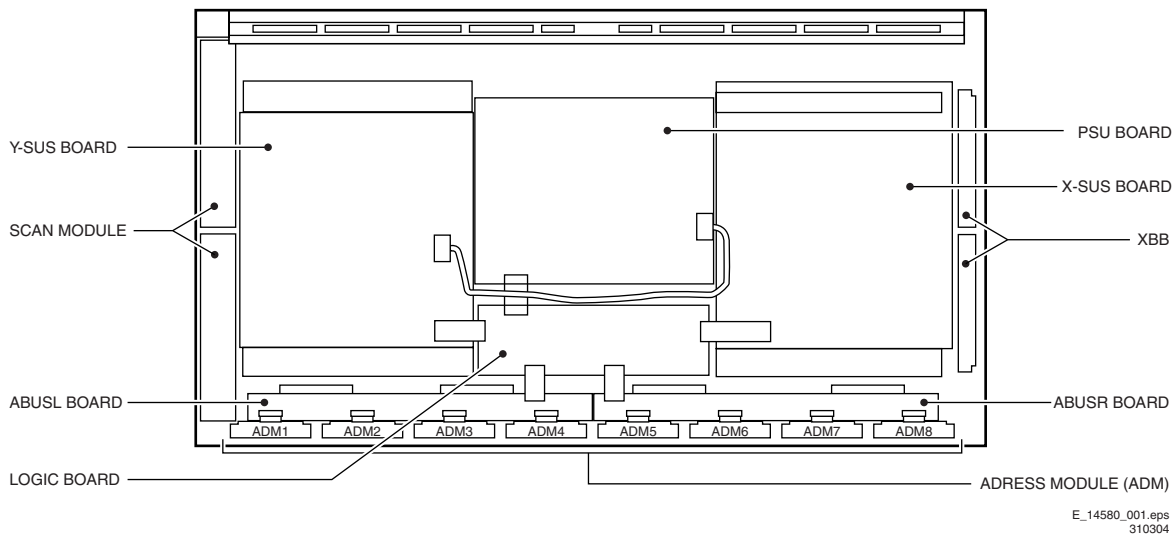


Figure 1-4 PWB locations


2. Safety Instructions, Warnings, and Notes

Index of this chapter:

- 2.1 Safety Instructions
- 2.2 Warnings
- 2.3 Notes


2.1 Safety Instructions

It is not allowed to operate the FTV-set without glass plate. One function of this glass plate is to absorb Infrared Radiation. Without this glass plate the level of Infrared Radiation produced by the plasma display could damage your eyes.

1. Safety regulations require that during a repair:
 - the set should be connected to the mains via an isolating transformer (in this particular case a transformer of ≥ 800 VA).
 - safety components, indicated by the symbol , should be replaced by components identical to the original ones.
2. Safety regulations require that after a repair the set must be returned in its original condition. In particular attention should be paid to the following points.
 - Note: The wire trees should be routed correctly and fixed with the mounted cable clamps.
 - The insulation of the mains lead should be checked for external damage.
 - The electrical DC resistance between the mains plug and the secondary side should be checked (only for sets that have a mains isolated power supply). This check can be done as follows:
 - unplug the mains cord and connect a wire between the two pins of the mains plug;
 - set the mains switch to the on position (keep the mains cord unplugged!);
 - measure the resistance value between the pins of the mains plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between $4.5\text{ M}\Omega$ and $12\text{ M}\Omega$;
 - switch off the TV and remove the wire between the two pins of the mains plug.
 - The cabinet should be checked for defects to avoid touching of any inner parts by the customer.

2.2 Warnings

1. ESD

All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD ) . Careless handling during repair can reduce life drastically. When repairing, make sure that you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential.

1. Available ESD protection equipment:
 - complete kit ESD3 (combining all 6 prior products - small table mat) 4822 310 10671
 - wristband tester 4822 344 13999
2. Never replace modules or other components while the unit is switched on.
3. When making settings, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

2.3 Notes

1. A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel it is recommended to do some maintenance by a qualified service employee only.

2. Never disconnect the power display cable when the set is operating
3. With DST no failures (error-codes) can be read, when the set is in Service-mode.
4. If DST reacts with "error 2", there is no communication between the TV and the DST. Note that the IR-transmitter LED is positioned at the right side of IR-receiver eye of the E-box. Take into account that receiver-LED on DST is positioned not in the middle but at the left side. Point corresponding LEDs to each other. In case the amount of Infrared produced by the screen pollutes the communication, the set can be set in Stand-by-mode. Then still the error-messages can be retrieved.

2.3.1 Notes on Safe Handling of the Plasma Display

Notes to Follow During Service

- The work procedures shown with the Note indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times other than when adjusting and checking the product, be sure to turn OFF the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of PC board, start the servicing work at least 30 seconds after the main power has been turned off. Especially when installing and removing the power supply PC board and the SUS PC board in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned off.
- While the main power is on, do not touch any parts or circuits other than the ones specified. The high voltage power supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit PC board, be sure to remove static electricity from your body before handling the circuit PC board.
- Be sure to handle the circuit PC board by holding the large parts as the heat sink or transformer. Failure to observe this precaution may result in the occurrence of an abnormality in the soldered areas.
- Do not stack the circuit PC boards. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.

- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original setup

3. Directions for Use

Not applicable.

4. Mechanical Instructions

Index of this chapter:

4.1 Board Swap Instructions

Notes:

- Figures below can deviate from the actual situation, due to different set executions.
- For more detailed instructions regarding the (dis)assembly of the TV chassis that hold these PDPs, read the corresponding TV Service Manual.

4.1 Board Swap Instructions

4.1.1 General

Before dismounting panels read notes below!

Caution when removing circuit board!

When removing the circuit board after the main power is turned on/off, wait for at least one minute before starting to remove the circuit board.

If the circuit board removal is started immediately after turning off the main power, it can result in electric shock or damage to the circuit due to residual electric charge.

Caution on handling the FPC connector!

To release the black lock lever of the connector, flip it up gently in the middle with the nail of the thumb or forefinger, from the side with the cable. Never pinch the lock lever with fingers or tools.

Doing so might damage the lock lever.

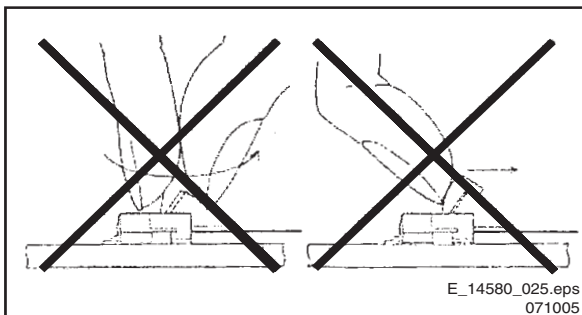


Figure 4-1 Handling the FPC connector

4.1.2 X-SUS Circuit Board

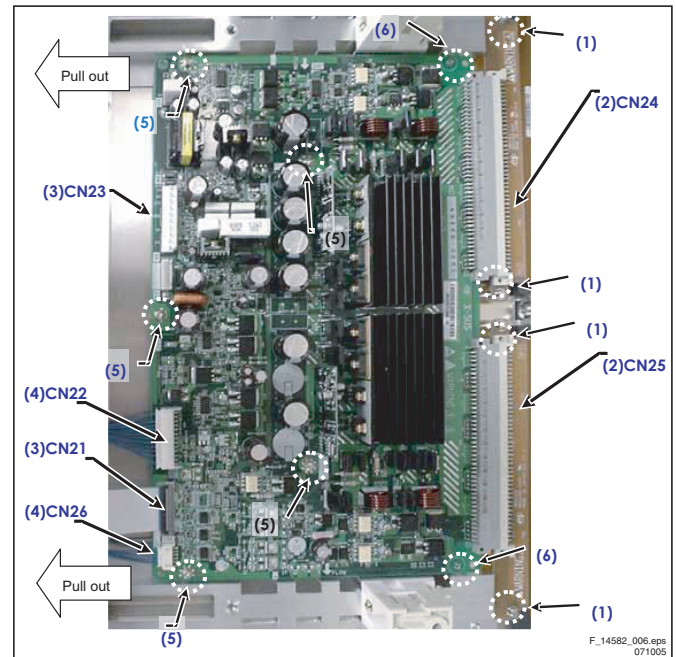


Figure 4-2 X-SUS board removal (1)

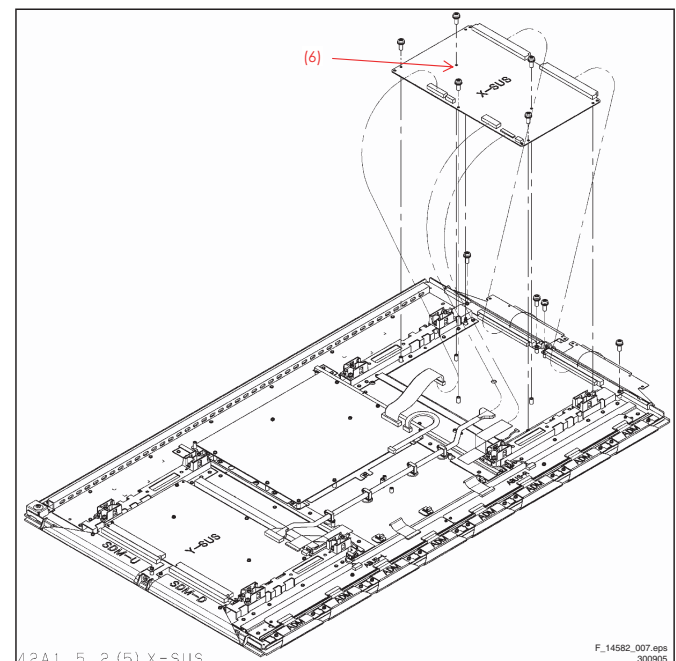


Figure 4-3 X-SUS board removal (2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

- Remove the fixing screws (M3 X 8).
- Release the lock of the FPC connector (CN21) and disconnect the signal cable.

3. Disconnect the connectors CN22, CN23 and CN26.
 4. Pull out the XSUS board horizontally and disconnect the connectors (CN24, CN25).
 5. Remove the X-SUS board.
- Make sure that you do not touch the heat sink when removing the Y-SUS board.

4.1.3 Y-SUS Circuit Board

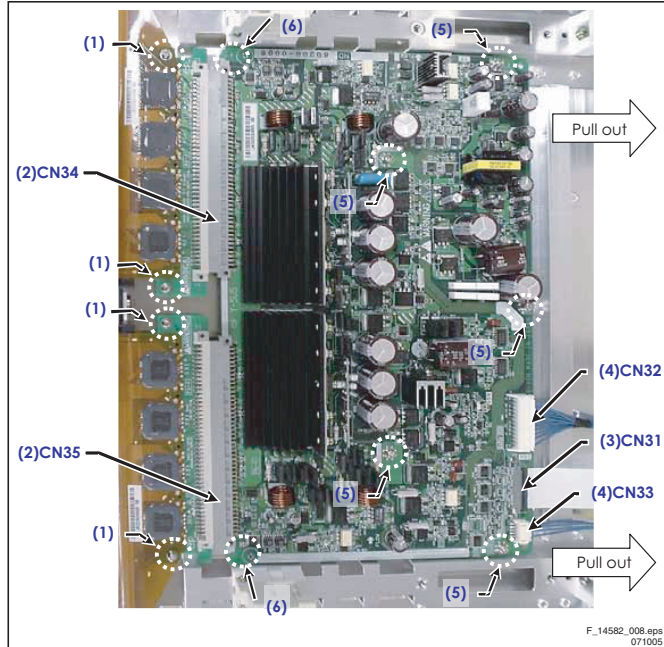


Figure 4-4 Y-SUS board removal (1)

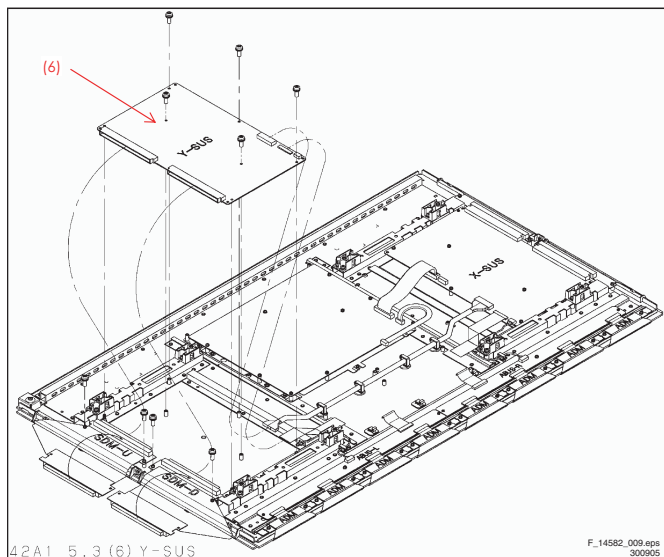


Figure 4-5 YSUS board removal (2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Remove the fixing screws (M3 X 8).
2. Release the lock of the FPC connector CN31 and disconnect the signal cable.
3. Disconnect the connectors CN32, CN33.
4. Pull out the YSUS board horizontally and disconnect the connectors (CN34, CN35).
5. Remove the Y-SUS board.

Make sure that you do not touch the heat sink when removing the Y-SUS board.

4.1.4 ABUS-L Circuit Board

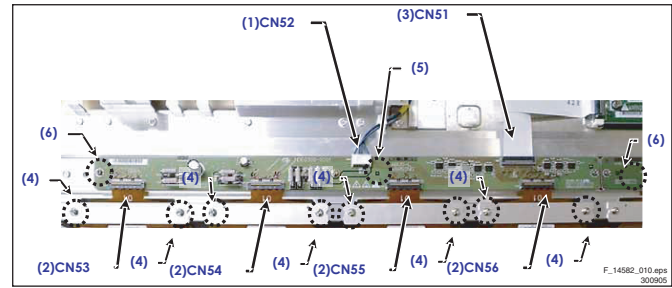


Figure 4-6 ABUS-L board removal (1)

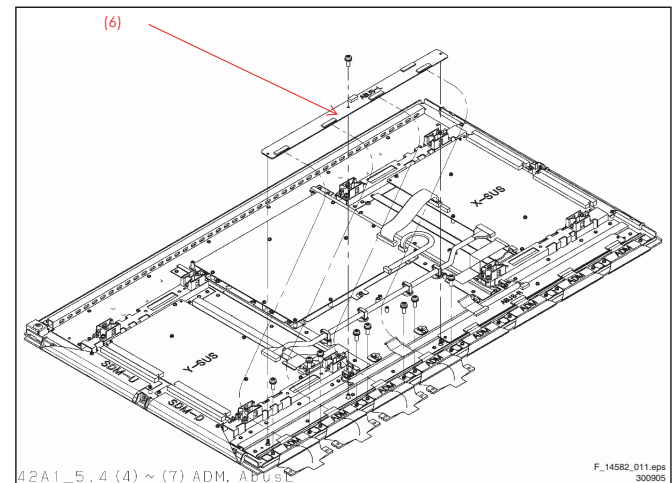


Figure 4-7 ABUS-L board removal (2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Disconnect the connector CN52 from the ABUS-L board.
2. Release the lock of the FPC connectors CN53, CN54, CN55 and CN56 and remove the ADM flexible board.
3. Release the lock of the FPC connector CN51 and disconnect the signal cable.
4. Remove the screws (M3X8) fixing the ADM.
5. Remove the screws (M3x8) fixing the ABUS-L board.
6. Remove the ABUS-L board.
7. When installing the ABUS L-board, put the board in such a position that it is locked by the tabs before fixing it with the screws.

4.1.5 ABUS-R Circuit Board

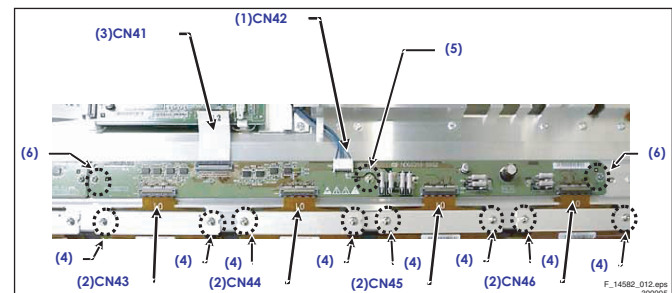


Figure 4-8 ABUS-R board removal (1)

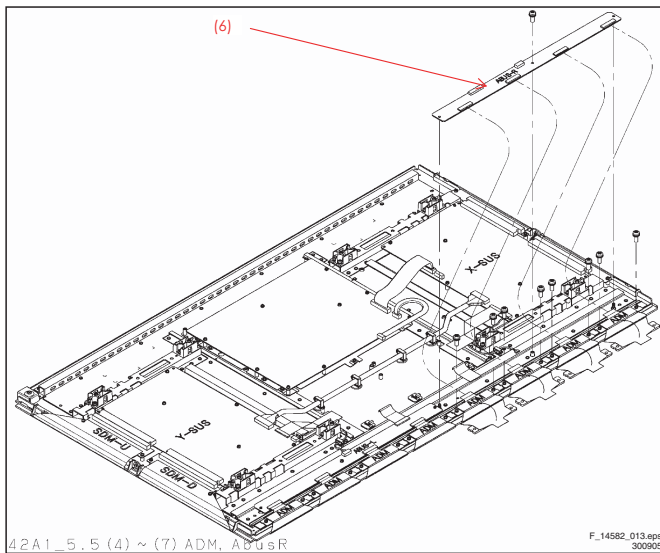


Figure 4-9 ABUS-R board removal (2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Disconnect the connector CN42 on the ABUS-R board.
2. Release the lock of the FPC connectors CN43, CN44, CN45, CN46 and disconnect the ADM flexible board.
3. Release the lock of the FPC connector CN41 and disconnect the signal cable.
4. Remove the screws (M3X8) fixing the ADM.
5. Remove the screws (M3X8) fixing the ABUS-R board.
6. Remove the ABUS-R board.
7. When installing the ABUS-R board, put the board in such a position that it is locked by the tabs before fixing it with the screws.

4.1.6 Logic Board

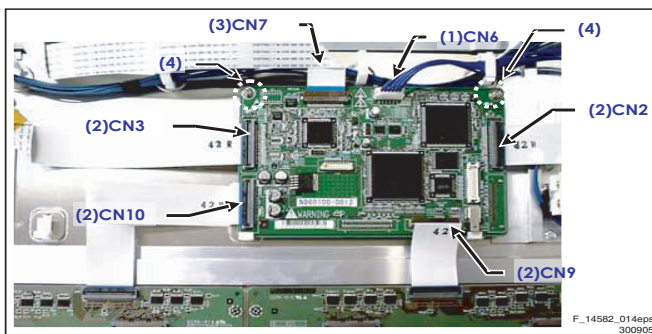


Figure 4-10 Logic board removal (1)

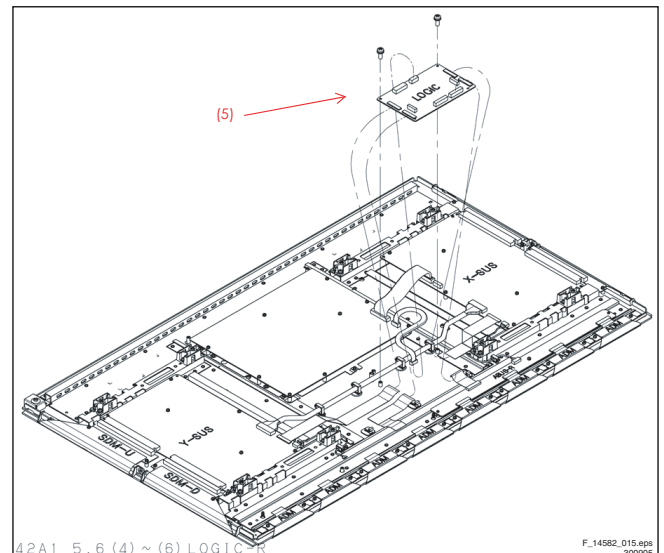


Figure 4-11 Logic board removal (2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Disconnect the EH connector CN6.
2. Release the lock of the FPC connectors CN2, CN3, CN4, CN5 and disconnect the signal cable.
3. Slide the lock of the FPC connector CN7 toward the PSU board side, then gently push it down toward the front and remove the PSU signal cable.
4. Remove the screws (M3 X 8) fixing the Logic board.
5. Remove the Logic board.
6. When installing the Logic board, put the board in such a position that it is locked by the tabs before fixing it with the screws.

4.1.7 PSU Board

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Release the lock of the large cable clamp.
2. Disconnect the X-SUS board connector CN23.
3. Disconnect the Y-SUS board connector CN33.
4. Disconnect the ABUSR board connector CN42.
5. Disconnect the ABUSL board connector CN52.
6. Remove the wires from the small cable clamp.
7. Disconnect the Logic board connector CN6.
8. Disconnect the PSU signal cable from the PSU board with connector CN69.

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

- 5.1 Repair Tools
- 5.2 Process Flow
- 5.3 Repair Instructions
- 5.4 Defect Description Form

5.1 Repair Tools

To be able to repair the Plasma Display Panels on board level, the following repair tools are available:

- Special LVDS cable: 9965 000 23434.
- Foam buffers: 3122 785 90581.

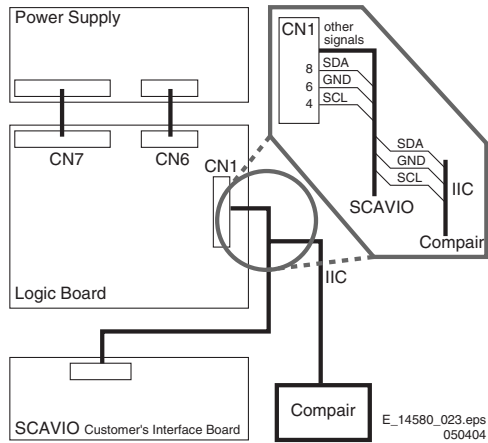


Figure 5-1 Extension cable kit ALiS PDP

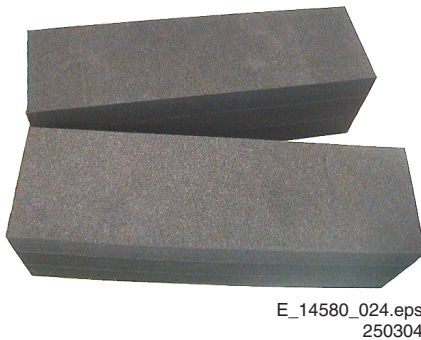


Figure 5-2 Foam buffers for FTV

5.2 Process Flow

The selected workshop receives the defect TV set and investigates the PDP. Two possible solutions follow:

5.2.1 Advanced PDP Exchange (Actual Way-of-working)

In case of:

- Glass broken,
- Flex foil damaged,
- Y-COM IC on flex foil is damaged, or
- NVM on logic board defect: no communication with ComPair

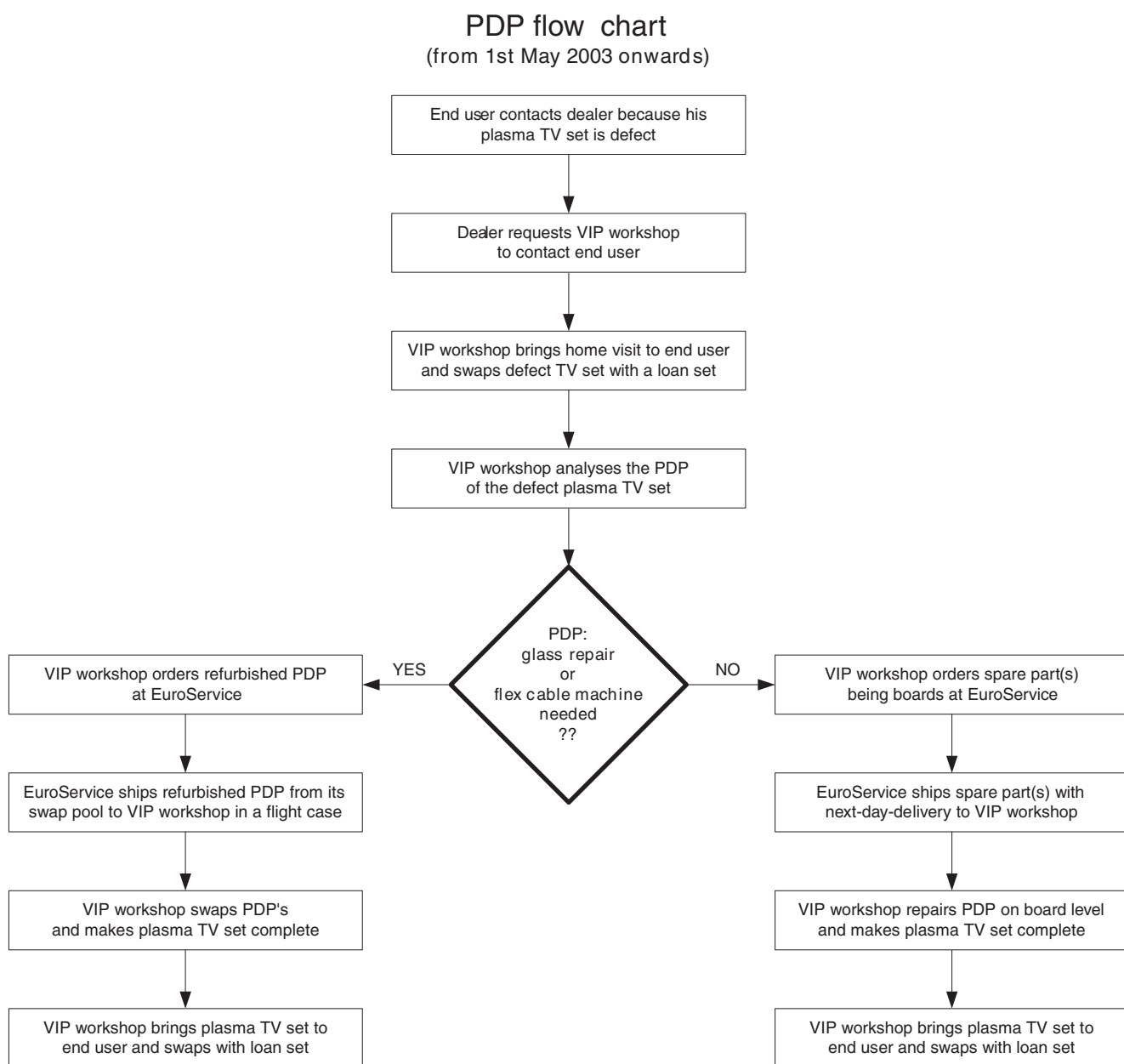
the procedure for repair is as follows:

A new PDP will be ordered at EuroService. They issue an RMA number and ship a refurbished PDP from its swap pool in a flight case to the workshop. After receipt, the workshop sends

the defective PDP, accompanied by a completely filled in Defect Description Form (see figure "Defect Description Form (DDF)"), in this flight case to EuroService. EuroService makes sure the defect PDP is repaired and afterwards added to its swap pool. The workshop makes the TV set complete by building in the refurbished PDP. Afterwards the TV set is returned to the customer.

5.2.2 Customized Repair

If the defect is not mentioned in 5.2.1, the workshop orders the necessary spare parts, being boards, at EuroService. After receipt the workshop swaps the concerning board and makes the TV set complete by building in the PDP. Afterwards the TV set is returned to the customer.



E_14580_027.eps
101005

Figure 5-3 PDP flow chart

5.3 Repair Instructions

5.3.1 General

In case of:

- a broken glass panel,
- a defective flex foil, or
- a defective Y-COM IC on the flex foil

the PDPs need to be send back via the central repair procedure of EuroService.

In other cases the Plasma Display Panels must be repaired on board level.

5.3.2 32" H1 ALiS Plasma Display Panel

These Plasma Display Panels are used in FM23 sets with production code AG00 up to and including AG05.

The involved Plasma Display Panels are:

Display type	Service code number	Production code
FPF32C106128UA-51	9322 172 11682	
FPF32C106128UA-52	9322 178 04682	
FPF32C106128UA-62	9322 190 61682	From AG06 0242 onwards

The available modules for the Plasma Display Panel FPF32C106128UA-51 and -52 are:

Module description	Factory code number	Service code number
X-SUS board	FPF17R-XSS5002	9965 000 17432
Y-SUS board	FPF17R-YSS5003	9965 000 17433
Logic board	FPF17R-LGC5012	9965 000 17435
ABUS Right	FPF17R-ABR5005	9965 000 17436
ABUS Left	FPF17R-ABL5004	9965 000 17437
Signal Cable (Logic - ABUS,SUS)	FPF17R-CBL2001	9965 000 17438
Signal Cable (XSUS-YSUS)	FPF17R-CBL1001	9965 000 17439

The available modules for the Plasma Display Panel FPF32C106128UA-62 are:

Module description	Factory code number	Service code number
X-SUS board	FPF17R-XSS5010	9965 000 17440
Y-SUS board	FPF17R-YSS5011	9965 000 17441
Logic board	FPF17R-LGC5013	9965 000 17442 * ₁
ABUS Right	FPF17R-ABR5005	9965 000 17436
ABUS Left	FPF17R-ABL5004	9965 000 17437
Signal Cable (Logic - ABUS,SUS)	FPF17R-CBL2001	9965 000 17438
Signal Cable (XSUS-YSUS)	FPF17R-CBL1001	9965 000 17439

5.3.3 32" H2 ALiS Plasma Display Panel

These Plasma Display Panels are used in FM23 sets with production code:

- AG07 and higher for the sets 32FD9954/17S and 32FD9954/69S
- AG08 and higher for the sets 32FD994/69S
- AG09 and higher for the sets 32FD9944/01S

The involved Plasma Display Panel is:

Display type	Service code number	Production code
FPF32C106128UB-72	932219411682	

The available modules for this Plasma Display Panel are:

Module description	Factory code number	Service code number
X-SUS board	FPF17R-XSS5016	9965 000 22709
Y-SUS board	FPF17R-YSS5017	9965 000 22710
Logic board	FPF17R-LGC5018	9965 000 22711 * ₁
ABUS Right	FPF17R-ABR5015	9965 000 22713
ABUS Left	FPF17R-ABL5014	9965 000 22712
Signal Cable (Logic - ABUS,SUS)	FPF17R-CBL2001	9965 000 17438
Signal Cable (XSUS-YSUS)	FPF17R-CBL1001	9965 000 17439

5.3.4 37" H2 ALiS Plasma Display Panel

These Plasma Display Panels are used in FM33 sets with production code AG00 and onwards.

The involved Plasma Display Panels are:

Display type	Service code number	Production code
FPF37C128128UA-72	9322 194 09682	

The available modules for these Plasma Display Panels are:

Module description	Factory code number	Service code number
X-SUS board	FPF18R-XSS5007	9965 000 23342
Y-SUS board	FPF18R-YSS5008	9965 000 23343
Logic board	FPF18R-LGC5009	9965 000 23344 * ₁
ABUS Right	FPF18R-ABR5005	9965 000 23346
ABUS Left	FPF18R-ABL5004	9965 000 23347
Signal Cable (Logic -ABUS,SUS)	FPF18R-CBL100103	9965 000 17431
Signal Cable (XSUS-YSUS)	FPF18R-CBL100103	9965 000 17431
Signal Cable (Logic - ABUS,SUS)	FPF18R-CBL200112	9965 000 17430
Signal Cable (XSUS-YSUS)	FPF18R-CBL200113	9965 000 23345

5.3.5 37" A1 ALiS Plasma Display Panel

These Plasma Display Panels are used in FM24 sets with production code AG00 and higher.

The involved Plasma Display Panel is:

Display type	Service code number	Production code
FPF37C128128UB-72	9322 217 56682	

The available modules for these Plasma Display Panels are:

Module description	Factory code number	Service code number
X-SUS board	FPF22R-XSS0003	9965 000 29948
Y-SUS board	FPF22R-YSS0009	9965 000 29949
Logic board	FPF22R-LGC0038	9965 000 29952
ABUS Right	FPF22R-ABL0014	9965 000 29951
ABUS Left	FPF22R-ABR0013	9965 000 29950
Signal Cable (Logic-ABUS, SUS)	FPF22R-CBL001201	9965 000 29944
Signal Cable (XSUS, YSUS)	FPF22R-CBL001221	9965 000 29945
Signal Cable (Logic-ABUS, SUS)	FPF22R-CBL001232	9965 000 29946
Signal Cable (XSUS, YSUS)	FPF22R-CBL001262	9965 000 29947
Power Cable	FPF22R-CBL000702	9965 000 29937
Power Cable	FPF22R-CBL000903	9965 000 29938
Power Cable	FPF22R-CBL000905	9965 000 29939

5.3.6 42" H1 ALiS Plasma Display Panel

These Plasma Display Panels are used in FM24 sets with production code AG00 and higher.

The involved Plasma Display Panel is:

Display type	Service code number	Production code
FPF42C128128UB-54	9322 185 78682	

The available modules for these Plasma Display Panels are:

Module description	Factory code number	Service code number
X-SUS board	FPF16R-XSS500203	9965 000 17423
Y-SUS board	FPF16R-YSS500303	9965 000 17424
Logic board	FPF16R-LGC5006	9965 000 17425 * ₁
ABUS Right	FPF16R-ABR5005	9965 000 17426
ABUS Left	FPF16R-ABL5004	9965 000 17427
Signal Cable (Logic-XSUS)	FPF16R-CBL200104	9965 000 17428
Signal Cable (Logic-YSUS)	FPF16R-CBL200106	9965 000 17429
Signal Cable (Logic-ABUS)	FPF18R-CBL200112	9965 000 17430
Signal Cable (XSUS-YSUS)	FPF18R-CBL100103	9965 000 17431

5.3.7 42" H2 ALiS Plasma Display Panel

These Plasma Display Panels are used in FM24 sets with production code:

- AG04 and higher for the sets 42FD9934/17S, 42FD9934/69S, 42FD9944/01S, 42FD9944/17S, 42FD9944/69S and 420P30/00
- AG06 and higher for the sets 42FD9954/69S

The involved Plasma Display Panel is:

Display type	Service code number	Production code
FPF42C128128UB-72	9322 194 10682	

The available modules for these Plasma Display Panels are:

Module description	Factory code number	Service code number
X-SUS board	FPF16R-XSS5008	9965 000 22704
Y-SUS board	FPF16R-YSS5009	9965 000 22705
Logic board	FPF16R-LGC500703	9965 000 22706 * ₁
ABUS Right	FPF16R-ABR5011	9965 000 22707
ABUS Left	FPF16R-ABL5010	9965 000 22708
Signal Cable (Logic-XSUS)	FPF16R-CBL200104	9965 000 17428
Signal Cable (Logic-YSUS)	FPF16R-CBL200106	9965 000 17429
Signal Cable (Logic-ABUS)	FPF18R-CBL200112	9965 000 17430
Signal Cable (XSUS-YSUS)	FPF18R-CBL100103	9965 000 17431

5.3.8 42" A1 ALiS Plasma Display Panel

The involved Plasma Display Panel is:

Display type	Service code number	Production code
FPF42C128128UC-52	9322 212 78682	

The available modules for these Plasma Display Panels are:

Module description	Factory code number	Service code number
X-SUS board	FPF23R-XSS 0005	9965 000 26824
Y-SUS board	FPF23R-YSS0010	9965 000 26825
Logic board	FPF23R-LGC0026	9965 000 26826
ABUS Right	FPF23R-ABR0002	9965 000 26823
ABUS Left	FPF23R-ABL0001	9965 000 26798
Signal Cable (Logic-ABUS, SUS)	FPF23R-CBL001203	9965 000 29940
Signal Cable (XSUS, YSUS)	FPF23R-CBL001223	9965 000 29941
Signal Cable (Logic-ABUS, SUS)	FPF23R-CBL001234	9965 000 29943
Signal Cable (XSUS, YSUS)	FPF23R-CBL001263	9965 000 29944
Power Cable	FPF23R-CBL000703	9965 000 29934
Power Cable	FPF23R-CBL000904	9965 000 29935
Power Cable	FPF23R-CBL000906	9965 000 29936

5.3.9 42" A2 ALiS Plasma Display Panel

The involved Plasma Display Panel is:

Display type	Service code number	Production code
FPF42C128128UD-52	9322 224 77682	

The available modules for these Plasma Display Panels are:

Module description	Factory code number	Service code number
X-SUS board	FPF28R-XSS0026	9965 000 32353
Y-SUS board	FPF28R-YSS0027	9965 000 32354
Logic board	FPF28R-LGC0045	9965 000 32352
ABUS Right	FPF28R-ABR0020	9965 000 32356
ABUS Left	FPF28R-ABL0019	9965 000 32355
Signal Cable (Logic-XSUS)	FPF28R-CBL003303	9965 000 32357
Signal Cable (Logic-YSUS)	FPF26R-CBL002611	9965 000 32358
Signal Cable (Logic-ABUS)	FPF28R-CBL003103	9965 000 32359
Signal Cable (XSUS-YSUS)	FPF26R-CBL002621	9965 000 32370

5.3.10 42" A3 ALiS Plasma Display Panel

The involved Plasma Display Panel is:

Display type	Service code number	Production code
FPF42C128128UE-52	9322 227 20682	

The available modules for these Plasma Display Panels are:

Module description	Factory code number	Service code number
X-SUS board	FBF29R-XSS0037	9965 000 32663
Y-SUS board	FPF29R-YSS0038	9965 000 32664
Logic board	FPF29R-LGC057	9965 000 32662
ABUS Right	FPF29R-ABR0031	9965 000 32666
ABUS Left	FPF29R-ABL0030	9965 000 32665
ABUS	FPF29R-ABR0026	9965 000 32667
Signal Cable (Logic-XSUS)	FPF29R-CBL001411	9965 000 32669
Signal Cable (Logic-YSUS)	FPF29R-CBL001412	9965 000 32670
Signal Cable (Logic-ABUS)	FPF29R-CBL001401	9965 000 32668
Signal Cable (XSUS, YSUS)	FPF29R-CBL003601	9965 000 32672
Signal Cable (Logic-ABUS)	FPF29R-CBL001421	9965 000 32671
PSU Cable (XSUS-ABUSR)	FPF29R-CBL003701	9965 000 32673

Remark:

*1) If the Logic board is defective, the procedure mentioned in figures "Logic Board Exchange (1 and 2)" must be used.

5.3.11 Fault Finding Flowcharts

Problem analysis procedure PDP repair / Board swap

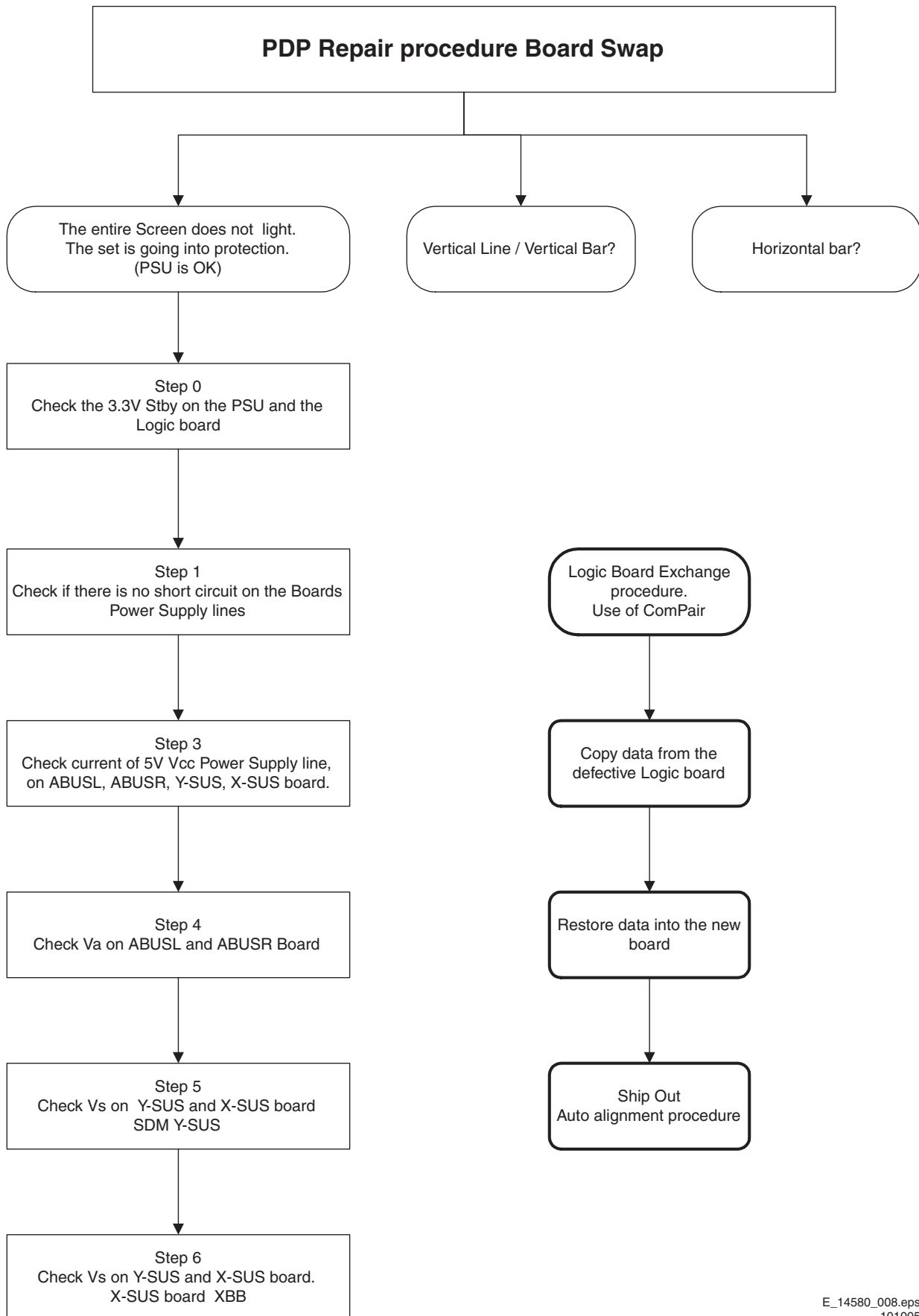


Figure 5-4 Problem analysis procedure PDP repair / board swap

Problem Analysis Procedure the entire screen does not light.

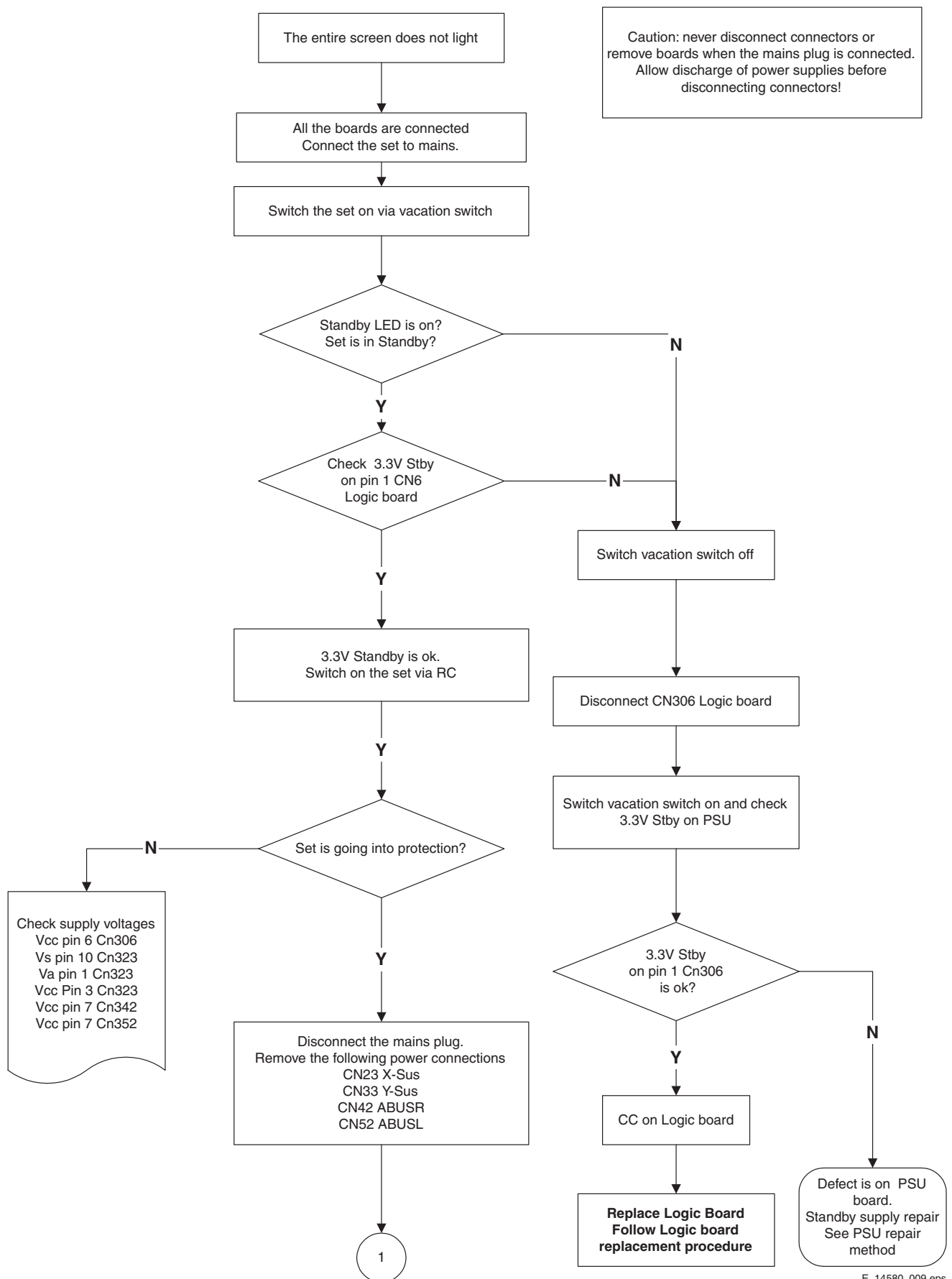


Figure 5-5 Problem analysis procedure the entire screen does not light

Short-circuit check on Power Supply Lines

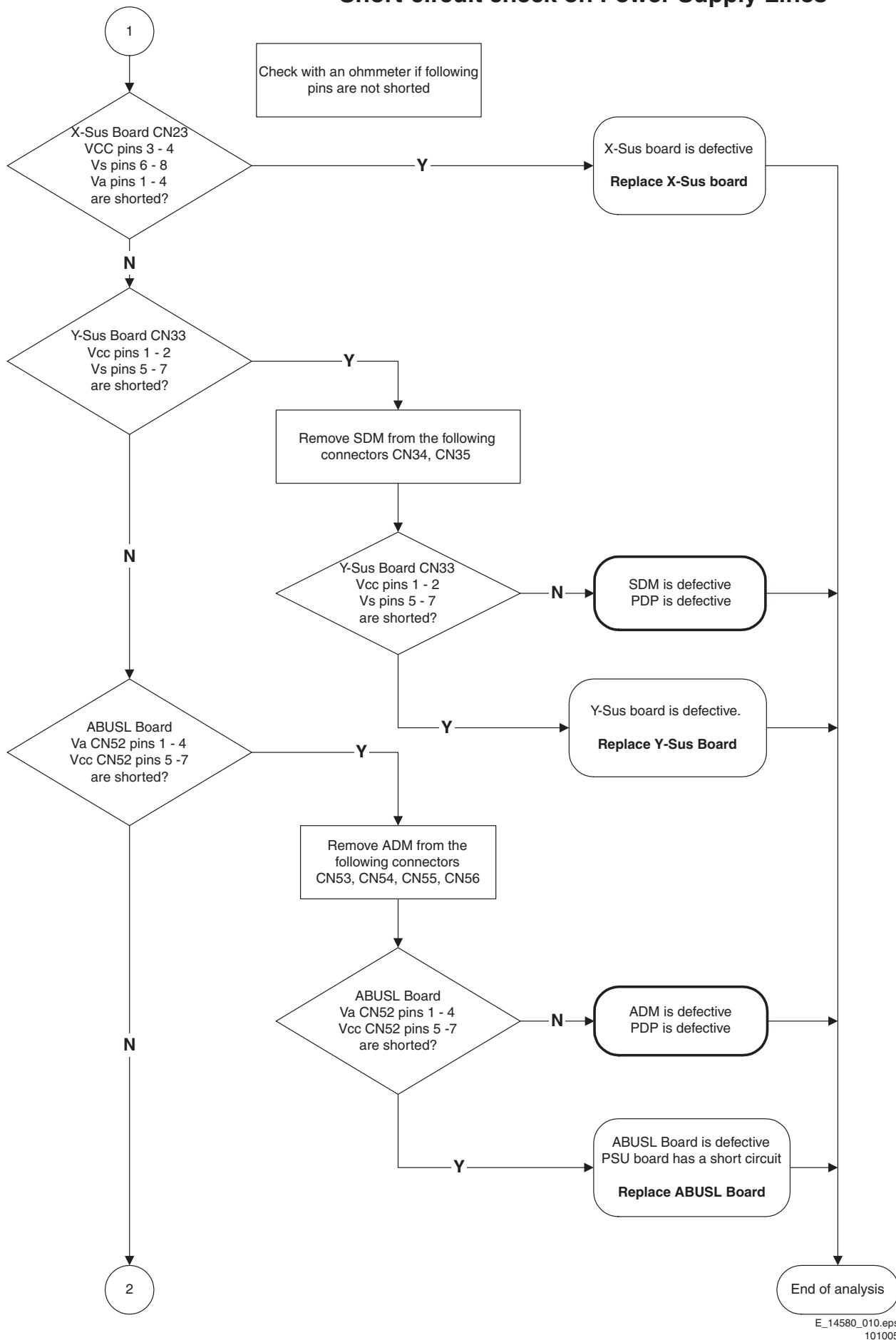


Figure 5-6 Short circuit check on power supply lines (1/2)

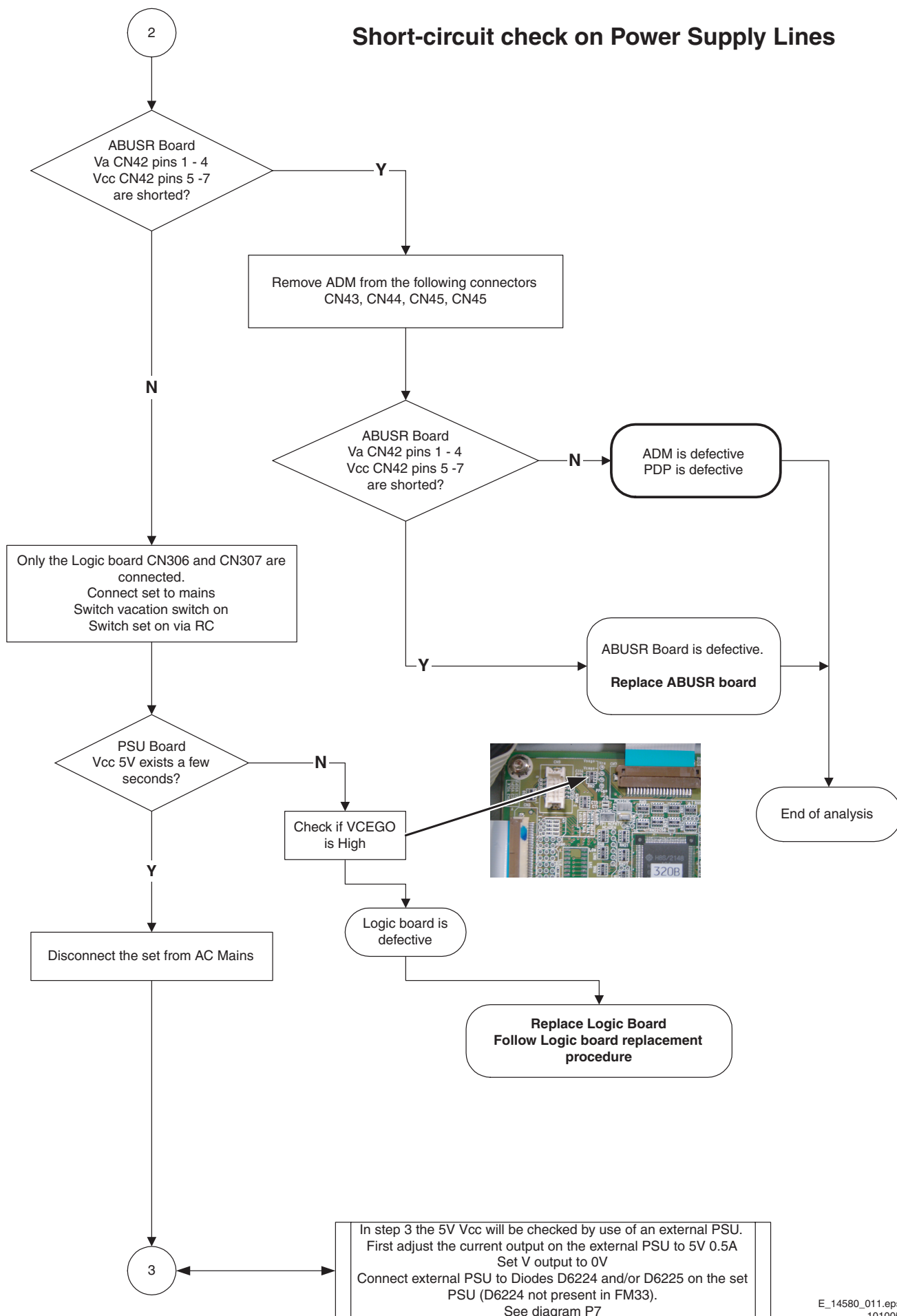


Figure 5-7 Short circuit check on power supply lines (2/2)

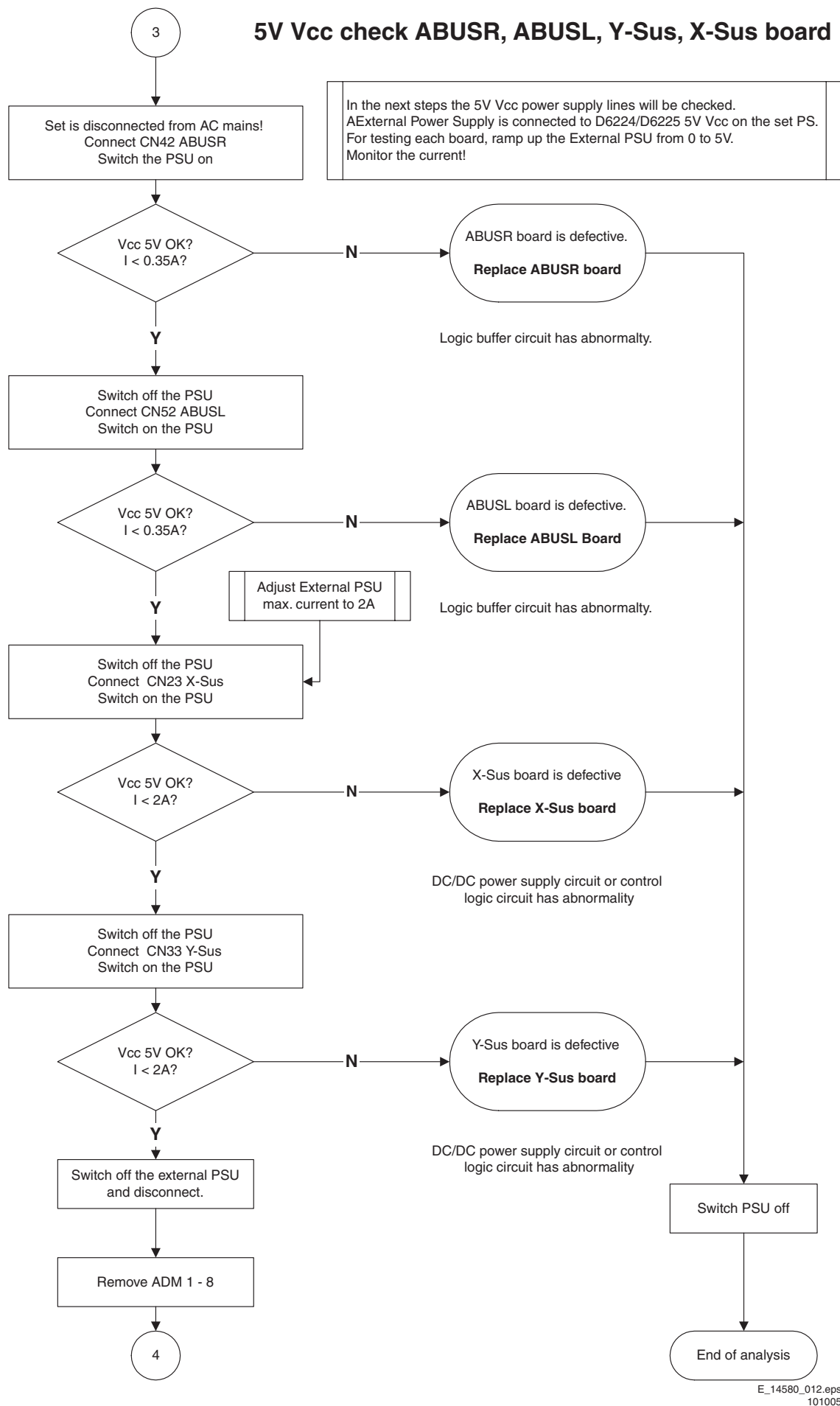


Figure 5-8 5V Vcc check ABUSR, ABUSL, Y-Sus X-Sus board

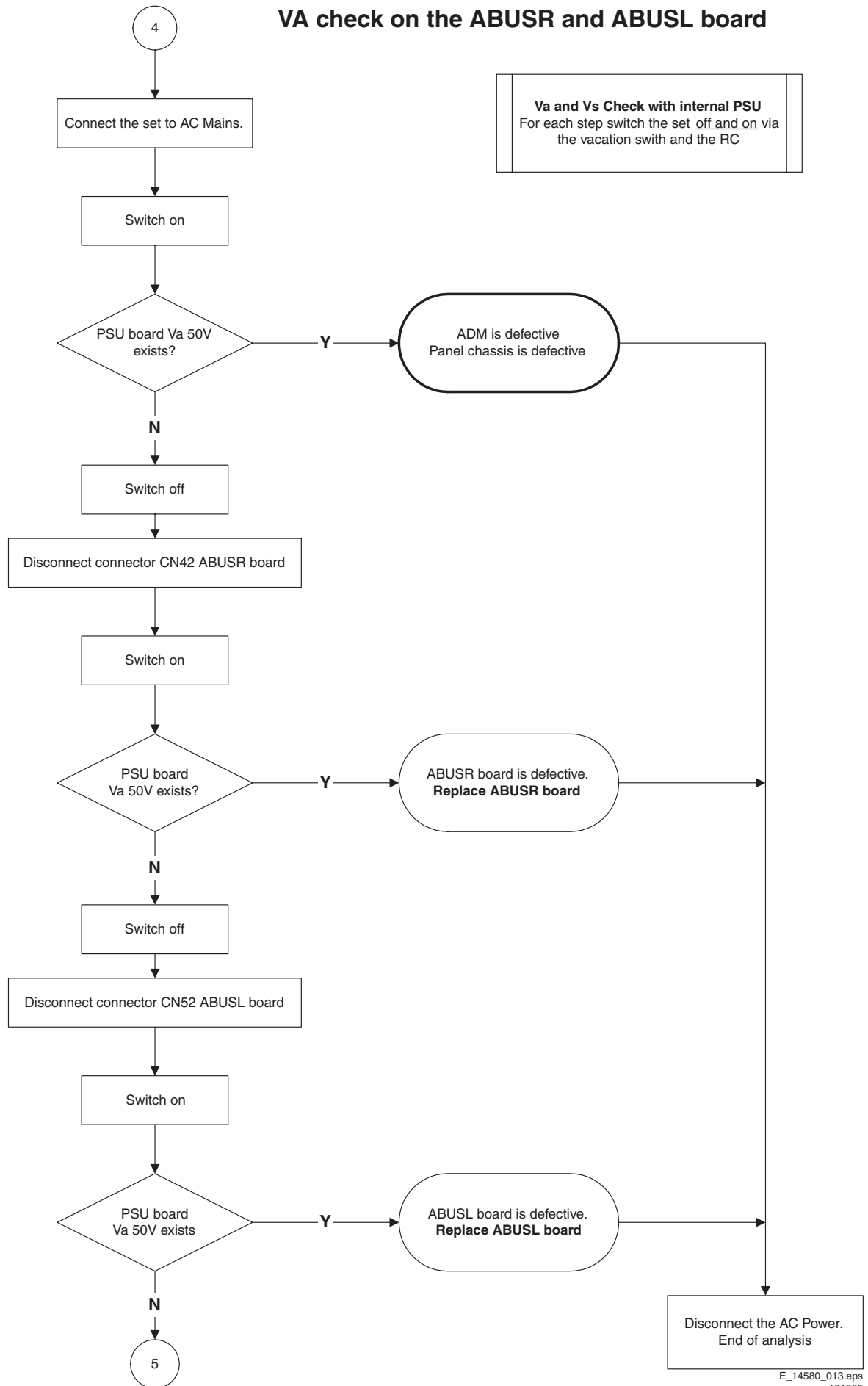


Figure 5-9 VA check on the ABUSR and ABUSL board

Vs Check on Y-Sus & X-Sus board and SDM / XBB

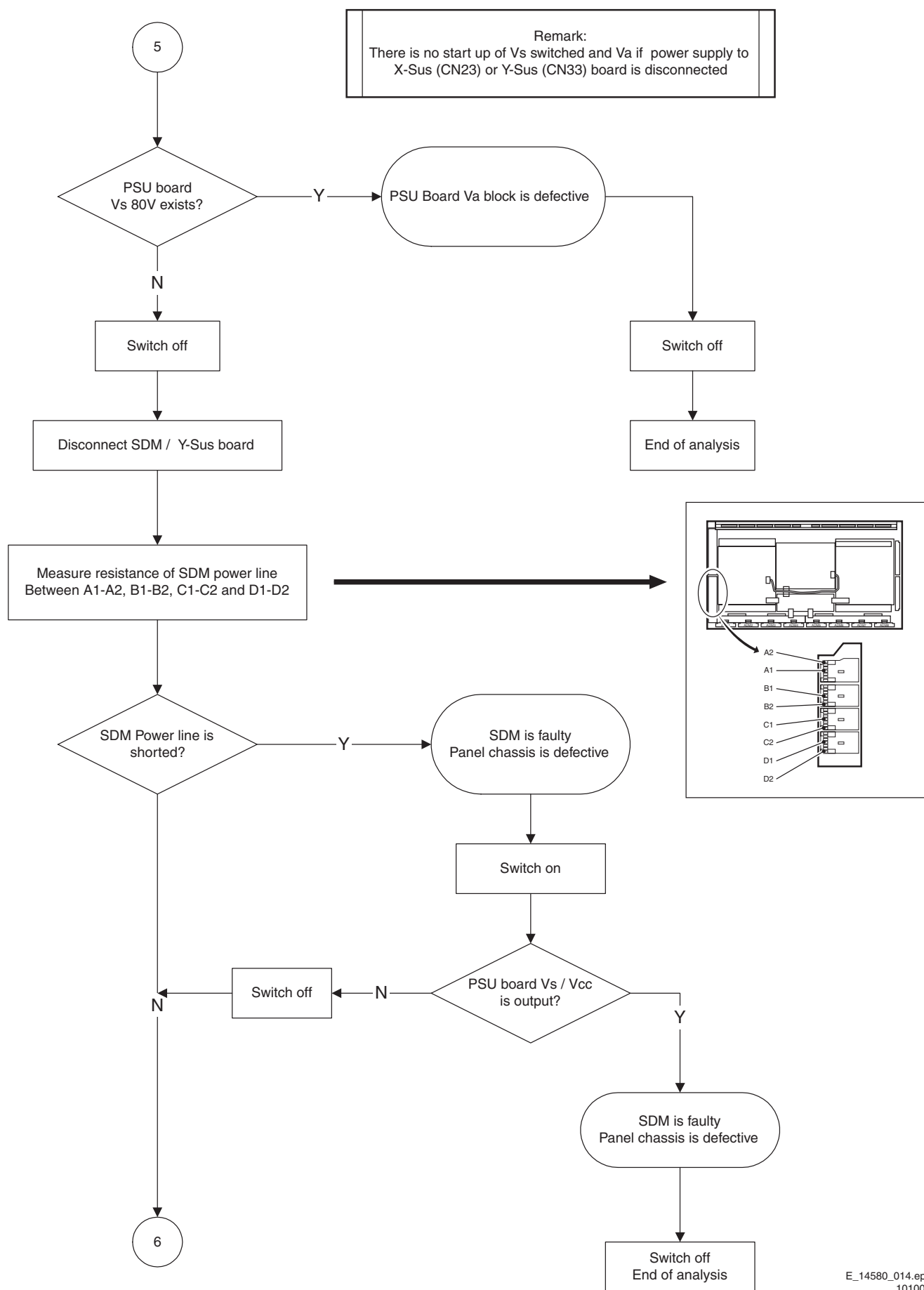


Figure 5-10 Vs check on the Y-Sus and X-Sus board, and SDM / XBB (1/2)

Vs Check on Y-Sus & X-Sus board and SDM / XBB

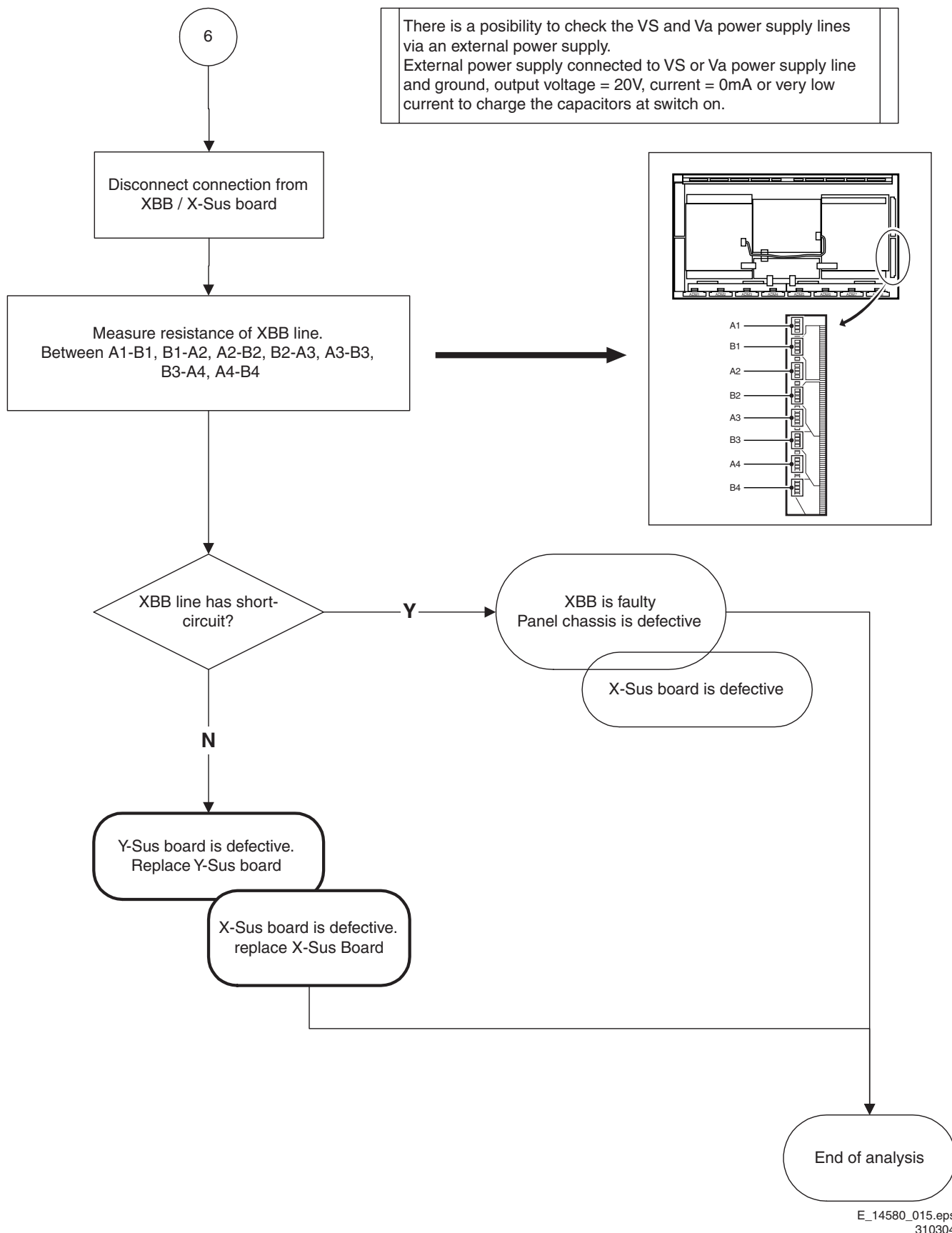
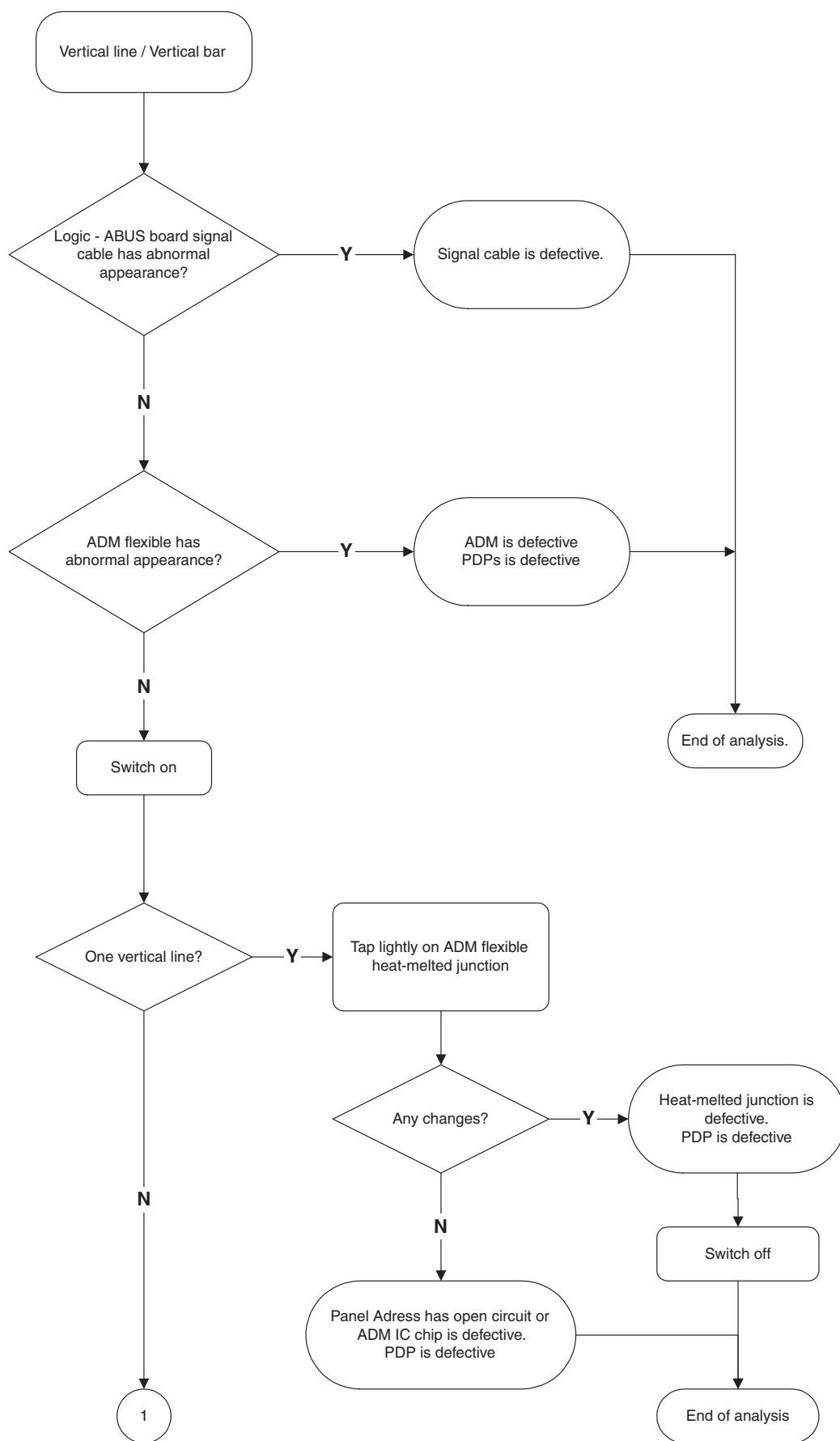


Figure 5-11 Vs check on the Y-Sus and X-Sus board, and SDM / XBB (2/2)

Vertical Line / Vertical bar Problem analysis procedure



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Figure 5-12 Vertical line / vertical bar problem analysis procedure (1/4)

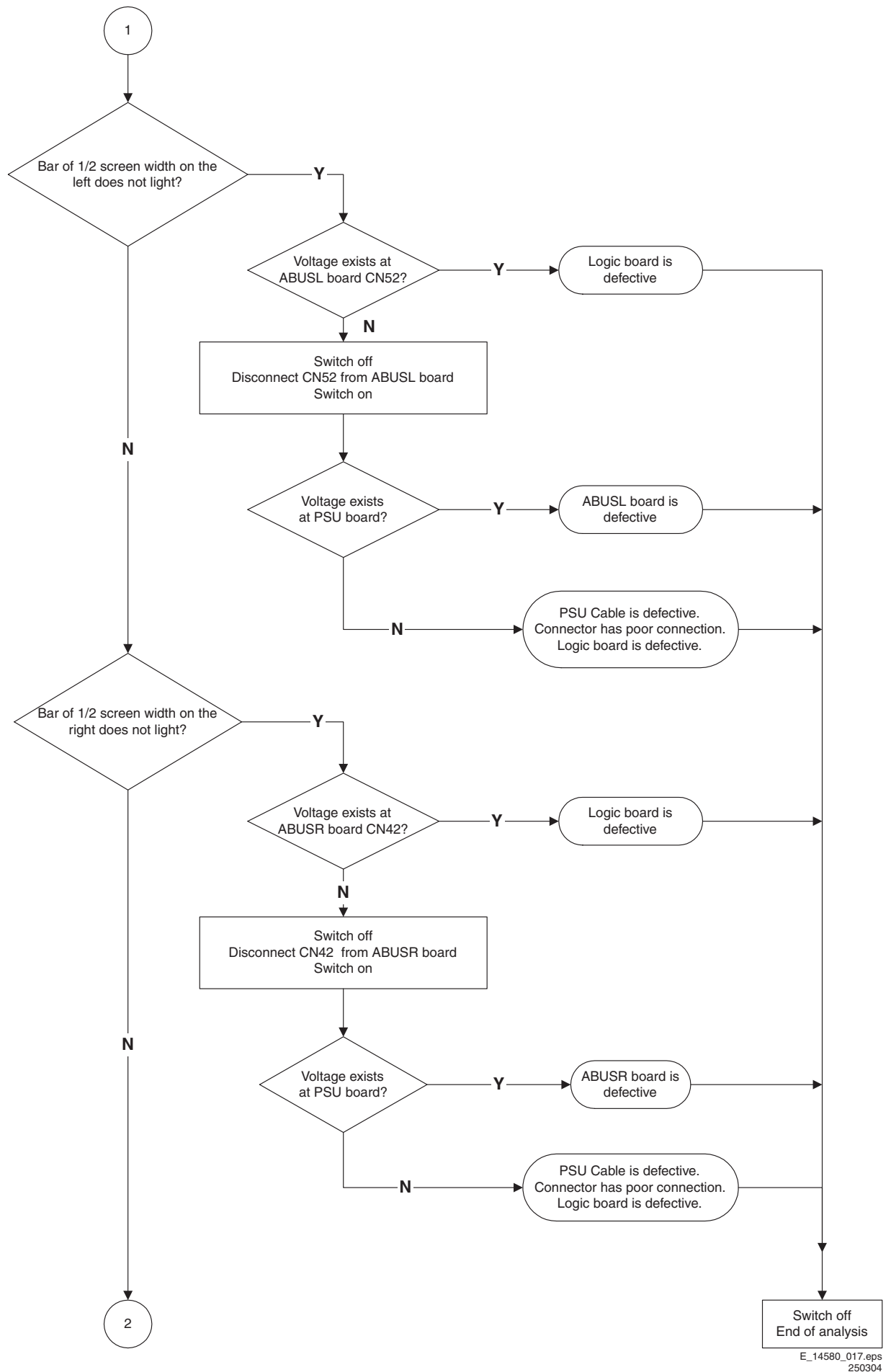


Figure 5-13 Vertical line / vertical bar problem analysis procedure (2/4)

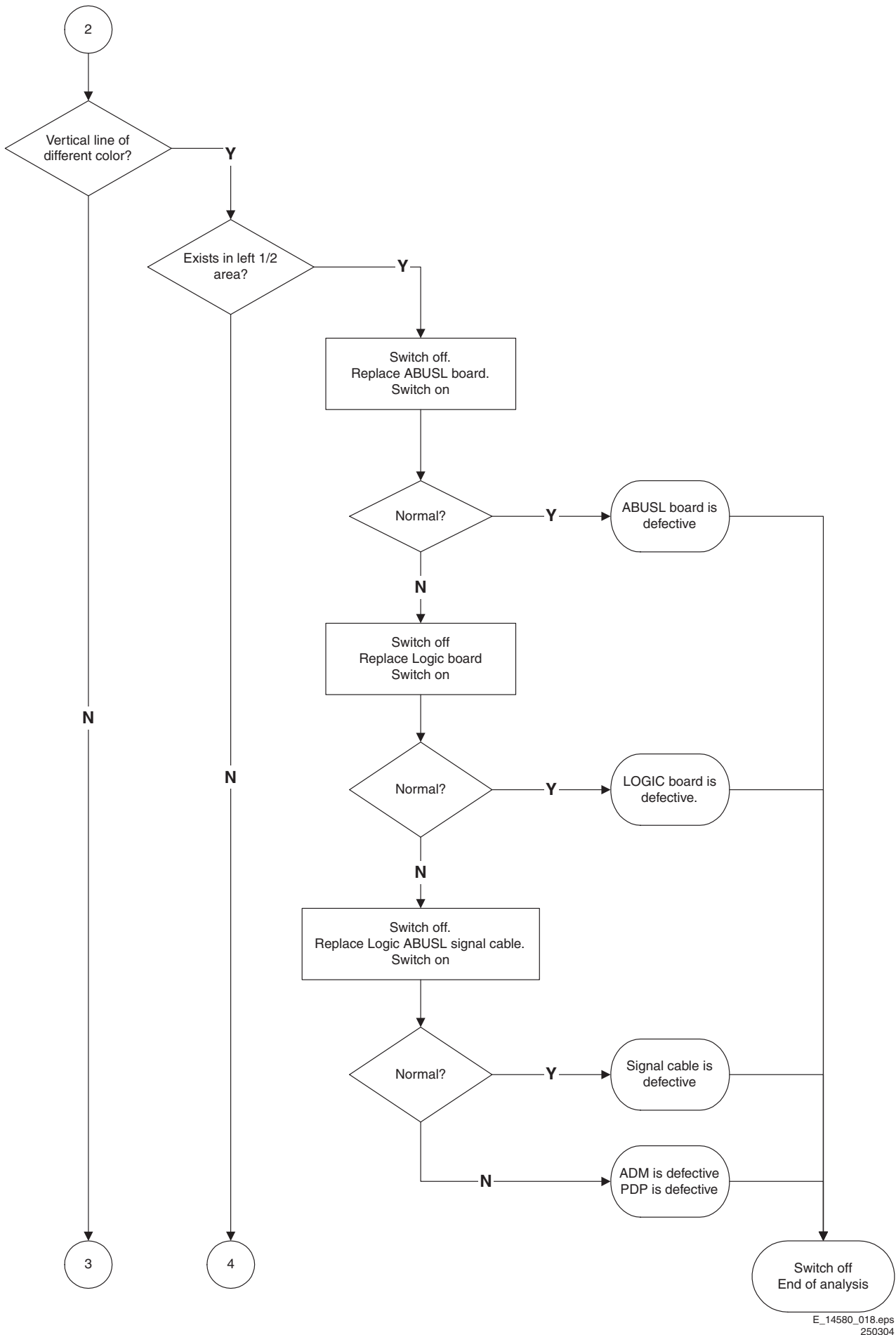


Figure 5-14 Vertical line / vertical bar problem analysis procedure (3/4)

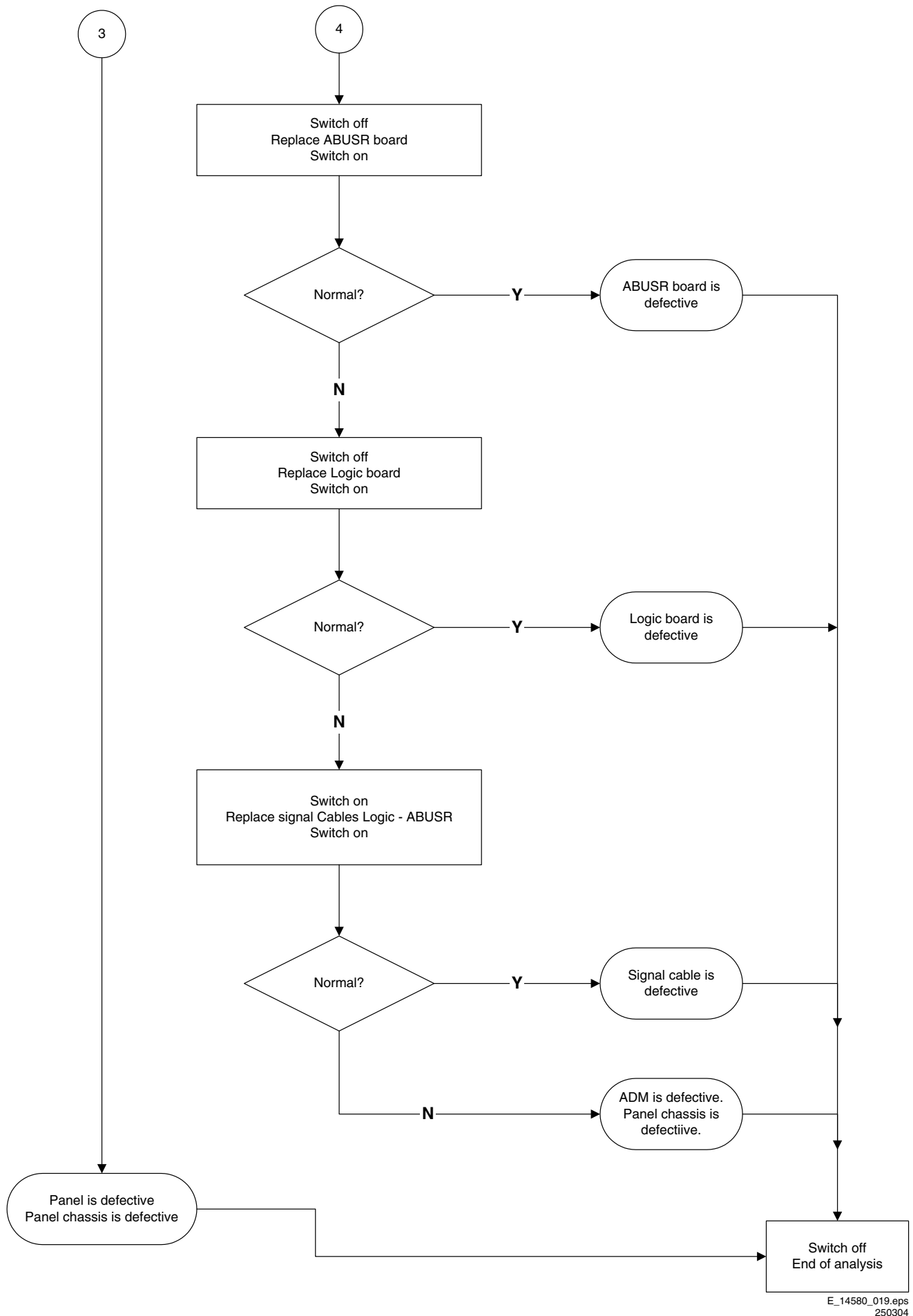


Figure 5-15 Vertical line / vertical bar problem analysis procedure (4/4)

Horizontal bar problem analysis procedure

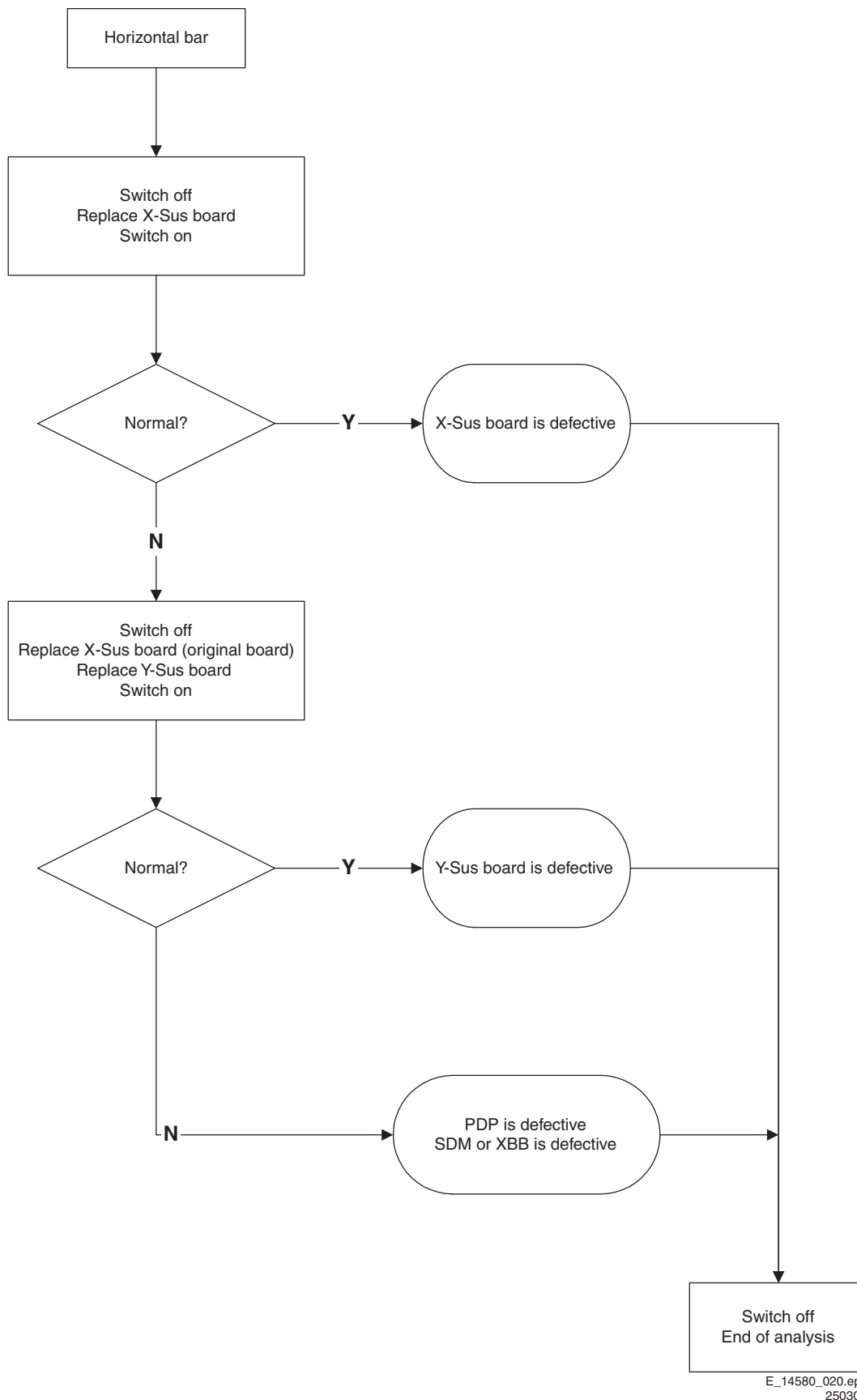
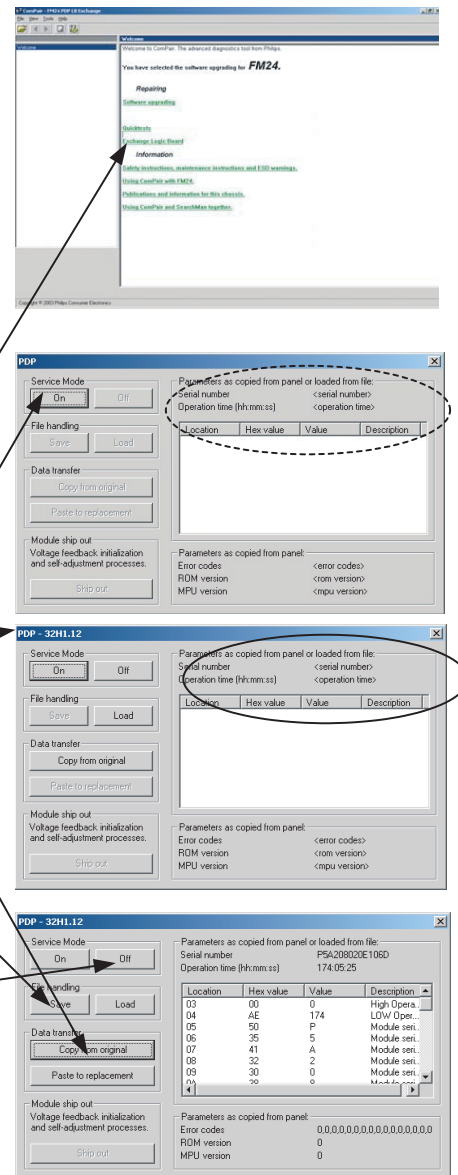
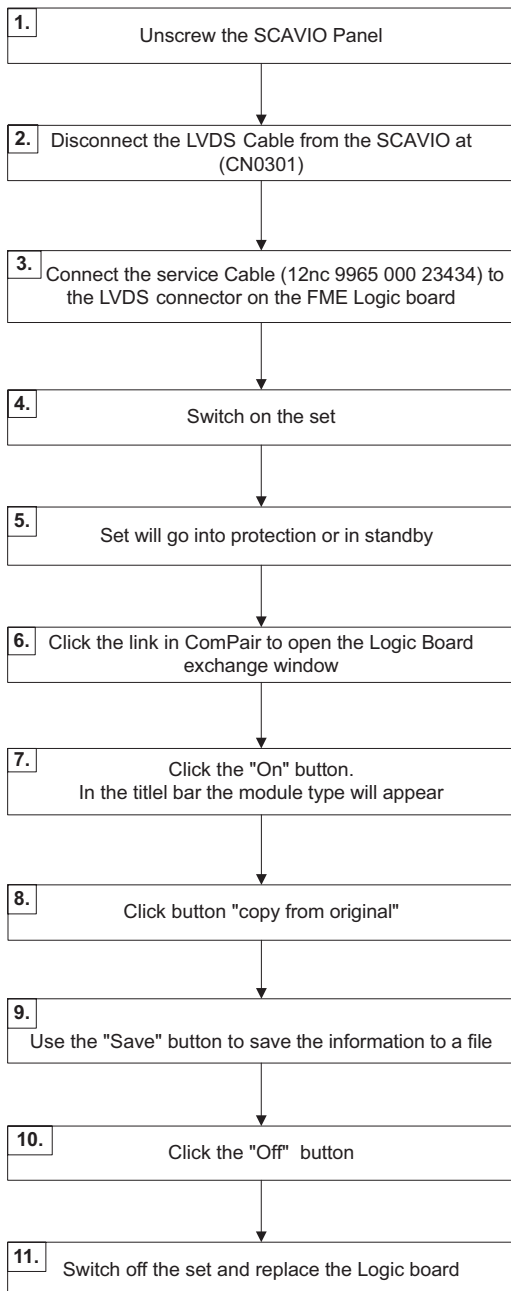


Figure 5-16 Horizontal bar problem analysis

Remark: Do not interchange boards between different PDPs, this can damage your PDP

Logic Board Exchange (1)

1. Copy NVM Data from defective Logic Board



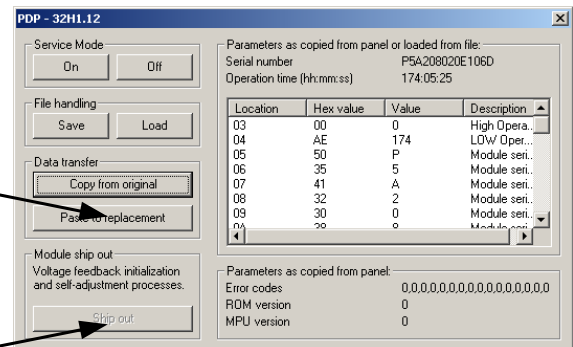
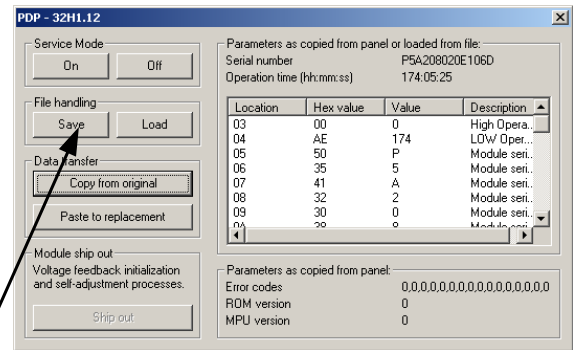
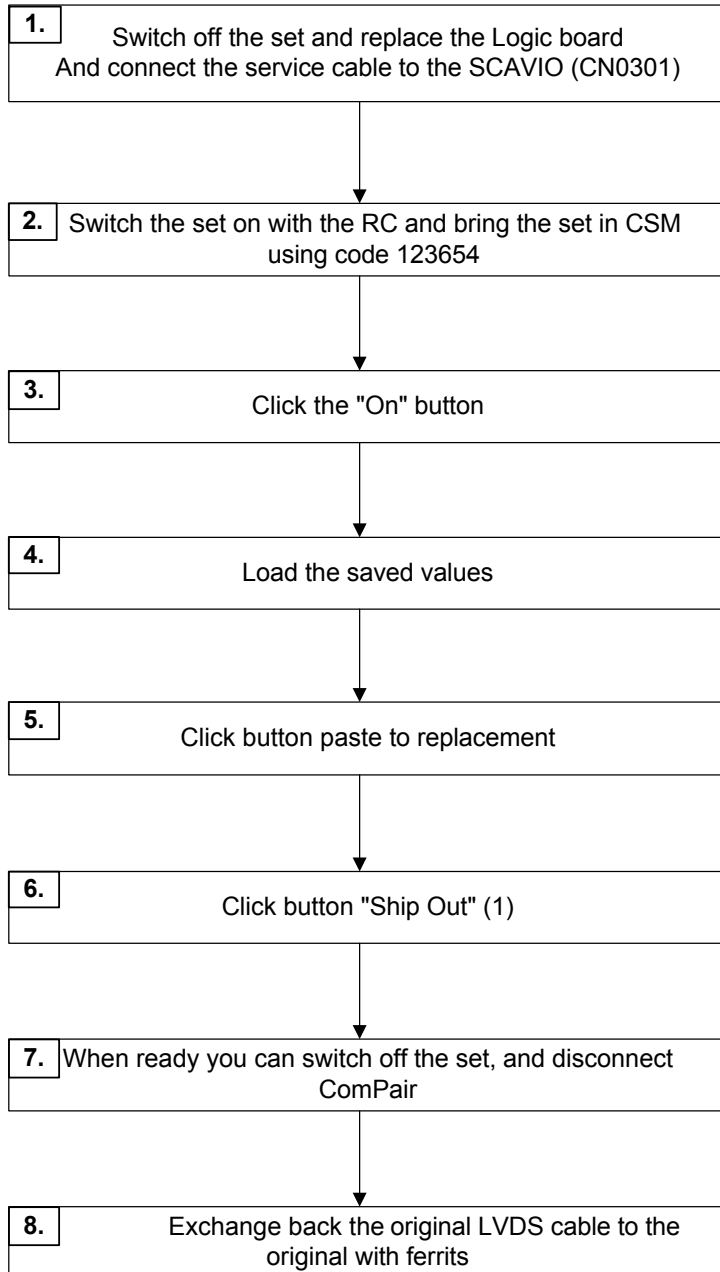
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111005

Figure 5-17 Logic Board Exchange (1/2)

- Unscrew the SCAVIO panel. Now you can reach the cable going to connector CN1 on the Logic Board
- Disconnect the cable from the SCAVIO panel at connector 0301. Leave the rest connected!
- Connect the ComPair I2C cable as given in this diagram.
- Switch on the set. It will go to stand-by or protection mode.
- Click the link in ComPair to open the Logic Board exchange window.
- Click the 'On' button. In the title bar the module type will appear: 37H1.11, 42H2, or something similar.
- Click button 'Copy from original'
- The data is read from the EEPROM on the logic board and displayed in the list.
- Use the 'Save' button to save the information to a file. This is optional, but better safe than sorry!
Note: If you close the window without saving, all settings will be lost. If you intend to close this window before replacing the board, you should save the settings so you can load them later.
- Click the 'Off' button.
- Switch off the set and replace the Logic Board with another one.

Logic Board Exchange (2)

2. Write NVM Data to the new Logic Board



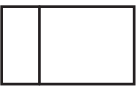
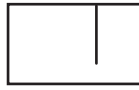
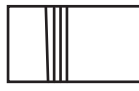

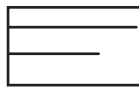



(1) The PDP screen will be blanked for about 15s, then 15s later, the 'Ship out' process will end

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Figure 5-18 Logic Board Exchange (2/2)

1. Switch off the set and replace the Logic Board with another one. Now also connect the cable to connector 0301 as depicted in the diagram above.
2. Restart the set with the new board. Switch on the set with the remote control and activate CSM (123654). This is to prevent the set to switch off because no input devices are connected.
3. Click the 'On' button.
4. The module type will again appear in the title bar. This may be different now from step 7 because another Logic Board is used. If you closed the window after step 9 and did save the settings you should load them now. Use the Load button to do so.
5. Click button 'Paste to replacement'. The settings previously copied from the old board are now written to the new board. If successful the button 'Ship out' will be enabled.
6. Click button 'Ship out'.
7. Now a process of voltage feedback initialization and self-adjustment starts. This will take a few seconds. When ready you can switch off the set, disconnect ComPair and restart the set again to test.
8. Exchange the service LVDS cable with the original LVDS cable.

No	Fault contents	Fault status	Suspected fault location	Analysis procedure and measure
1	Entire screen does not light.	After momentarily going on, the screen becomes black immediately or after a few seconds. Main power is turned off.	 X-SUS, Y-SUS PSU Panel chassis LOGIC ABUSL ABUSR	Refer to the entire screen does not light.
2		Screen lights dimly even on the back screen	 LOGIC	Replace LOGIC board and follow Logic Board exchange procedure
3	Vertical Line	Single vertical line (of different color)	 Panel chassis LOGIC	Refer to vertical Line / bar..
4		Vertical line from the middle of effective scan area (Vertical line of different color)	 Panel chassis	Replace panel chassis
5	Vertical bar	Bar width of 1/7 of horizontal size or in multiples of 1/7, is displayed. Abnormal display.	 Panel chassis ABUSL ABUSR LOGIC Above boards are connected	Refer to vertical Line / bar..
6		Bar width of 3/7 or 4/7 of the screen width, is displayed. Abnormal display. (Vertical line of different color)	 Panel chassis ABUSL ABUSR LOGIC Above boards are connected	Refer to vertical Line / bar..
7	Horizontal line	Single horizontal line (No light) or single horizontal does not light among the effective scanning area. Single horizontal line does not light	 Panel chassis	Replace panel chassis
8		Every other line (No light) Entire screen	 X-SUS Y-SUS	Replace X-SUS Y-SUS board

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Figure 5-19 Fault symptom overview (1/3)

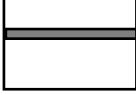

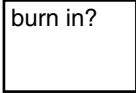

No	Fault contents	Fault status		Suspected fault location	Analysis procedure and measure
9	Horizontal bar	Bar width of 1/8 or multiples of 1/8 of the screen height, is displayed Abnormal (Screen does light)		Panel chassis	Replace panel chassis
10		Bar width of 1/2 of the screen height. Abnormal display (Screen does not light)		Panel chassis Y-SUS, X-SUS Above boards are connected	Refer to horizontal bar.
11	Image sticking. Burn in?	Fixed display contents are always displayed.		Panel chassis	Perform all white heat run. After judgment, replace panel chassis if needed.
12	Stains	Oval-shaped points having abnormal luminance are scattered in the upper or lower part of screen.		Panel chassis	Perform all white heat run. After judgment, replace panel chassis.
13	Twinkle	The entire screen momentarily becomes brighter or darker.		Poor connector contact. Panel chassis	
14	Flicker	The entire screen flickers continuously		Poor connector contact. FFC (Flat Foil connector Cable)	Connector / cable reconnection or Cable Exchange
15	Luminance is abnormal	Screen is too dark or too bright. (Out of specifications)			
16	Chrominance is abnormal	Colors cannot be displayed orrectly.		LOGIC	Replace LOGIC board and folow Logic Board echange procedure
17	Sync is disturbed			LOGIC	

Figure 5-20 Fault symptom overview (2/3)

No	Fault contents	Fault status		Suspected fault location	Analysis procedure and measure
18	Picture distorted			LOGIC	Replace LOGIC board and follow Logic Board exchange procedure
19	Steps of gradations are skipped	Luminance linearity is poor.		LOGIC	
20	Abnormal sound			PSU, X-SUS Y-SUS (Core is broken, or transformer is abnormal)	Locate cause of abnormality from listening and viewing. Replace the cause of problem
21	Control on external communication is abnormal	Contrast, color temperature adjustment and Y cannot be changed.		LOGIC	Replace LOGIC board and follow Logic Board exchange procedure

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Figure 5-21 Fault symptom overview (3/3)

5.4 Defect Description Form

This form must be used by the workshops for warranty claims:

DDF FLAT TV (panels & boards) version 1.1				Date last modified: 08/03/2005		
To be filled in by <u>WORKSHOP / WORK CENTER</u>						
Country:		<div style="font-size: 24px; font-weight: bold; margin-bottom: 10px;">Philips</div> <div style="font-size: 18px; font-weight: bold; margin-bottom: 10px;">LCD & Plasma</div> <div style="font-size: 16px; font-weight: bold; border-bottom: 1px solid black; margin-bottom: 5px;">DEFECT DESCRIPTION</div> <div style="font-size: 16px; font-weight: bold; border-bottom: 1px solid black;">FORM</div>		Type nr./Model nr. set		
Customer Account nr.:				Serial nr. set		
				Type nr. display		
Job sheet nr.:				Serial nr. display		
		Part nr display (12nc)				
		Return number		0170 _ _ _ _ _		
GENERAL REPAIR DATA	Condition	<input type="checkbox"/> Constantly <input type="checkbox"/> Intermittently <input type="checkbox"/> After a while <input type="checkbox"/> In a hot environment <input type="checkbox"/> In a cold environment <input type="checkbox"/> Other :				
	Symptom(s)	<input type="checkbox"/> No backlight <input type="checkbox"/> No picture <input type="checkbox"/> Picture too bright <input type="checkbox"/> Shading / smearing on picture <input type="checkbox"/> Only partial picture <input type="checkbox"/> Unstabel picture <input type="checkbox"/> Flickering / flashing picture <input type="checkbox"/> Lines across/down image <input type="checkbox"/> Inactive row(s) <input type="checkbox"/> Inactive column(s) <input type="checkbox"/> Missing colour(s) <input type="checkbox"/> Other:				
PANEL REPAIR	Pixel Defect(s):	<input type="checkbox"/> Dark dots <input type="checkbox"/> Bright dots	<u>Qty of dots :</u>	Mark Defect(s)	<div style="color: red; font-weight: bold; font-size: 1.2em; margin-bottom: 5px;">----- Picture -----</div> Insert picture or mark defect !	
	Symptoms	Following defect symptoms are out of warranty: <div style="display: flex; justify-content: space-between;"> <div> <ul style="list-style-type: none"> Broken glass Scratch(es) on display </div> <div> <ul style="list-style-type: none"> Number of dark/bright pixels within spec. Burn in (only for Plasma TV) </div> </div>			These symptoms are not claimable.	
BOARD REPAIR	<u>For Plasma TV repair only</u>		Spare Part Nr. New Board	Barcode Nr. Defect Board	Barcode Nr. Replaced Board	
			1.			
			2.			
			3.			
			4.			
To be filled in by <u>EUROSERVICE</u> RMA number: Date of receipt:						
Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected. Note 2: Please fill out this form <u>completely</u> and correctly, otherwise Euroservice is unable to fulfil the repair request!						
Owner: PHILIPS CE EUROSERVICE DE10WEG						

Figure 5-22 Defect Description Form (DDF)

6. Block Diagrams, Test point Overview, and Waveforms

6.1 Block Diagrams

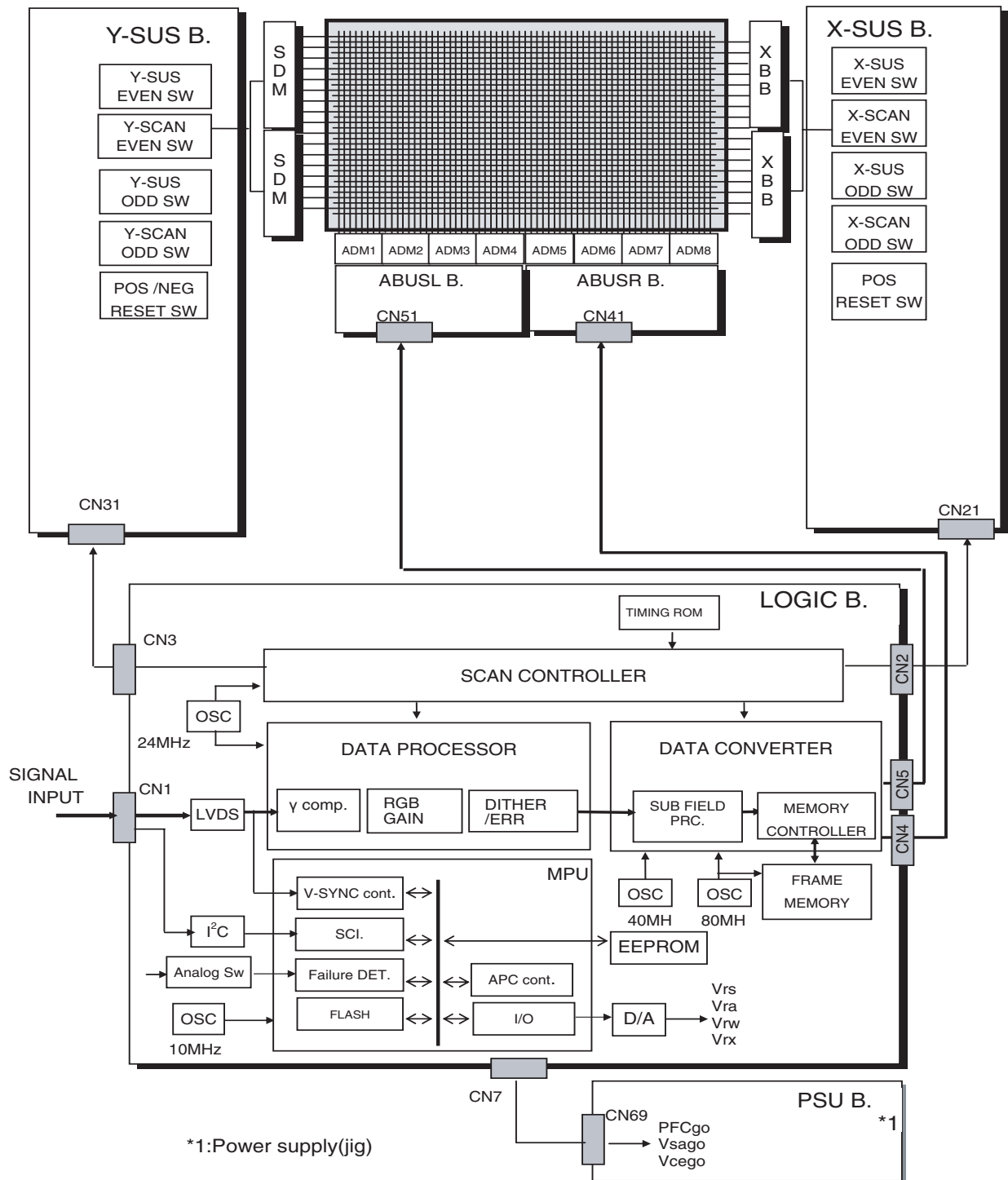
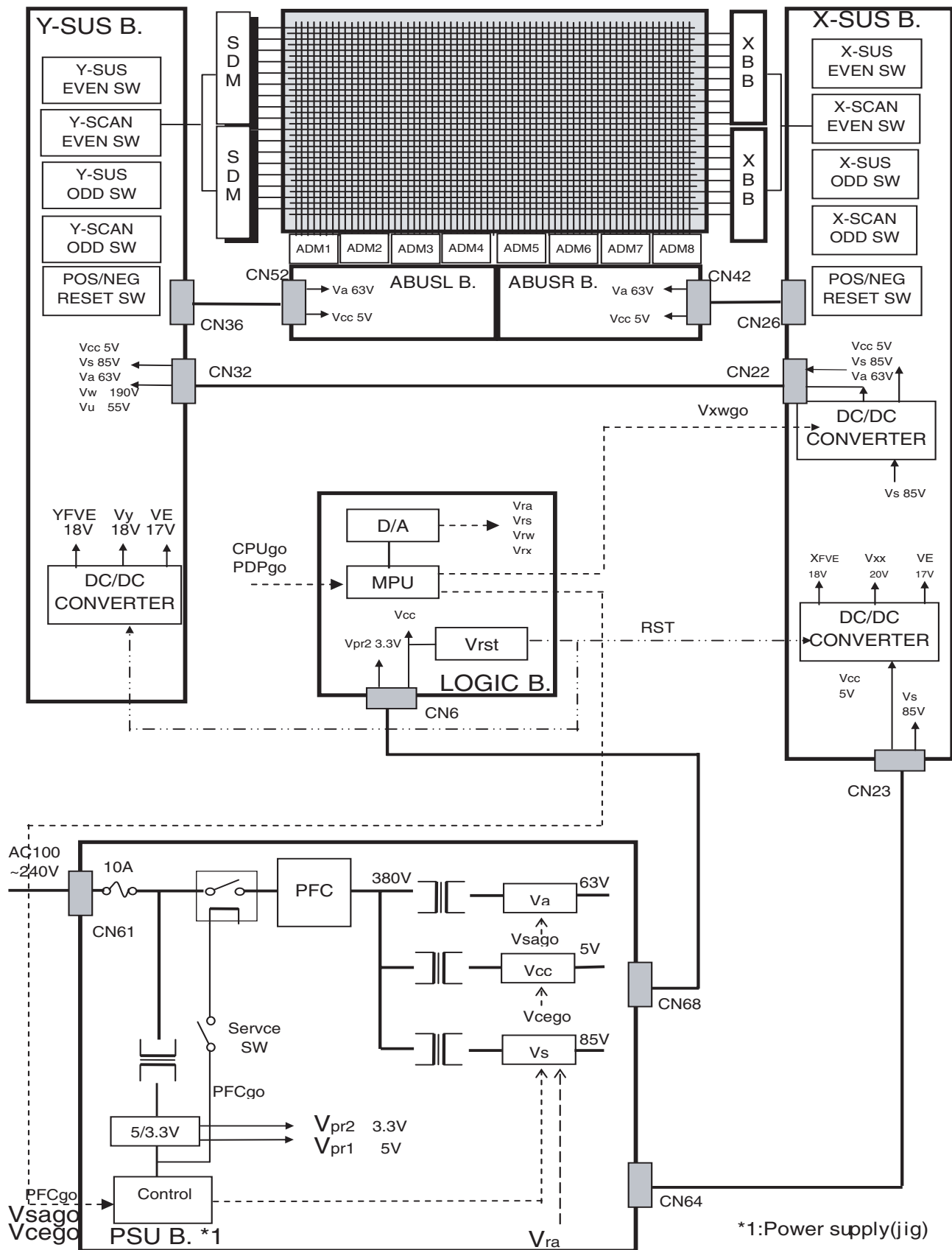


Figure 6-1 Signal block diagram



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300905

Figure 6-2 Power block diagram

6.2 Test Points

Not available.

6.3 Wave Forms

Not available.

7. Circuit Diagrams and PWB Layouts

Not applicable.

8. Alignments

Index of this chapter:

8.1 Voltage Setting Procedure

8.1 Voltage Setting Procedure

On the back of the PDP, in the top right hand corner, you find the Voltage Setting label:

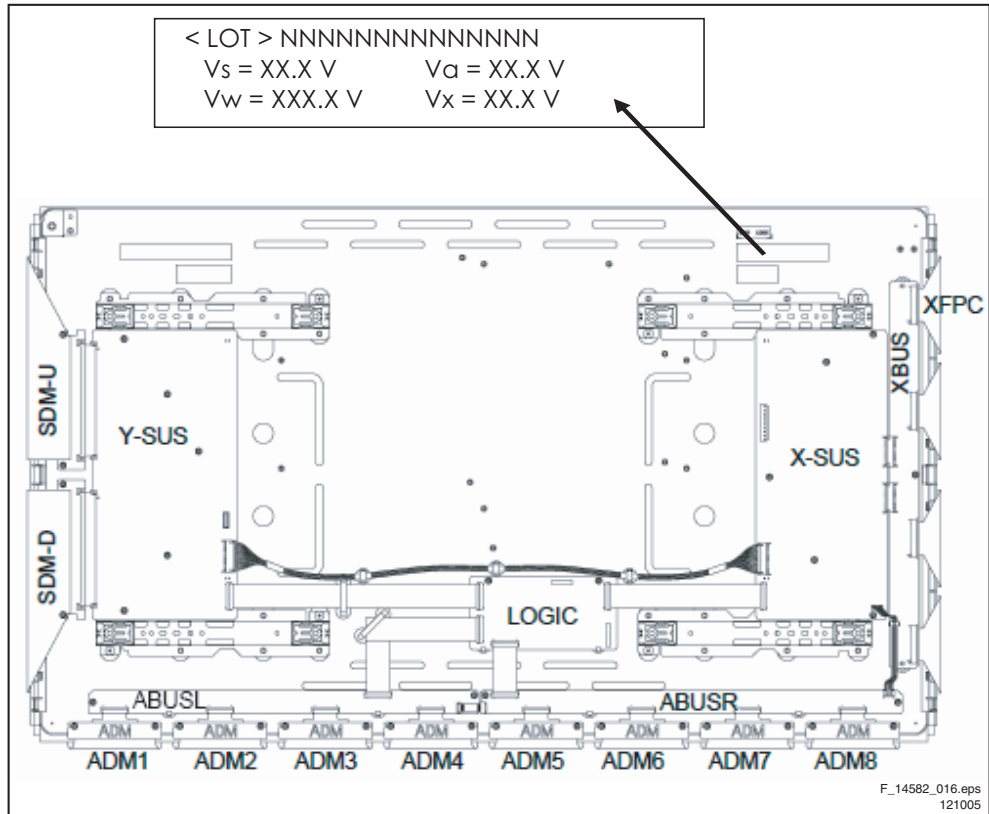


Figure 8-1 Voltage setting label

This Voltage Setting label shows the following messages:

Table 8-1

Item	Adjustment items	Measurement point	Adjustment value (conditions)
1	Vs voltage adjustment	PSU board F241 or CN392 test points	Voltage setting label indication value* $\pm 1\%$ (all black)
2	Va voltage adjustment	PSU board F240 or CN392 test points	Voltage setting label indication value* $\pm 1\%$ (all black)
3	Vw voltage adjustment	X-SUS board connector CN26 6-pin	Voltage setting label indication value* $\pm 1\%$ (all black)
4	Vx voltage adjustment	X-SUS board connector CN26 1-pin	Voltage setting label indication value* $\pm 1\%$ (all black)

If the voltage adjustments Vs and Va on the Power Supply Unit must be performed, depends on the version of the Power Supply Unit (see table 8-2).

Table 8-2

	PSU version 3	PSU v3 with precision R's	PSU version 4
PDP with Vs feedback (-52 PDP)	Feedback loop 'OFF', alignment is necessary	Feedback loop 'ON', alignment (check) is necessary (see voltage setting label)	Feedback loop 'ON', no alignment necessary
PDP with Vs/Va feedback (with 'B' in serial number)	Feedback loop 'OFF', alignment is necessary	Feedback loop 'ON', no alignment (check) necessary	Feedback loop 'ON', no alignment necessary

This table also shows if the Vs and Va control loop must be switched ON or OFF.

The voltage adjustments Vw and Vx are done automatically via ComPair. After exchange of the Logic Board, click on 'Ship out'. The settings from the old Logic Board will be restored in the new Logic Board.

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

- 9.1 Board Function Description
- 9.2 List of Abbreviations

9.1 Board Function Description

9.1.1 Logic Board Function

Data Processor

- (γ adjustment (1 / 2.2 / 2.4 / 2.6 / 2.8).
- NTSC/EBU format (Colour matrix) Switch.
- RGB gain Control (White balance adjustment, amplitude limitation).
- Error diffusion technology (grey scale adjustment).
- Dither (grey scale adjustment).
- Burn-in pattern generation.

Data Converter

- Quasi out-line adjustment (luminous pattern control).

Scan Controller

- Address driver control signal generator (ADM).
- Scan driver control signal generator (SDM).
- X/Y sustain control signal generator.

Waveform ROM

- Waveform pattern for drive / timing memory.

MPU

- Synchronous detection.
- System control.
- Driving voltage (Va, Vs, Vr, Vw) minute adjustment.
- Abnormal watch (breakdown detection) / abnormal processing.
- I_s (sustain) current control (sustain pulse control).
- I_a (address) current control (sub-field control).
- External communication control.
- Flash memory (firmware).

EEPROM

- Control parameter memory.
- The accumulation energizing time (every hour).
- Abnormal status memory (16 careers).

9.1.2 Function of X-SUS Board

DC/DC power supply block

- Vs (+60V), Vw (+185V), Vx (+45V).
- Vcc (+5V), XFvcc (+5V, floating), XFve (+18V, floating), Ve (+17V), Vb(-5V).

X Switching Block

- Switching during address period.
- Switching during sustain period.
- Switching during reset period.

Current Detector Block

- I_{sx} (sustain) current detection.

9.1.3 Function of Y-SUS Board

DC/DC Power Supply Block

- Vcc (+5V) -> Y Fvcc (+5V, floating)/Y Fve (+ 18V, floating)/Ve (+ 17V)

Switching Block

- Switching during address period.
- Switching during sustain period.
- Switching during reset period.

Current Detector Block

- I_{sy} (sustain) current detection.
- I_{sp} (SDM) current detection.

9.1.4 Function of PSU Board

Stand-by Power Supply Block

- AC100-240: +5V & +3V3 Stand-by.

PFC Block (AD/DC Power Supply Block)

- AC100-240: +390V.

AD/DC Power Supply Block

- +380V, Vcc (+5V), Vs (+80V), Va (+60V).

Current Detection Block

- I_a (address) current detection.

Abnormal Voltage Monitoring

- Vs excess voltage monitoring.
- Va excess voltage monitoring.

9.2 List of Abbreviations

ADM	Address module
Burn-in rack	Test equipment of the shelf test in which the PDP unit is left to stand in drive condition
CPU	The unit for controlling the circuit operation
DOXE	The control voltage for even-numbered lines in the X direction
DOXO	The control voltage for odd-numbered lines in the X direction
DOYSD	Used in the drive voltage in the Y direction (down)
DOYSU	Used in the drive voltage in the Y direction (up)
External power ON	Running the external powers (Vcc, Va, Vs) on the designated voltage. Unless otherwise specified
External power OFF	Making the external powers (Vcc, Va, Vs) to stop their operation completely. Unless otherwise specified
Flexible cable	The cable to connect the electric circuit to the panel
Flicker	Continuous switching between bright and dark views by the PDP itself
Gradation	Shading of the display colour
OPUMP	The name of a circuit where the current from X/YSUS is returned
Oscilloscope	A device that allows the flow and strength of the running current to be visually checked and measured
Panel	The indication part of the plasma display panel (PDP)
Panel voltage	The voltage required operating the PDP normally
Parts	Each PC board and parts mounted in the PC boards

PDP	Plasma display panel abbreviated
Probe	A cable with contact finger that can transfer the status of the electric circuit to be measured to an oscilloscope
Protection cover	A cover made of aluminium to protect the PDP entirely during test
ROM	Memory that stores the drive sequence and other data
SDM	Scan module
SUS	XSUS or YSUS
Tapping	Light impact
Unit of COM	The unit of circuits connected to the panel with flexible cable (YCOM UP/DOWN, XBUS UP/DOWN, address sections, the unit of PC boards in ACOM 1 to 5).
Va	The power supply at 60 V, which is used to write data on the panel
Vcc	The power supply at 5 V, which is used to operate the logic section mainly
Vs	The power supply ranging from 127 V to 180 V, which is used to maintain display data. In addition, this can serve as the primary side for the secondary voltage (Vw, -Vy, Vsc)
White solid	A condition when the screen display is entirely white
XSUS	The name of the circuit that controls the panel operation in the X direction
YCOM	The circuit used to output a panel Y line selection signal and the voltage of a display data keep signal
YCOMDV	The name of the panel drives voltage signal output from YCOM UP/DOWN section
YSUS	The name of the circuit that controls the panel operation in the Y direction

10. Spare Parts List

For spare parts list see chapter 5

11. Revision List

Supplement on the following service manuals:

Table 11-1 Overview of chassis and manuals, covered by this manual

Display type	Model #	Chassis	Manual #
32" H1	32FD9944/01S	FM23 AA	312278513891
	32FD9944/69S	FM23 AA	312278513891
	32FD9954/17S	FM23 AA	312278513891
	32FD9954/69S	FM23 AA	312278513891
	32HF9964/12Z	FM23 AA	312278513891
	32HF9964/22Z	FM23 AA	312278513891
	32PF9964/12S	FM23 AA	312278513891
	32PF9965/12S	F22RE AA	312278513171
32" H2	32FD9944/01S	FM23 AA	312278513891
	32FD9944/69S	FM23 AA	312278513891
	32FD9954/17S	FM23 AA	312278513891
	32FD9954/69S	FM23 AA	312278513891
37" H2	420P10/00	FTV1.9DE AA	312278510170
	42FD9932/01G	FTV1.9DE AA	312278510170
	42FD9932/01S	FTV1.9DE AA	312278510170
	42FD9932/17G	FTV1.9DE AA	312278510170
	42FD9932/69G	FTV1.9DE AA	312278510170
	42FD9932/69S	FTV1.9DE AA	312278510170
	42PF9952/12S	FTV1.9DE AA	312278510170
	42PF9952/19S	FTV1.9DE AA	312278510170
	42PF9952/32S	FTV1.9DE AA	312278510170
	42PF9952/39S	FTV1.9DE AA	312278510170
	42PF9952/58S	FTV1.9DE AA	312278510170
37" A1	Information not available		
42" H1	420P30/00	FM23 AA	312278513891

Display type	Model #	Chassis	Manual #
	42FD9934/17S	FM24 AA	312278513891
	42FD9934/69S	FM24 AA	312278513891
	42FD9944/01S	FM24 AA	312278513891
	42FD9944/69S	FM24 AA	312278513891
	42FD9954/17S	FM24 AA	312278513891
	42FD9954/69S	FM24 AA	312278513891
42" H2	42FD9934/17S	FM24 AA	312278513891
	42FD9934/69C	FM24 AA	312278513891
	42FD9934/69S	FM24 AA	312278513891
	42FD9944/01S	FM24 AA	312278513891
	42FD9944/69S	FM24 AA	312278513891
	42FD9944/93S	FM24 AA	312278513891
	42FD9954/17S	FM24 AA	312278513891
	42FD9954/69C	FM24 AA	312278513891
	42FD9954/69S	FM24 AA	312278513891
	42FD9954/93S	FM24 AA	312278513891
	BDH4211/00	FM24 AB	312278513891
	BDH4221/00	FM24 AB	312278513891
42" A1	42PF9956/37	FTP2.2U AA	312278514662
	42PF9966/12	FTP2.2E AA	312278514651
42" A2	42PF9966/10	FTP2.2E AA	312278514651
	42PF9966/12	FTP2.2E AA	312278514651
42" A3	42PF5620/10	LC4.9E AA	312278515431
	42PF7520D/79	LC4.3A AB	312278515360
	42PF9967D/10	FTP2.4E AB	312278515740

11.1 Service Manual 3122 785 1458.1

The code numbers of X-SUS and Y-SUS boards in table of chapter 5.3 are corrected.

11.2 Service Manual 3122 785 1458.2

New display types added (A1, A2, and A3).

Service Service Service

FHP PDP Repair Manual

FPF42C128135UA-52 (42" A4)

Service Manual

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Subject to modification

EN 3122 785 16400



PHILIPS

1. Technical Specifications

Index of this chapter:

- 1.1 Specifications
- 1.2 Serial Numbers
- 1.3 Chassis overview

1.1 Specifications

1.1.1 42" A4

No	Item	Spec. FPF42C128135UA-52
1	Resolution	1024 (H) x 1080 (V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	3072 (H) x 1080 (V)
3	Pixel Pitch	0.90 mm (H) x 0.485 mm (V)
4	Cell Pitch	0.30 mm (H) x 0.485 mm (V)
5	Display size	921.60 (H) x 523.8 mm (V)
6	Screen size	Diagonal 42"
7	Screen aspect	16:9
8	Dimensions	994 (W) x 587 (H) x 66 (D) mm
9	Weight	About 16 kg
10	H sync, V sync, data	50 kHz (H), 50/60/70 Hz (V), LVDS

1.2 Serial Numbers

Check the serial ID number of the product requested for repair, before starting the problem analysis and repair.

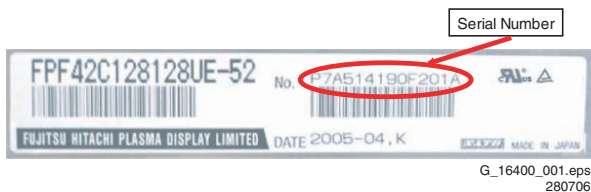


Figure 1-1 PDP Serial number

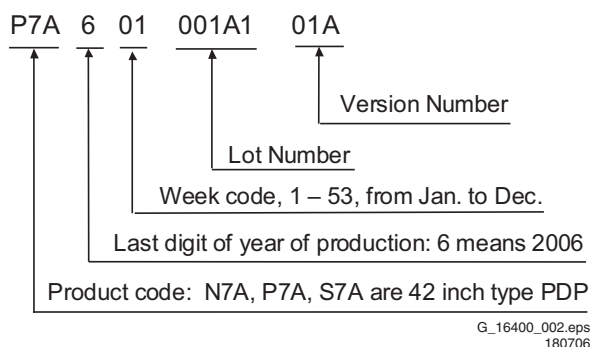


Figure 1-2 PDP Serial number explanation

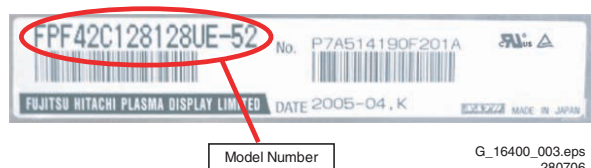


Figure 1-3 PDP Model number

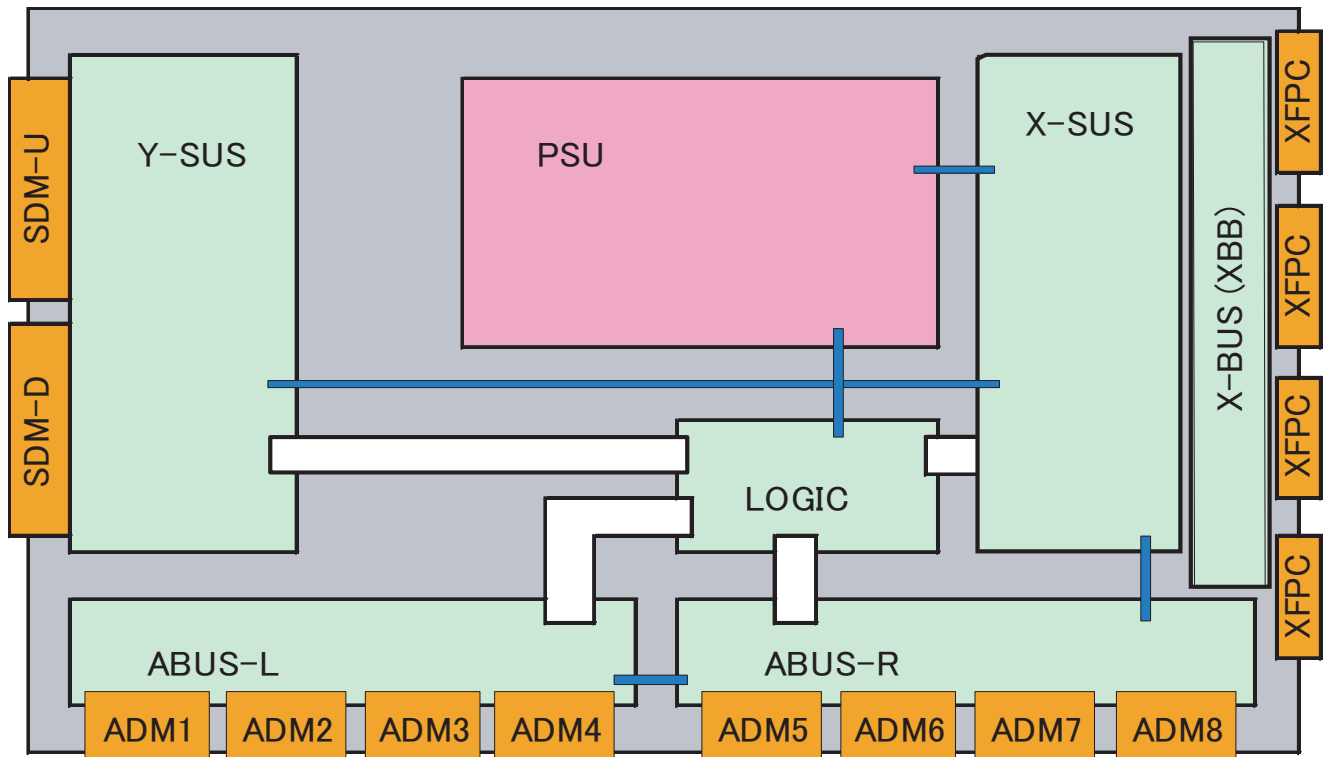
FPF42C128128UC -52	42A1 (covered)
FPF42C128128UD -52	42A2 (by manual)
FPF42C128128UE -52	42A3 (3122 785 14580)
FPF42C128135UA -52	42A4 (in this manual)

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Figure 1-4 List of model numbers

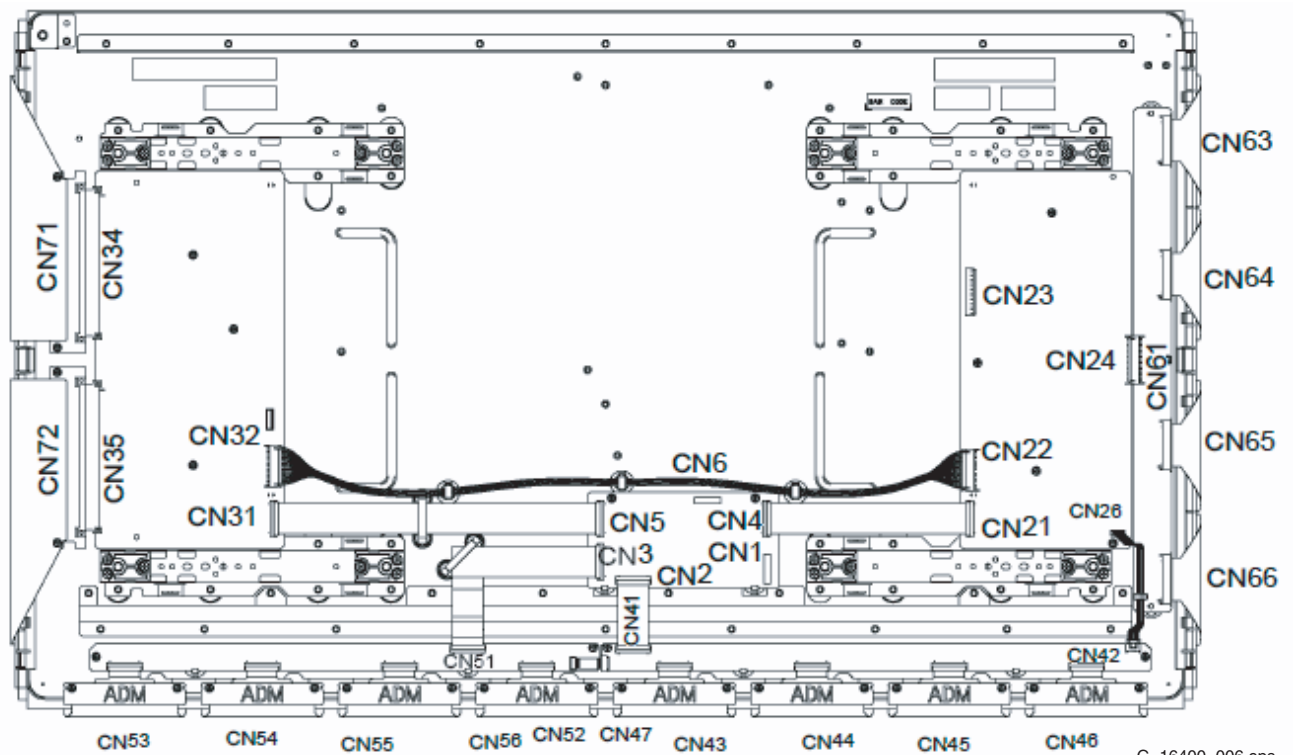
Note: The PDP serial number and the serial number of the completed chassis (product requested for repair) are usually the same when the product is brought in for repair the first time.

1.3 Chassis overview



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Figure 1-5 PWB locations



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Figure 1-6 Connector positions

1.4 Some connector layouts

Pin No.	Signal name	Pin No.	Signal name
1	RA-	2	GND (LVDS)
3	RA+	4	SCL
5	RB-	6	GND
7	RB+	8	SDA
9	RC-	10	GND (LVDS)
11	RC+	12	CPUGO
13	RXCLKIN-	14	PDPGO
15	RXCLKIN+	16	IRQ
17	RD-	18	PDWN
19	RD+	20	GND (LVDS)
21	RE-	22	GND
23	RE+	24	GND
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND

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Figure 1-7 LVDS connector CN1 Logic Board

Pin No.	Symbol
1	Vcc
2	GND
3	Vpr2
4	GND
5	Vra
6	Vrs
7	VCEGO
8	VSAGO
9	PFCGO

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Figure 1-8 Power supply connector CN6 Logic Board

Pin No.	Symbol
1	Va
2	N.C.
3	Vcc
4	GND
5	GND
6	GND
7	N.C.
8	Vs
9	Vs
10	Vs


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270706

Figure 1-9 Power supply connector CN23 X-SUS Board

2. Safety Instructions, Warnings, and Notes

2.1 Safety Instructions

It is not allowed to operate the FTV-set without glass plate. One function of this glass plate is to absorb Infrared Radiation. Without this glass plate the level of Infrared Radiation produced by the plasma display could damage your eyes.

1. Safety regulations require that during a repair:
 - the set should be connected to the mains via an isolating transformer (in this particular case a transformer of ≥ 800 VA).
 - safety components, indicated by the symbol , should be replaced by components identical to the original ones.
2. Safety regulations require that after a repair the set must be returned in its original condition. In particular attention should be paid to the following points.
 - Note: The wire trees should be routed correctly and fixed with the mounted cable clamps.
 - The insulation of the mains lead should be checked for external damage.
 - The electrical DC resistance between the mains plug and the secondary side should be checked (only for sets that have a mains isolated power supply). This check can be done as follows:
 - unplug the mains cord and connect a wire between the two pins of the mains plug;
 - set the mains switch to the on position (keep the mains cord unplugged!);
 - measure the resistance value between the pins of the mains plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between 4.5 M Ω and 12 M Ω ;
 - switch off the TV and remove the wire between the two pins of the mains plug.
 - The cabinet should be checked for defects to avoid touching of any inner parts by the customer.

LED is positioned at the right side of IR-receiver eye of the E-box. Take into account that receiver-LED on DST is positioned not in the middle but at the left side. Point corresponding LEDs to each other. In case the amount of Infrared produced by the screen pollutes the communication, the set can be set in Stand-by-mode. Then still the error-messages can be retrieved.


2.3.1 Notes on Safe Handling of the Plasma Display

Notes to Follow During Service

- The work procedures shown with the Note indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times other than when adjusting and checking the product, be sure to turn OFF the main POWER switch and disconnect the power cable from the power supply of the display during servicing.
- To prevent electric shock and breakage of PC board, start the servicing work at least 30 seconds after the main power has been turned off. Especially when installing and removing the power supply PC board and the SUS PC board in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned off.
- While the main power is on, do not touch any parts or circuits other than the ones specified. The high voltage power supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit PC board, be sure to remove static electricity from your body before handling the circuit PC board.
- Be sure to handle the circuit PC board by holding the large parts as the heat sink or transformer. Failure to observe this precaution may result in the occurrence of an abnormality in the soldered areas.
- Do not touch the circuit PC boards. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original setup

2.2 Warnings

ESD

All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD ). Careless handling during repair can reduce life drastically. When repairing, make sure that you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential.

1. Available ESD protection equipment:
 - complete kit ESD3 (combining all 6 prior products - small table mat) 4822 310 10671
 - wristband tester 4822 344 13999
2. Never replace modules or other components while the unit is switched on.
3. When making settings, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

2.3 Notes

1. A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel it is recommended to do some maintenance by a qualified service employee only.
2. Never disconnect the power display cable when the set is operating
3. With DST no failures (error-codes) can be read, when the set is in Service-mode.
4. If DST reacts with "error 2", there is no communication between the TV and the DST. Note that the IR-transmitter

3. Directions for Use

Not applicable.

4. Mechanical Instructions

Notes:

- Figures below can deviate from the actual situation, due to different set executions.
- For more detailed instructions regarding the (dis)assembly of the TV chassis that hold these PDPs, read the corresponding TV Service Manual.

4.1 Board Swap Instructions

4.1.1 General

Before dismounting panels read notes below!

Caution when removing circuit board!

When removing the circuit board after the main power is turned on/off, wait for at least one minute before starting to remove the circuit board.

If the circuit board removal is started immediately after turning off the main power, it can result in electric shock or damage to the circuit due to residual electric charge.

Caution on handling the FPC connector!

To release the black lock lever of the connector, flip it up gently in the middle with the nail of the thumb or forefinger, from the side with the cable.

Never pinch the lock lever with fingers or tools. Doing so might damage the lock lever.

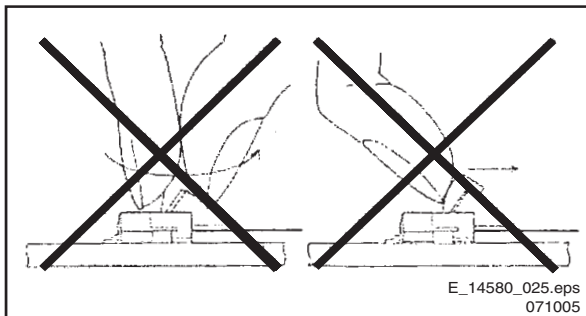


Figure 4-1 Handling the FPC connector

4.1.2 X-SUS and X-BUS Circuit Boards

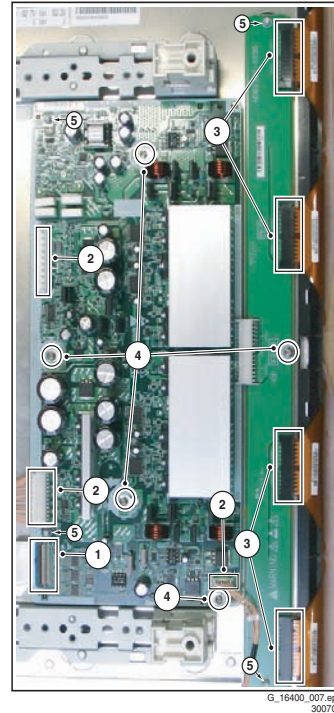


Figure 4-2 X-BUS and X-SUS board removal (1/2)

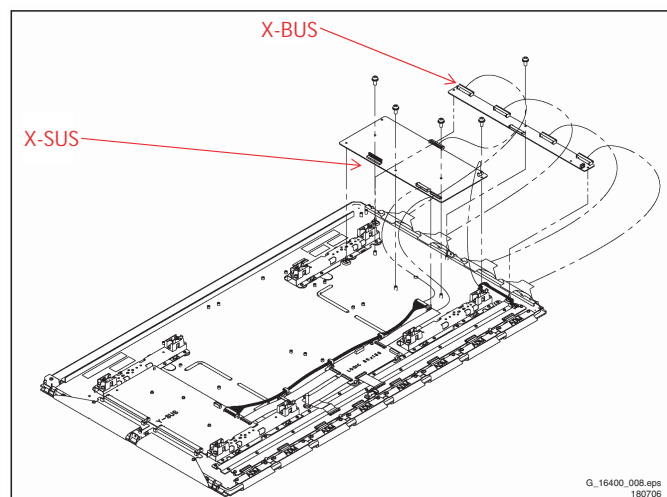


Figure 4-3 X-BUS and X-SUS board removal (2/2)

Remove the circuit boards by following the steps below. To install the circuit boards, reverse the removal procedure.

- Release the lock of the FPC connector [1] and unplug the signal cable.
- Unplug the connectors [2].
- Unplug the 4 XFPC's [3] on the X-BUS board.
- Remove the fixing screws [4].

- Release the white stand-offs [5] from the X-SUS board,

6. Remove the X-BUS board and the X-SUS board together.

Make sure that you do not touch the heat sink when removing the Y-SUS board.

4.1.3 Y-SUS Circuit Board

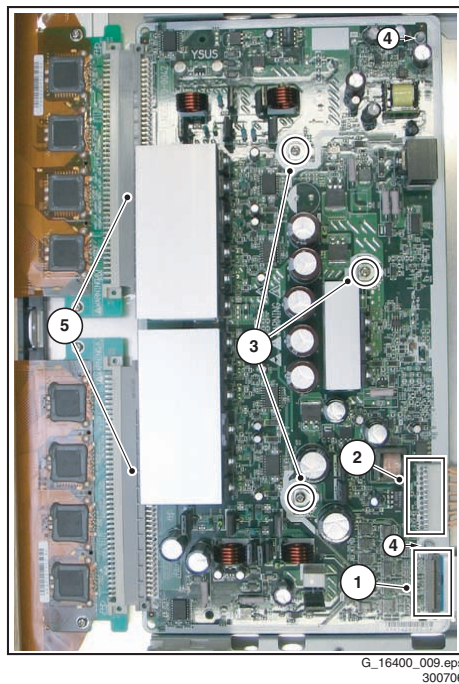


Figure 4-4 Y-SUS board removal (1/2)

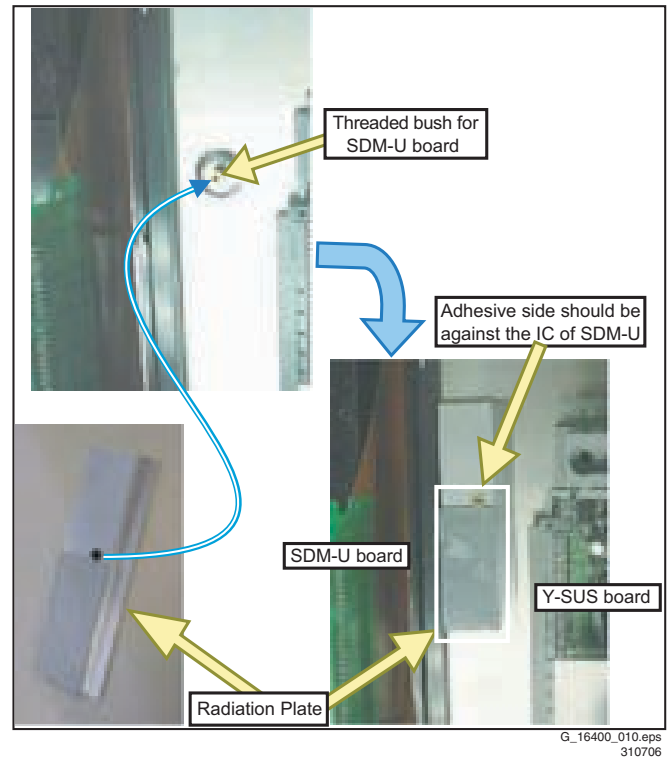


Figure 4-6 Radiation plate position

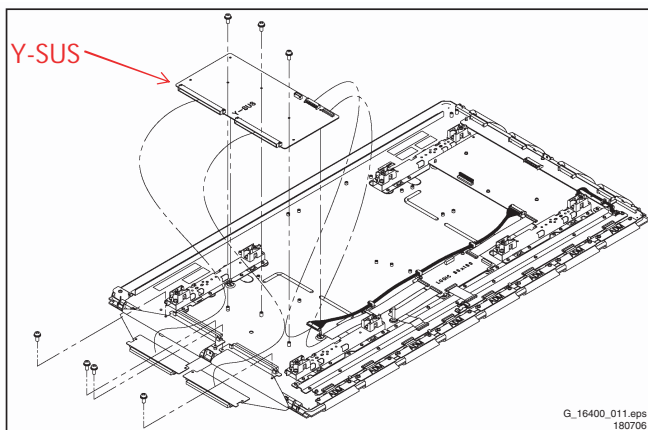


Figure 4-5 Y-SUS board removal (2/2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Release the lock of the FPC connector [1] and unplug the signal cable.
2. Unplug the connector [2].
3. Remove the fixing screws [3].
4. Release the white stand-offs [4] from the Y-SUS board.
5. Pull out the Y-SUS board horizontally, in this way unplugging the connectors [5].
6. Remove the Y-SUS board.

Make sure that you do not touch the heat sink when removing the Y-SUS board.

Note: Make sure the radiation plate is positioned correctly. It is located underneath the upper SDM, and the threaded bush should sit in the hole of the radiation plate.

4.1.4 ABUS-L Circuit Board

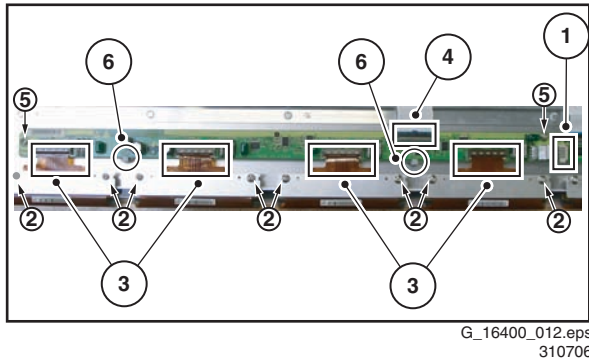


Figure 4-7 ABUS-L board removal (1/2)

4.1.5 ABUS-R Circuit Board

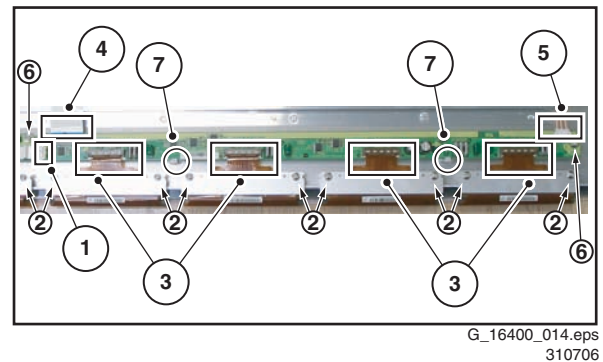


Figure 4-9 ABUS-R board removal (1/2)

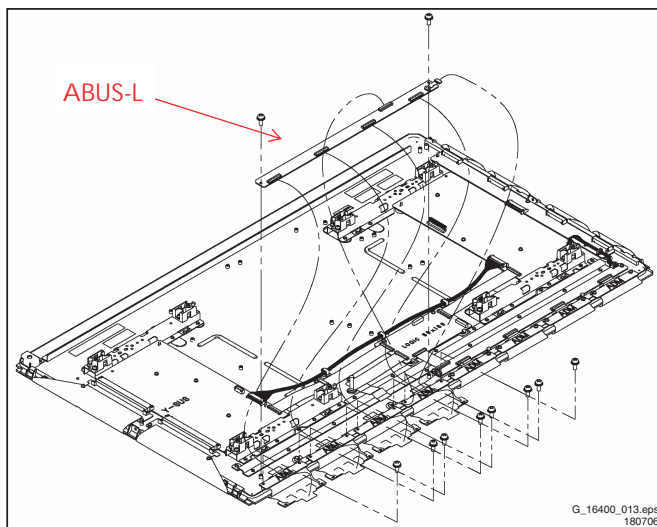


Figure 4-8 ABUS-L board removal (2/2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Unplug the connector [1].
2. Remove the screws [2] fixing the ADMs.
3. Release the lock of the FPC connectors [3], and remove the ADM flexible board.
4. Release the lock of the FPC connector [4] and unplug the signal cable.
5. Remove the screws [5] fixing the ABUS-L board.
6. Remove the ABUS-L board.
7. When installing the ABUS-L board, put the board in such a position that it is locked by the tabs [6] before fixing it with the screws.

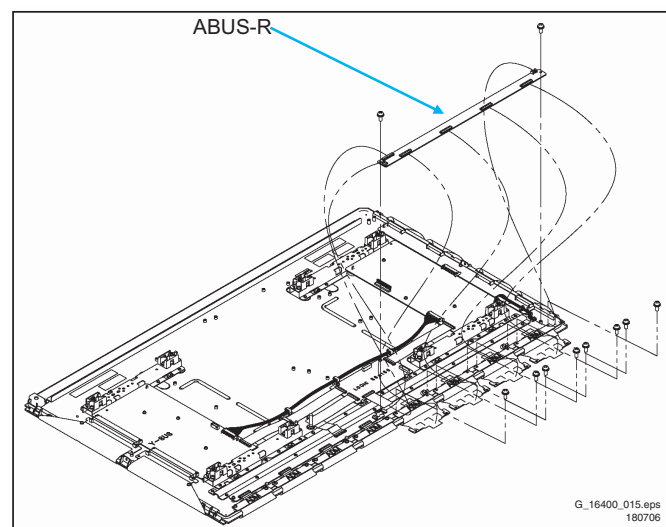


Figure 4-10 ABUS-R board removal (2/2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Unplug the connector [1].
2. Remove the screws [2] fixing the ADMs.
3. Release the lock of the FPC connectors [3], and remove the ADM flexible board.
4. Release the lock of the FPC connector [4] and unplug the signal cable.
5. Unplug the connector [5].
6. Remove the screws [6] fixing the ABUS-R board.
7. Remove the ABUS-R board.
8. When installing the ABUS-R board, put the board in such a position that it is locked by the tabs [7] before fixing it with the screws.

4.1.6 LOGIC Board

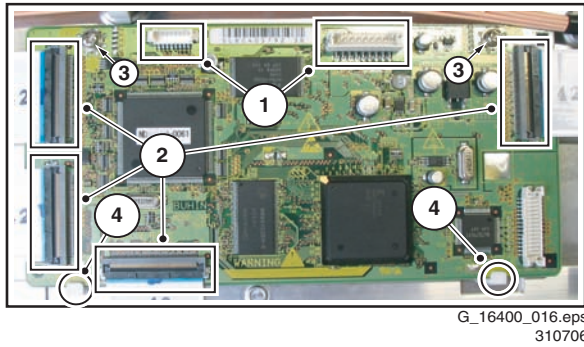


Figure 4-11 LOGIC board removal (1/2)

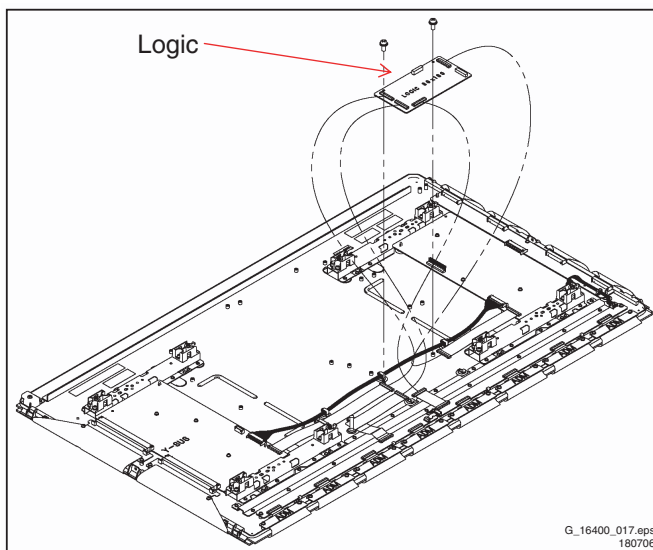


Figure 4-12 LOGIC board removal (2/2)

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Unplug connectors [1].
2. Release the lock of the FPC connectors [2] and unplug the signal cables.
3. Remove the screws [3] fixing the LOGIC board.
4. Remove the LOGIC board.
5. When installing the LOGIC board, put the board in such a position that it is locked by the tabs [4] before fixing it with the screws.

4.1.7 PSU Board



Figure 4-13 PSU board removal

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

1. Unplug connectors [1].
2. Remove screws [2].
3. Remove the PSU.

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

- 5.1 Repair Tools
- 5.3 Process Flow
- 5.4 Repair Instructions
- 5.5 Defect Description Form

5.1 Repair Tools

To be able to repair the Plasma Display Panels on board level, the following repair tools are available:

- Special LVDS cable: T.B.D.
- Foam buffers: 3122 785 90581.

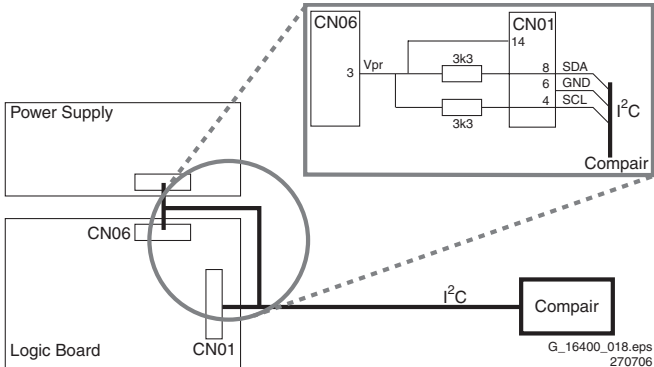


Figure 5-1 Extension cable kit ALiS PDP



Figure 5-2 Foam buffers for FTV

5.2 Error codes

When an error causes the PDP to switch “OFF”, an error code is put into an EEPROM on the Logic Board. You can read out the contents of the error code memory with the ComPair tool.

5.2.1 How to Connect the ComPair Tool

- Carefully disconnect the LVDS cable from CN01 on the Logic Board.
- If necessary connect a PSU with a voltage of 3.3V to drive the LOGIC board.
- Connect the cable from the ComPair tool to connector CN01 of the LOGIC board.
- Turn on the ComPair tool.
- Launch the ComPair software.
- Read out the error buffer.

5.2.2 Error Code Overview

Table 5-1 Error code table

Error code	Detected by board	Error description	Suspected board(s)			
21	X-SUS	Vxx power voltage is too high	X-SUS	LOGIC		
24		Vxx power voltage is too low	X-SUS	LOGIC		
25		Vex power voltage is too high	X-SUS			
26		Vex power startup is faulty	X-SUS	LOGIC		
44	Y-SUS	Vey power voltage is too low	Y-SUS	LOGIC		
45		Vey power voltage is too high	Y-SUS			
46		Vey power startup is faulty	Y-SUS	LOGIC		
4C		Temperature too high	Y-SUS	LOGIC		
61	X-SUS	Vs power voltage is too high	Y-SUS	X-SUS	LOGIC	PSU
62	Y-SUS	Vs power startup is faulty	X-SUS	Y-SUS	PSU	LOGIC
64		Ve power voltage is too low	LOGIC	X-SUS	Y-SUS	
65		Ve power voltage is too high	Y-SUS	Y-SUS		
66		Ve power startup is faulty	LOGIC	X-SUS	Y-SUS	
68		Vw power voltage is too low	Y-SUS	LOGIC		
69		Vw power voltage is too high	LOGIC	Y-SUS		
6A		Vw power startup is faulty	Y-SUS	LOGIC		
79		Vw power current is too high (during operation)	Y-SUS	X-SUS	LOGIC	
7B		Vs power voltage is too high (during startup)	Y-SUS	X-SUS	LOGIC	

5.3 Process Flow

The selected workshop receives the defect TV set and investigates the PDP. Two possible solutions follow:

5.3.1 Advanced PDP Exchange (Actual Way-of-Working)

In case of:

- Glass broken,
- Flex foil damaged,
- Y-COM IC on flex foil is damaged, or
- NVM on logic board defect: no communication with ComPair

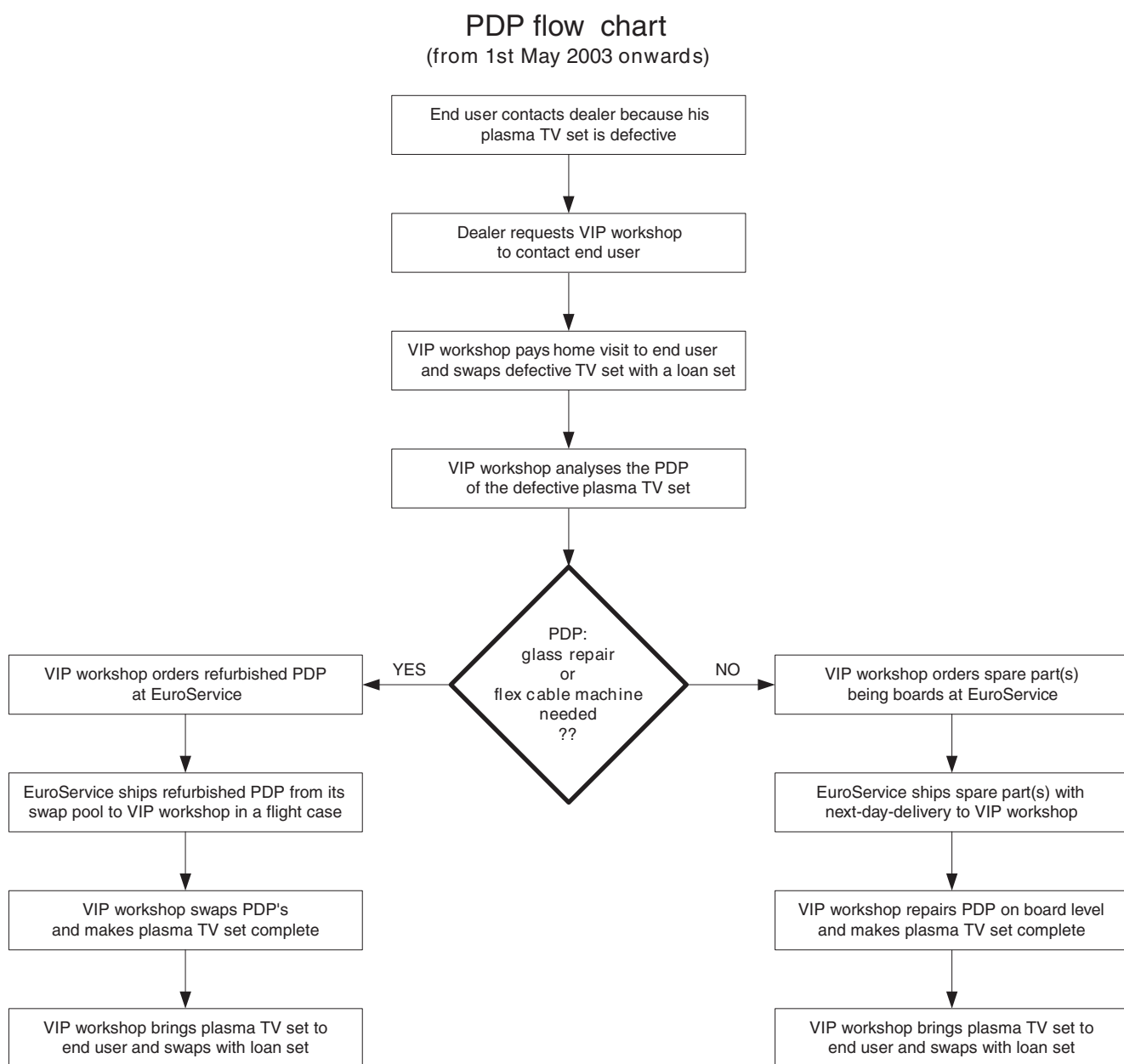
the procedure for repair is as follows:

A new PDP will be ordered at EuroService. They issue an RMA number and ship a refurbished PDP from its swap pool in a flight case to the workshop. After receipt, the workshop sends

the defective PDP, accompanied by a completely filled in Defect Description Form (see figure "Defect Description Form (DDF)"), in this flight case to EuroService. EuroService makes sure the defect PDP is repaired and afterwards added to its swap pool. The workshop makes the TV set complete by building in the refurbished PDP. Afterwards the TV set is returned to the customer.

5.3.2 Customized Repair

If the defect is not mentioned in 5.2.1, the workshop orders the necessary spare parts, being boards, at EuroService. After receipt the workshop swaps the concerning board and makes the TV set complete by building in the PDP. Afterwards the TV set is returned to the customer.



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Figure 5-3 PDP flow chart

5.4 Repair Instructions

5.4.1 General

In case of:

- a broken glass panel,
- a defective flex foil, or
- a defective Y-COM IC on the flex foil

the PDPs need to be send back via the central repair procedure of EuroService.

In other cases the Plasma Display Panels must be repaired on board level.

5.4.2 42" A4 ALiS Plasma Display Panel

The involved Plasma Display Panel is:

Display type	Service code number
FPF42C128135UA-52	9322 235 43682

The available modules for these Plasma Display Panels are:

Module description	FHP code number	Service code number
X-SUS board	FPF33R-XSS0041	9965 000 35647
Y-SUS board	FPF33R-YSS0042	9965 000 35648
Logic board	FPF33R-LGC0061	9965 000 35646
A-BUS Left	FPF33R-ABL0038	9965 000 35649
A-BUS Right	FPF33R-ABR0039	9965 000 35650
X-BUS board	FPF33R-XBU0035	9965 000 35651
Signal Cable LOGIC-X-SUS	FPF29R-CBL001411	9965 000 32669
Signal Cable LOGIC-Y-SUS	FPF29R-CBL001412	9965 000 32670
Signal Cable LOGIC-ABUS-L	FPF29R-CBL001401	9965 000 32668
Signal Cable LOGIC-ABUS-R	FPF29R-CBL001421	9965 000 32671
Power Cable X-SUS-Y-SUS	FPF29R-CBL003601	9965 000 32672
Power Cable X-SUS-ABUS-R	FPF29R-CBL003701	9965 000 32673

Remark:

1. If the LOGIC board is defective, the procedure mentioned in figures "Logic Board Exchange (1 and 2)" must be used.

5.4.3 Fault Finding Flowcharts

Problem analysis procedure: PDP repair / board swap

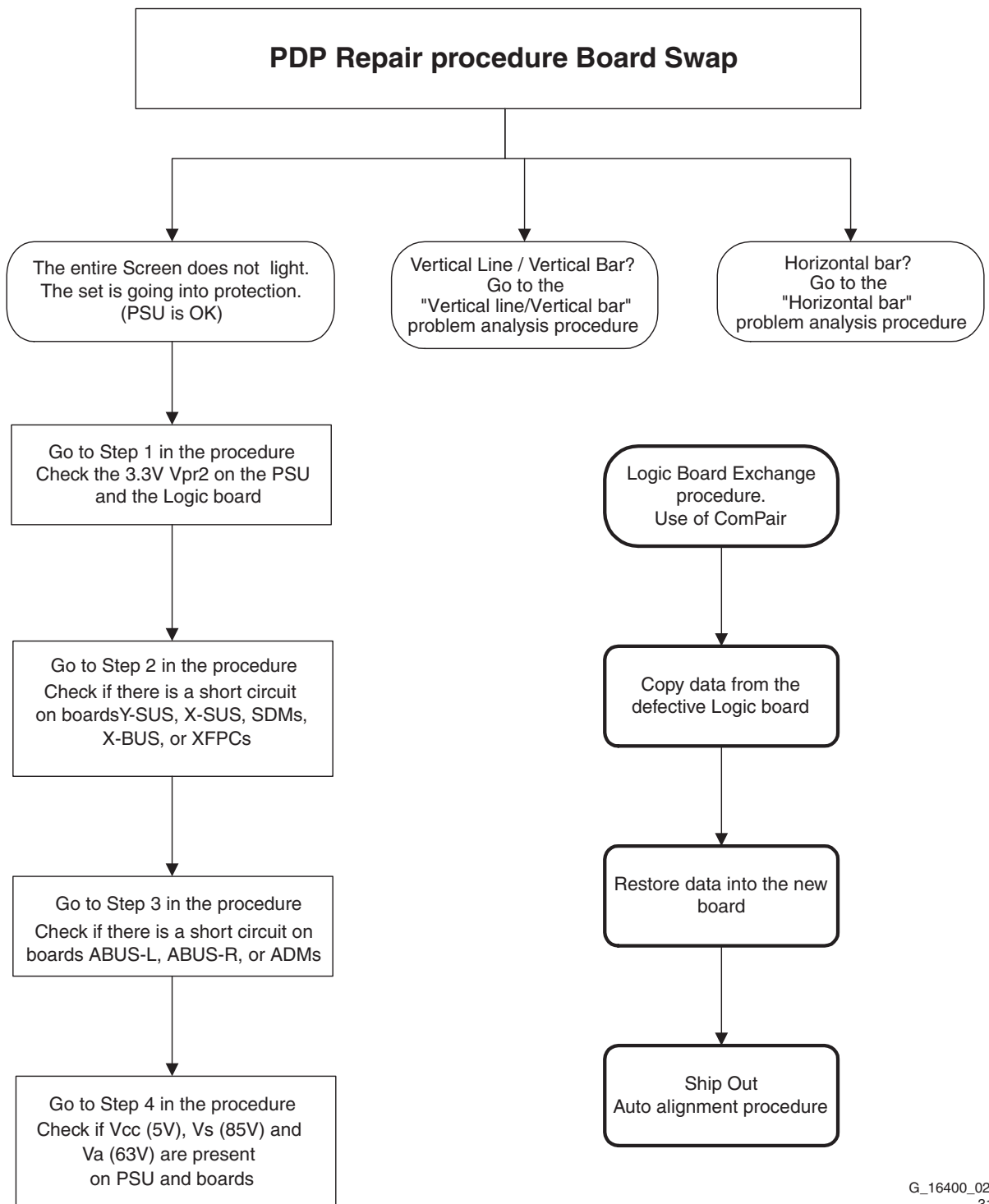
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Figure 5-4 Problem analysis procedure: PDP repair / board swap

Problem Analysis Procedure: The entire screen does not light

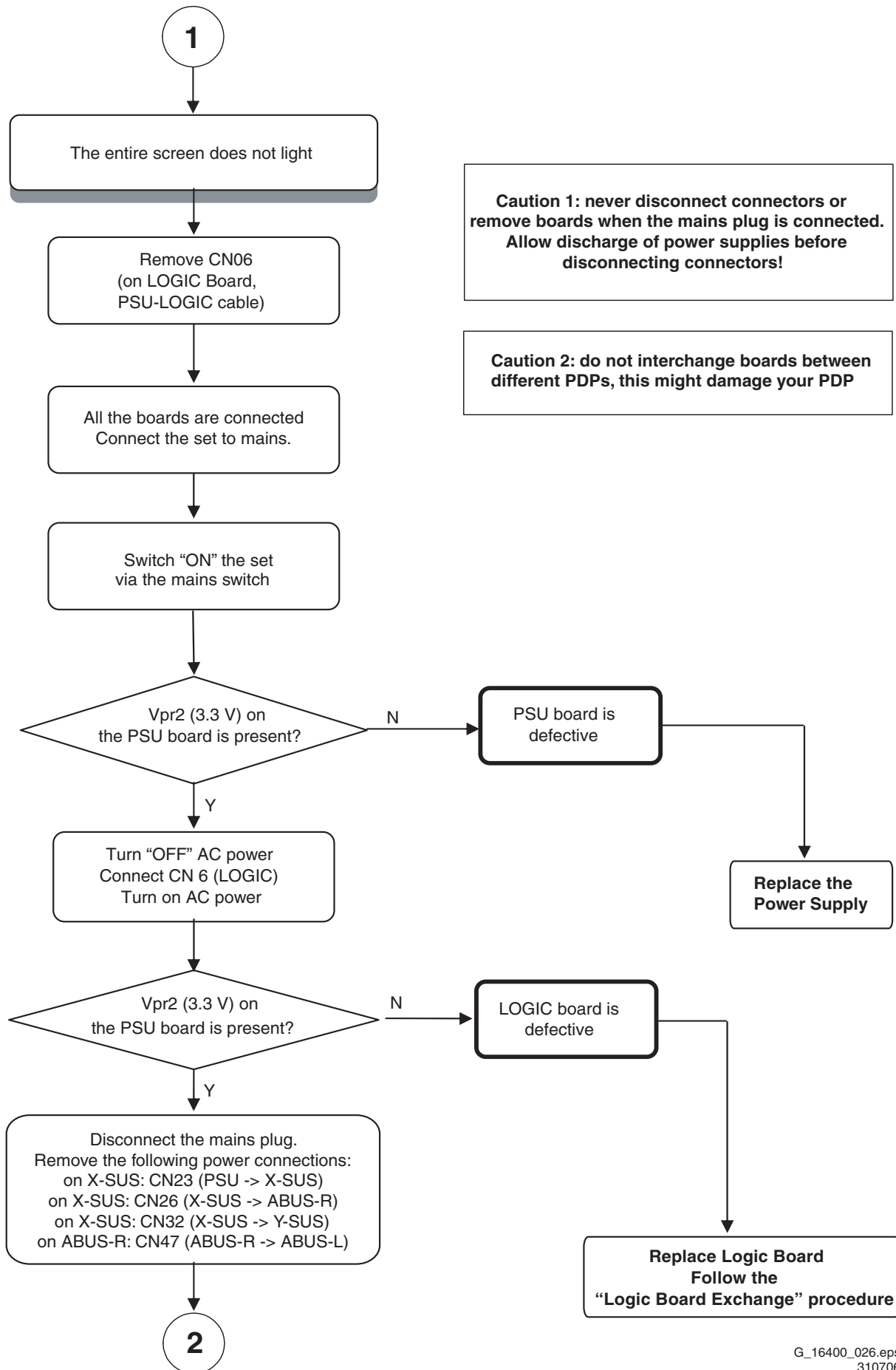


Figure 5-5 Problem analysis procedure: the entire screen does not light

Short-circuit check on Boards and Power Supply Lines

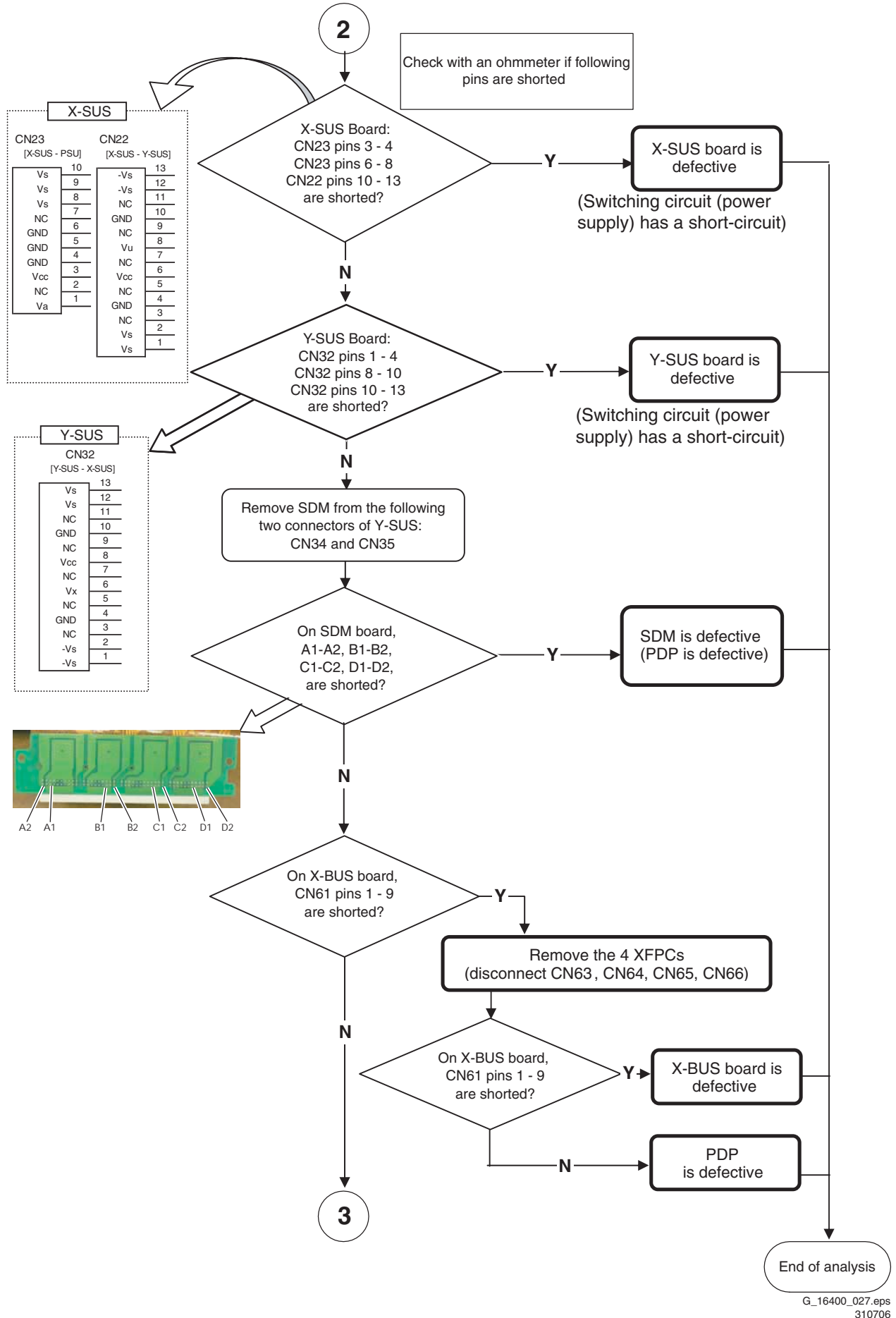


Figure 5-6 Short circuit check on boards and power supply lines (1/3)

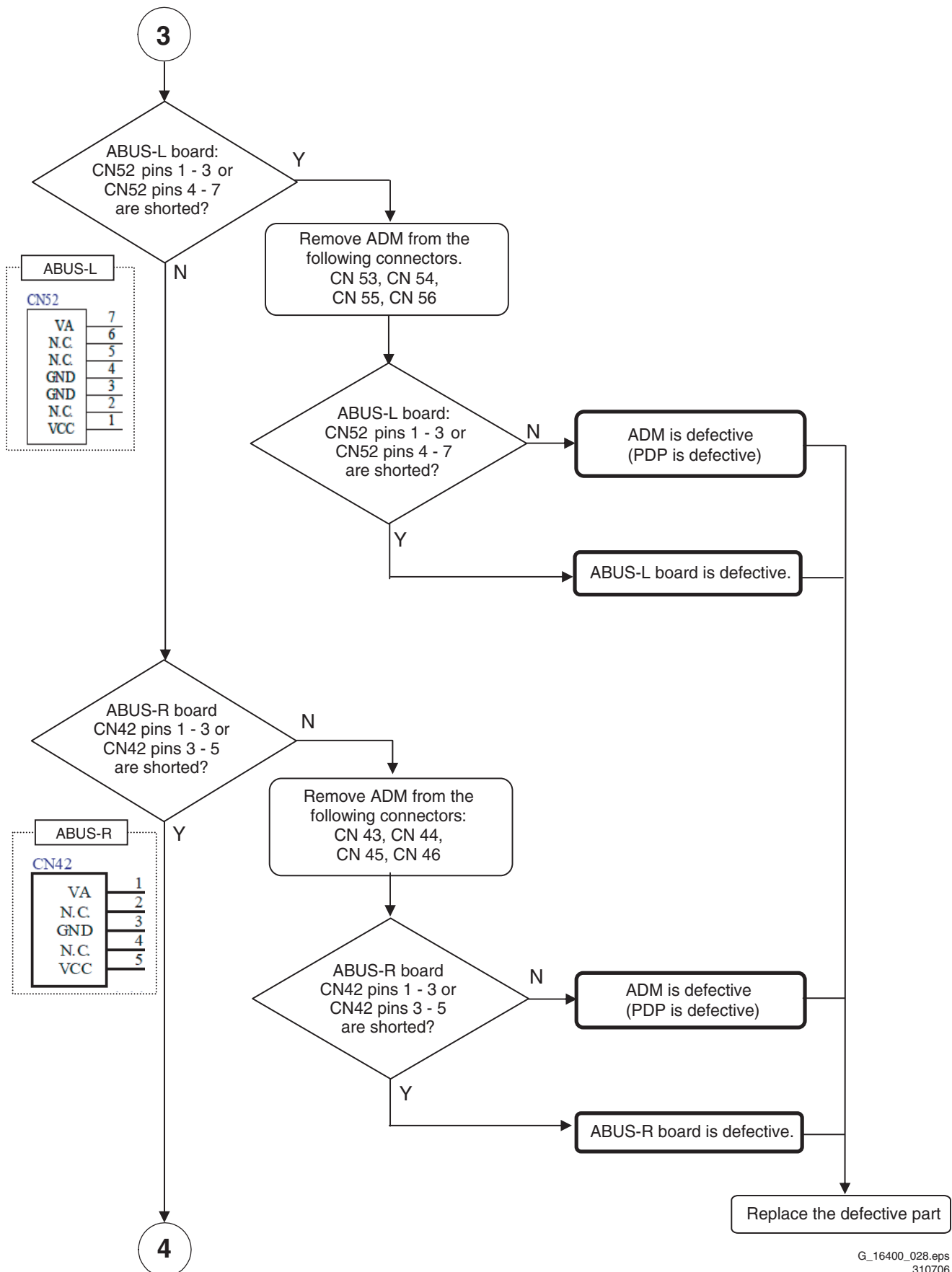


Figure 5-7 Short circuit check on boards and power supply lines (2/3)

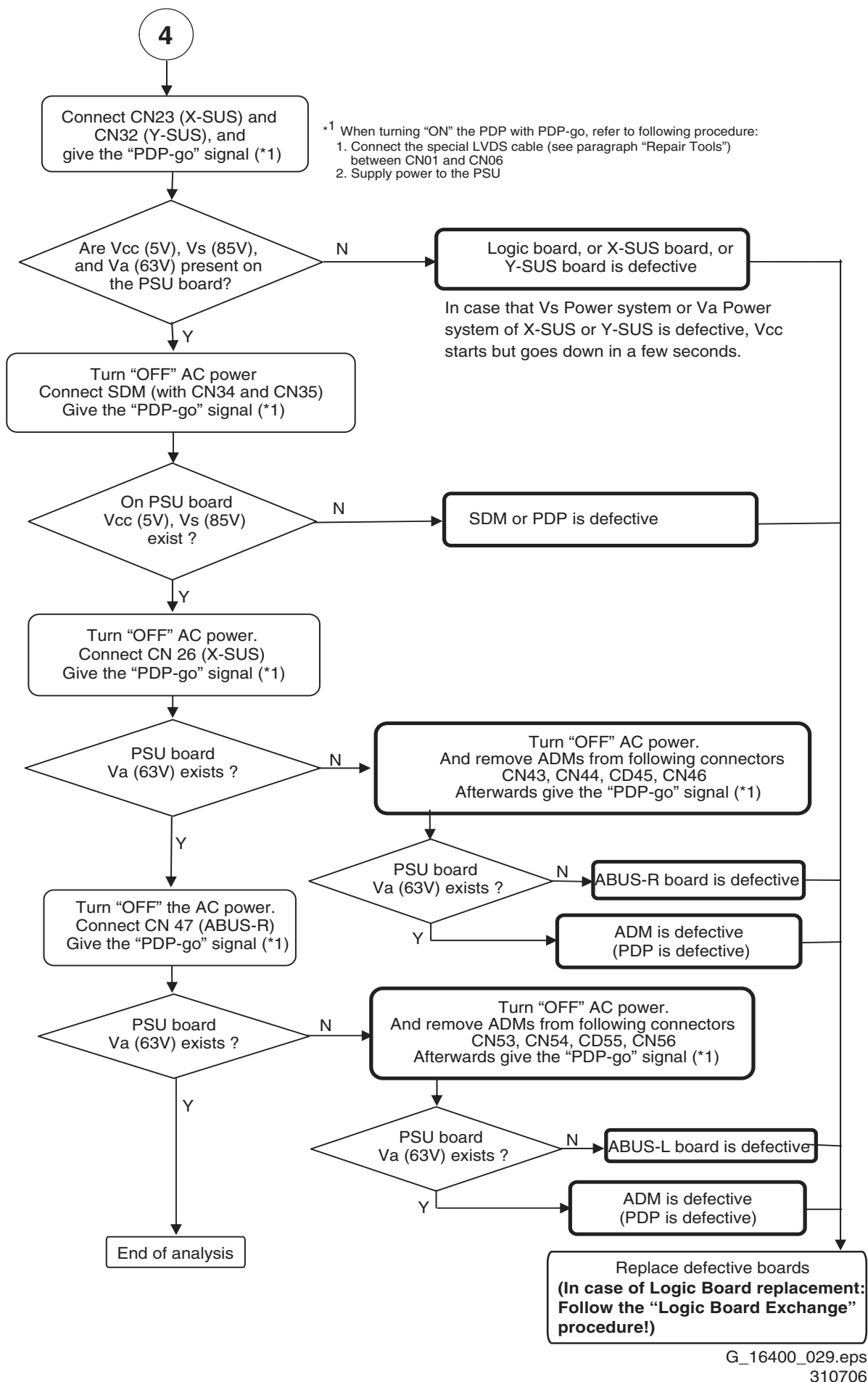
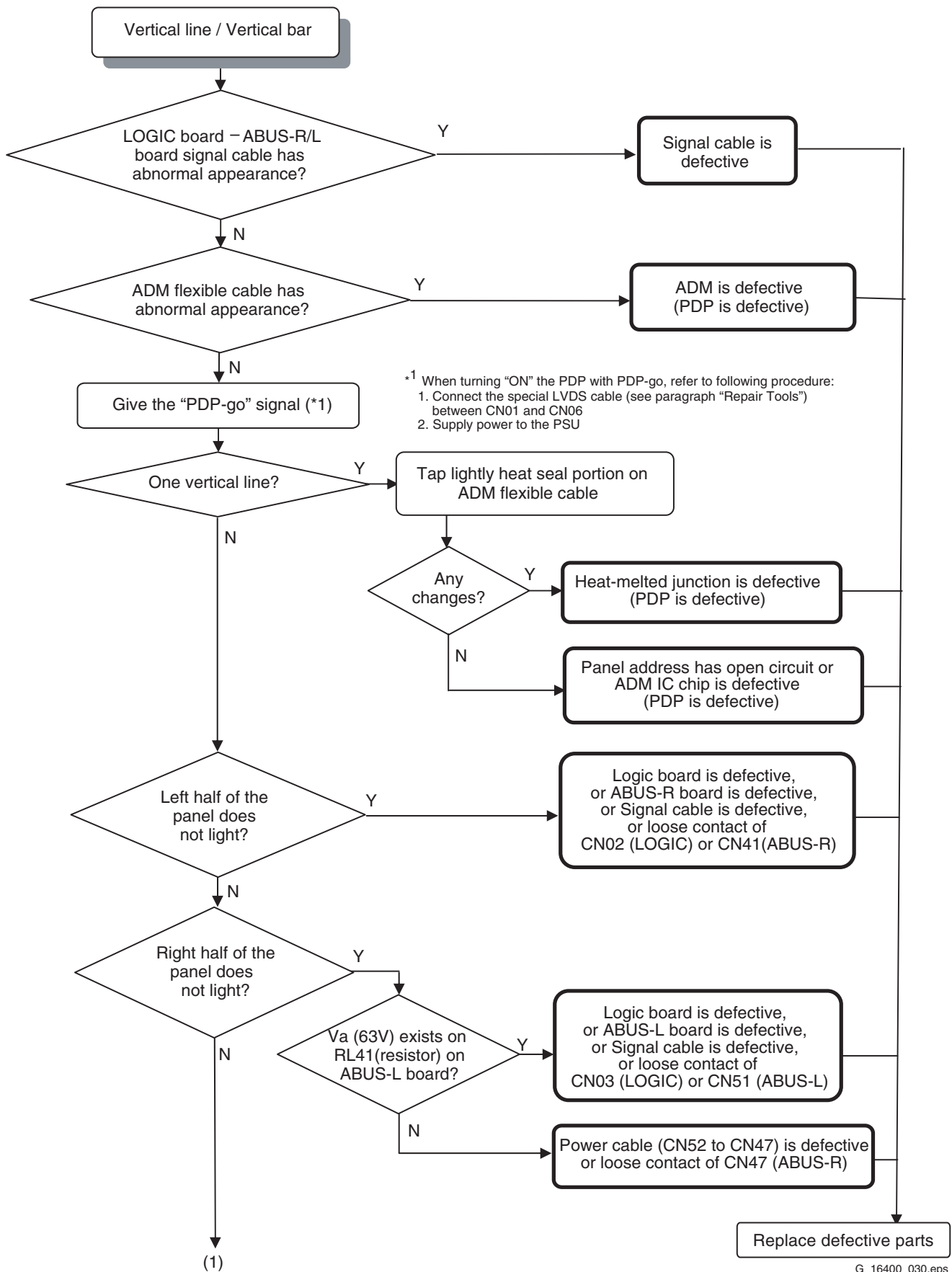


Figure 5-8 Short circuit check on boards and power supply lines (3/3)

"Vertical line/Vertical bar" problem analysis procedure



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Figure 5-9 Vertical line / vertical bar problem analysis procedure (1/3)

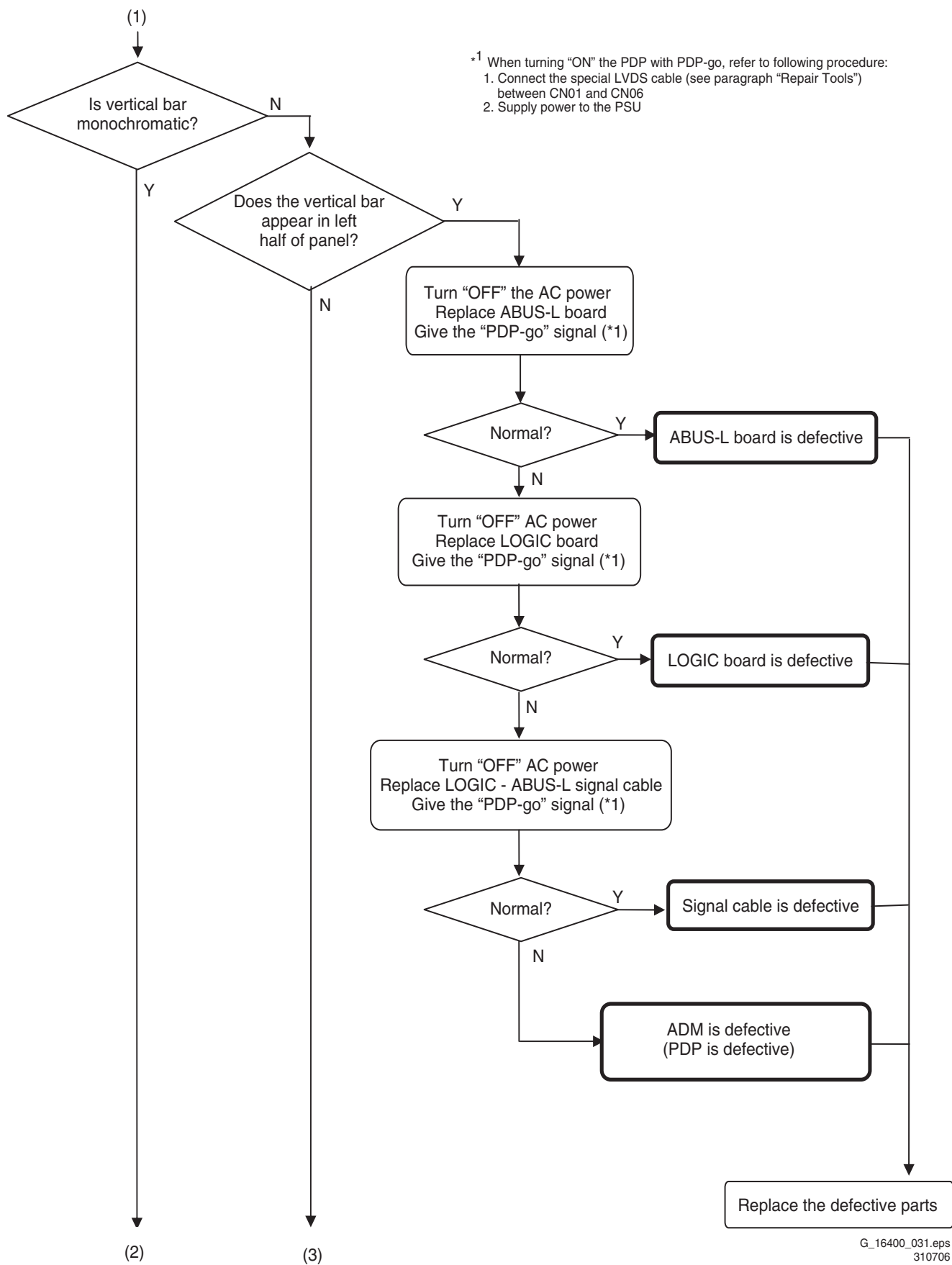


Figure 5-10 Vertical line / vertical bar problem analysis procedure (2/3)

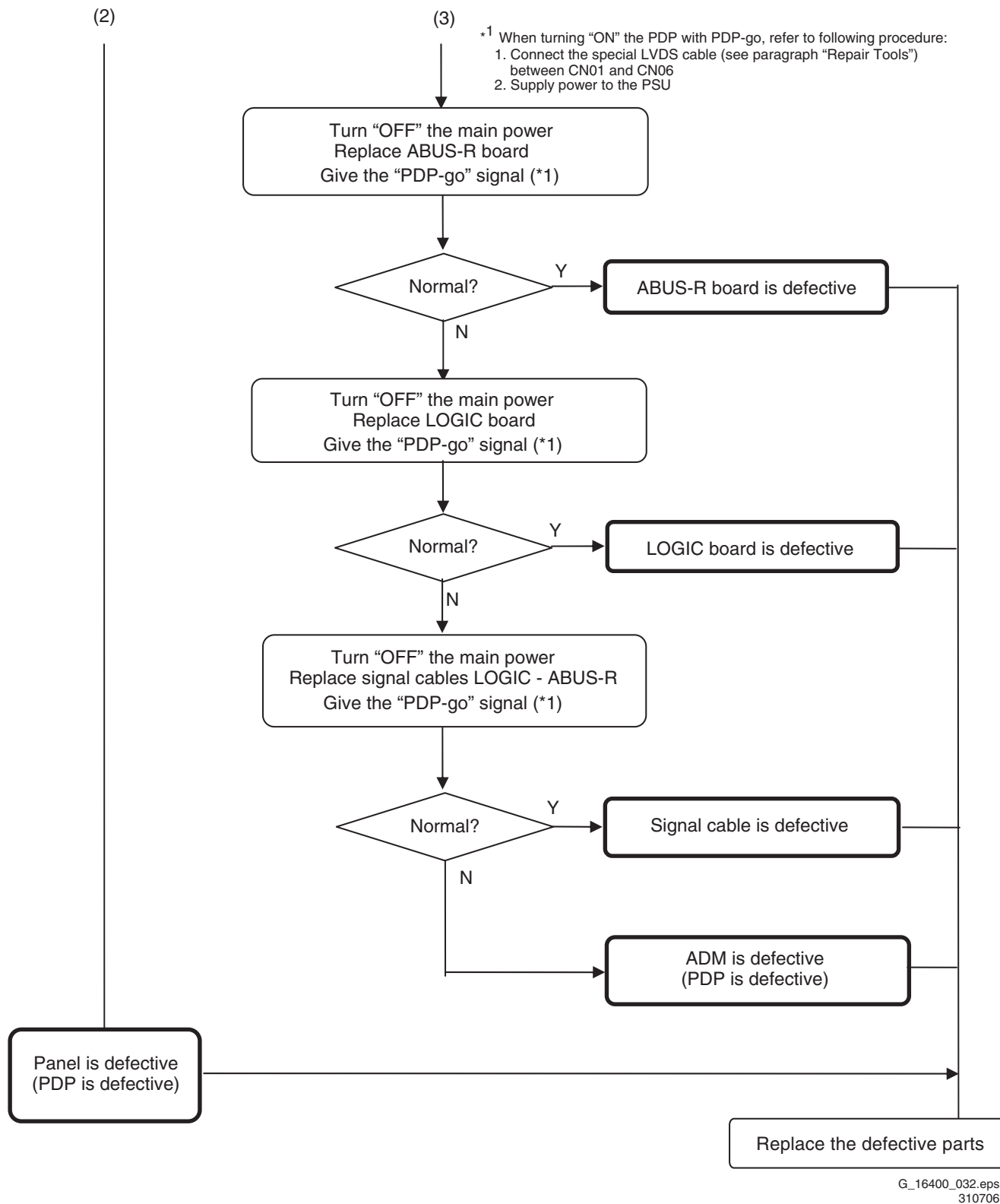


Figure 5-11 Vertical line / vertical bar problem analysis procedure (3/3)

"Horizontal bar" problem analysis procedure

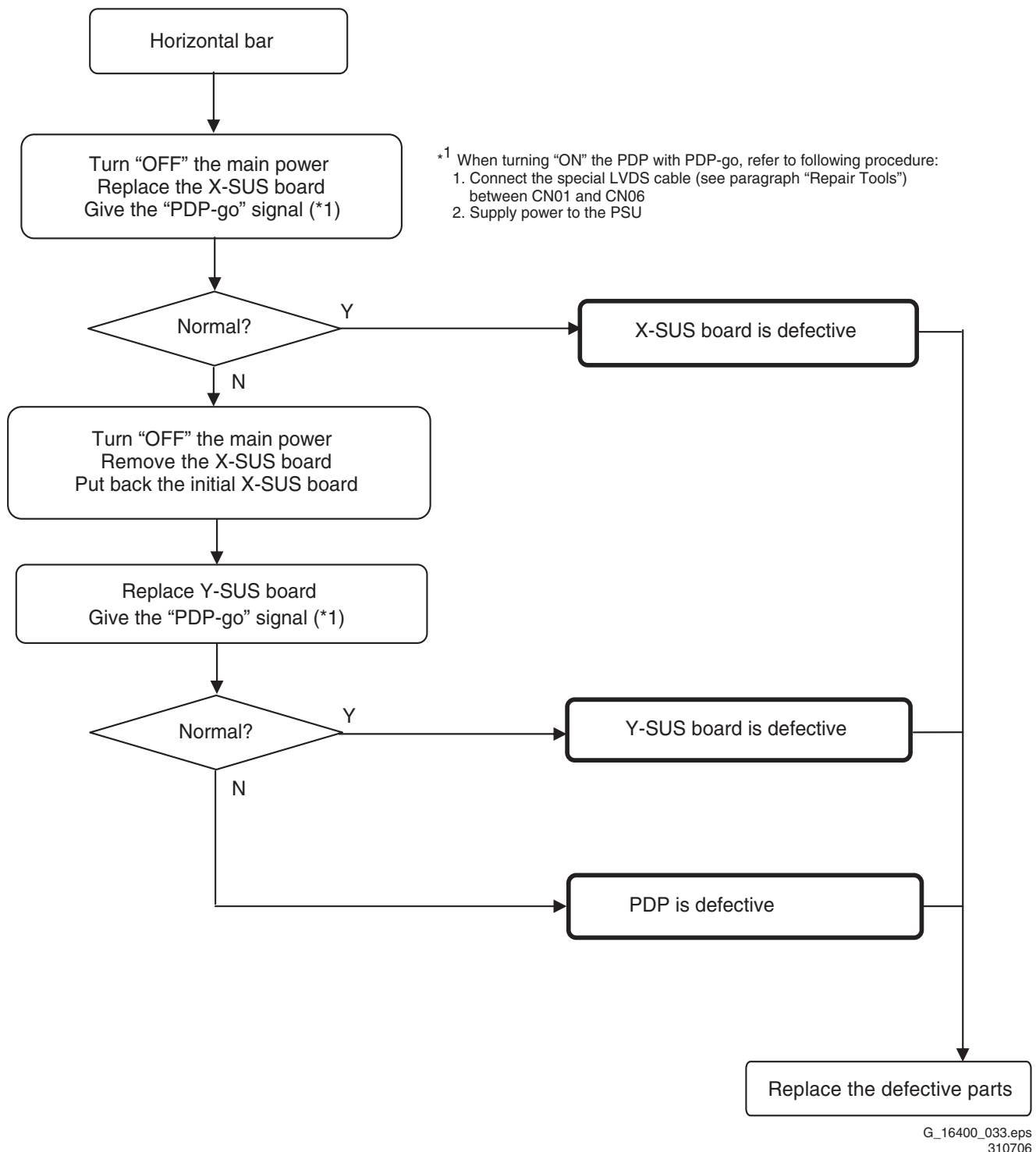
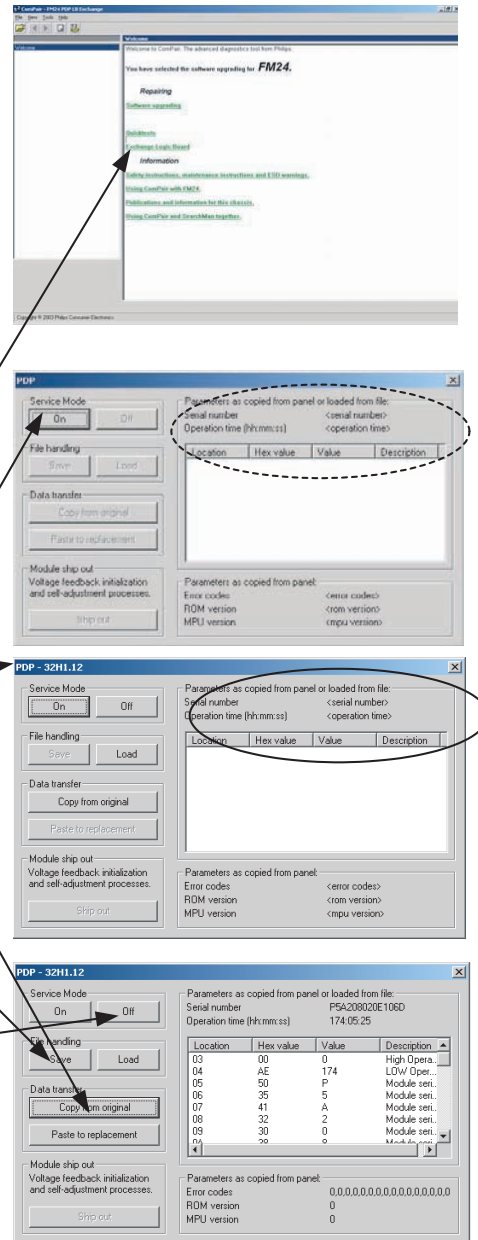
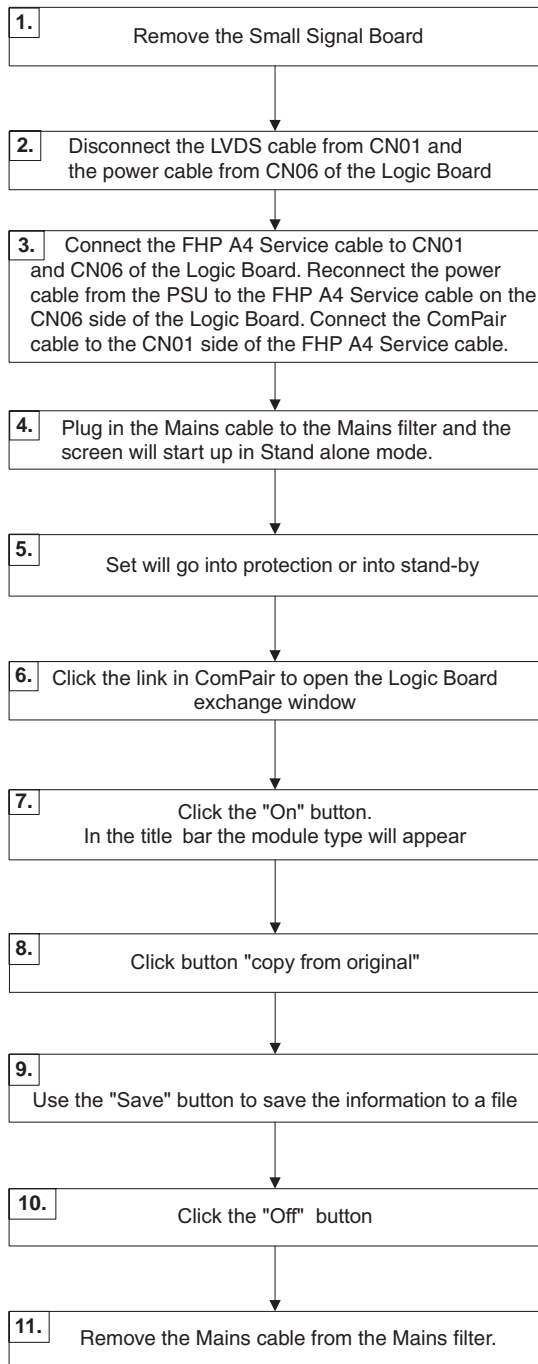


Figure 5-12 Horizontal line problem analysis procedure

Remark: Do not interchange boards between different PDPs, this might damage your PDP

Logic Board Exchange (1)

1. Copy NVM Data from defective Logic Board



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Figure 5-13 Logic Board Exchange (1/2)

1. Remove the SSB. Now you can reach the cable going to connector CN01 on the Logic Board.
2. Unplug the LVDS cable from the SSB at connector CN01. Also unplug the power cable at CN06.
3. Connect the FHP A4 service cable to CN01 and CN06. Connect the ComPair I2C cable to the CN01 side of the service cable, and the power cable to the CN06 side of it.
4. Plug in the mains cable. The display starts up in stand-alone mode.
5. Click the link in ComPair to open the Logic Board exchange window.
6. Click the 'On' button. In the title bar the module type will appear: 42A4, or something similar.
7. Click button 'Copy from original'
8. The data is read from the EEPROM on the logic board and displayed in the list.
9. Use the 'Save' button to save the information to a file. This is optional, but better safe than sorry!
Note: If you close the window without saving, all settings

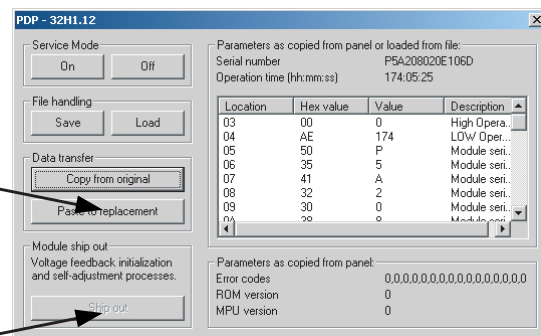
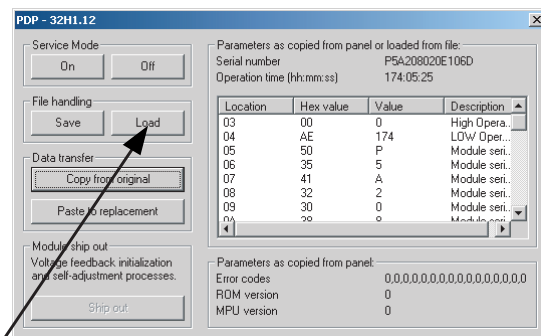
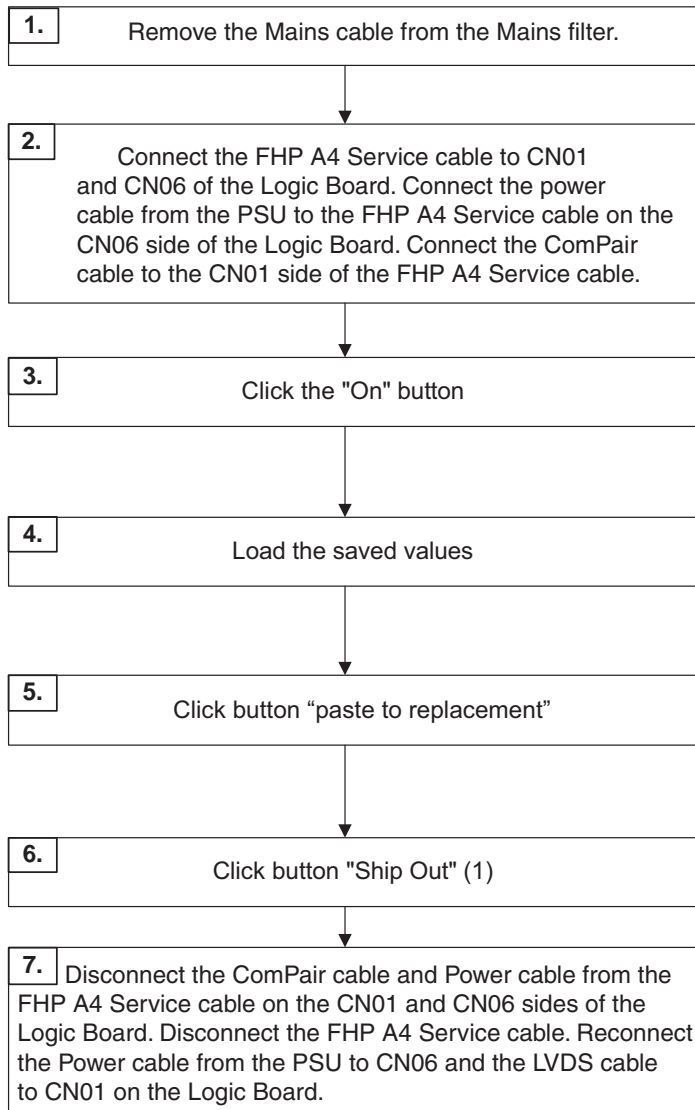
will be lost. If you intend to close this window before replacing the board, you should save the settings so you can load them later.

10. Click the 'Off' button.

11. Switch off the set and replace the Logic Board with another one.

Logic Board Exchange (2)


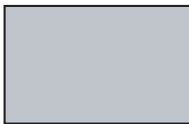

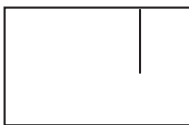
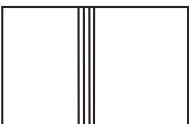

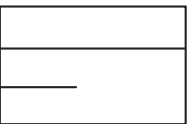
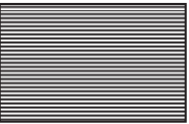
2. Write NVM Data to the new Logic Board



(1) The PDP screen will be blanked for about 15s, then 15s later, the 'Ship out' process will end

Figure 5-14 Logic Board Exchange (2/2)

1. Switch off the set and replace the Logic Board by another one. Now connect the service cable to connectors CN01 and CN06. Connect the power cable to the CN06 side of the service cable, and the ComPair cable to the CN01 side.
2. Restart the display with the new board.
3. Click the 'On' button.
4. The module type will again appear in the title bar. This may be different now from step 6 on the previous page, because now another Logic Board is used. If you closed the window after step 9 and did save the settings you should load them now. Use the 'Load' button to do so.
5. Click button 'Paste to replacement'. The settings previously copied from the old board are now written to the new board. If successful the button 'Ship out' will be enabled.
6. Click button 'Ship out'.
7. Now a process of voltage feedback initialization and self-adjustment starts. This will take a few seconds. When ready you can switch off the display.
8. Disconnect ComPair and remove the service cable, plug in the power cable at CN06 and the original LVDS cable at CN01.

NO	Fault contents	Fault status		Suspected fault location	Analysis procedure and measure
1	Entire screen does not light.	After momentarily going on, the screen becomes black immediately or after a few seconds (main power is turned off.)		X-SUS Y-SUS PSU Panel chassis LOGIC ABUSL ABUSR	Refer to "Entire screen does not light"
2		Screen lights dimly even on the back screen.		LOGIC	Replace the LOGIC board, following the "Logic Board Exchange" procedure
3	Vertical line	Single vertical line (of different color)		Panel chassis LOGIC	Refer to "Vertical line/bar"
4		Vertical line from the middle of effective scan area (vertical line of different color)		Panel chassis	Replace panel chassis
5	Vertical bar	Bar width of 1/7 of horizontal size or in multiples of 1/7, is displayed. Abnormal display		Panel chassis ABUS-L ABUS-R LOGIC Above boards are connected.	Refer to "Vertical line/bar"
6		Bar width of 3/7 or 4/7 of the screen width, is displayed. Abnormal display (vertical line of different color)		ABUS-L ABUS-R LOGIC Above boards are connected.	
7	Horizontal line	Single horizontal line (no light) or single horizontal line does not light among the effective scanning area. Single horizontal line does not light.		Panel chassis X-SUS Y-SUS ABUS-L ABUS-R	Replace panel chassis
8		Every other line (no light) in entire screen		X-SUS Y-SUS ABUS-L ABUS-R	Replace X-SUS, Y-SUS

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Figure 5-15 Fault symptom overview (1/2)




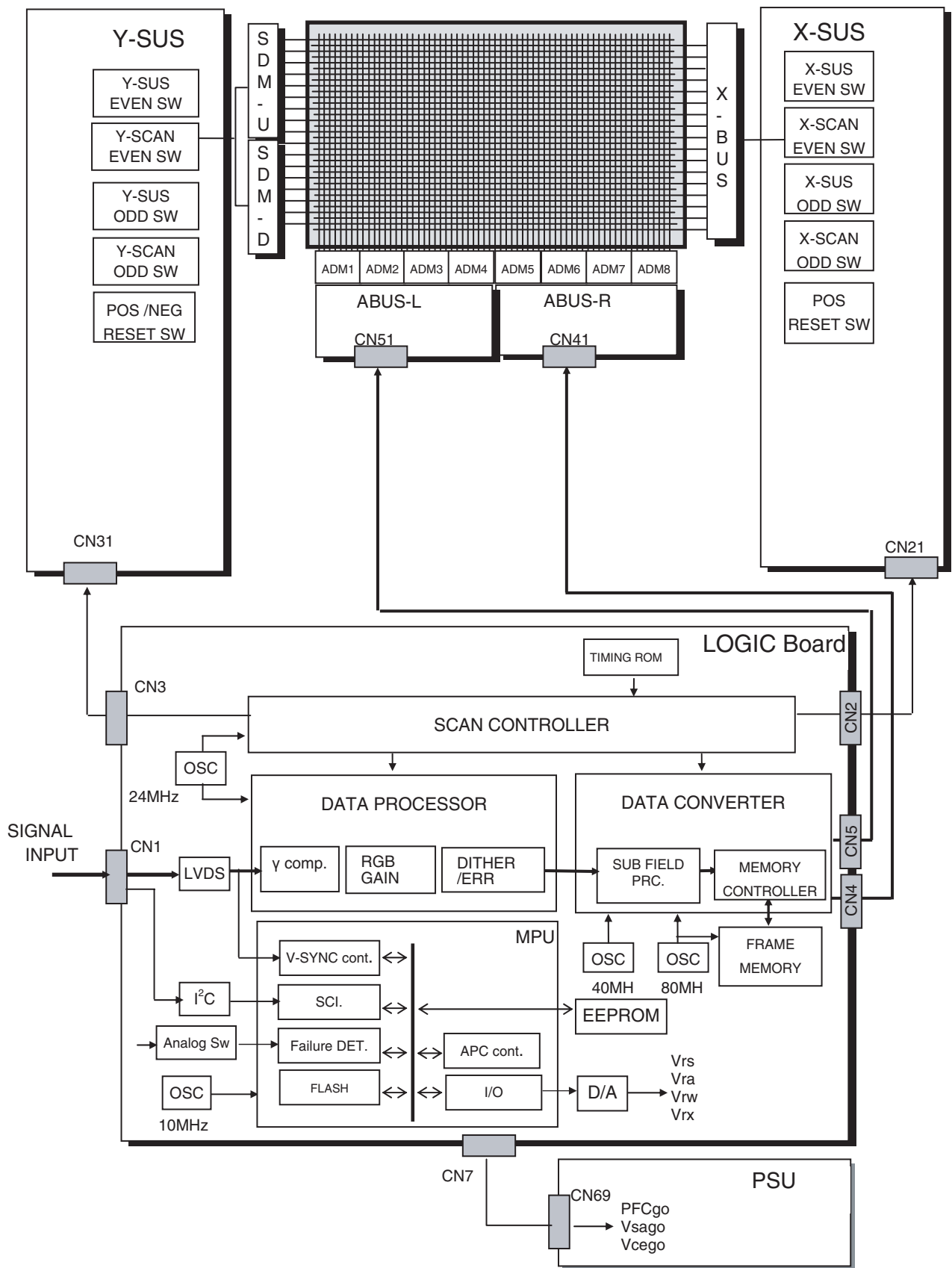
NO	Fault contents	Fault status		Suspected fault location	Analysis procedure and measure
9	Horizontal bar	Bar width of 1/8 or multiples of 1/8 of the screen height, is displayed. Abnormal (screen does not light)		Panel chassis	Replace panel chassis
10		Bar width of 1/2 of the screen height. Abnormal display (screen does not light)		Panel chassis Y-SUS X-SUS Above boards are connected.	Refer to "Horizontal bar"
11	Image sticking (Image retention)	Fixed display contents are always displayed.		Panel chassis	Perform all white heat run. After judgement, replace panel chassis
12	Twinkle	The entire screen momentarily becomes brighter or darker.		Poor connector contact	
13	Flicker	The entire screen flickers continuously.		Poor connector contact (CN2,3,21,31)	Connector / cable re-connection or cable exchange
14	Luminance is abnormal	Screen is too dark or too bright. (Out of specifications)			
15	Chrominance is abnormal	Colors cannot be displayed correctly.		LOGIC board	Replace Logic board, following the "Logic Board Exchange" procedure
16	Sync is disturbed				
17	Picture distorted				
18	Steps of gradation are skipped	Luminance linearity is poor.			
19	Abnormal sound			PSU X-SUS Y-SUS (Core is broken, or transformer is abnormal.)	Locate cause of abnormality from listening and viewing. Replace the cause of problem.
20	Control on external communication is abnormal	Contrast, color temperature adjustment and Y cannot be changed.		LOGIC board	Replace Logic board, following the "Logic Board Exchange" procedure

Figure 5-16 Fault symptom overview (2/2)

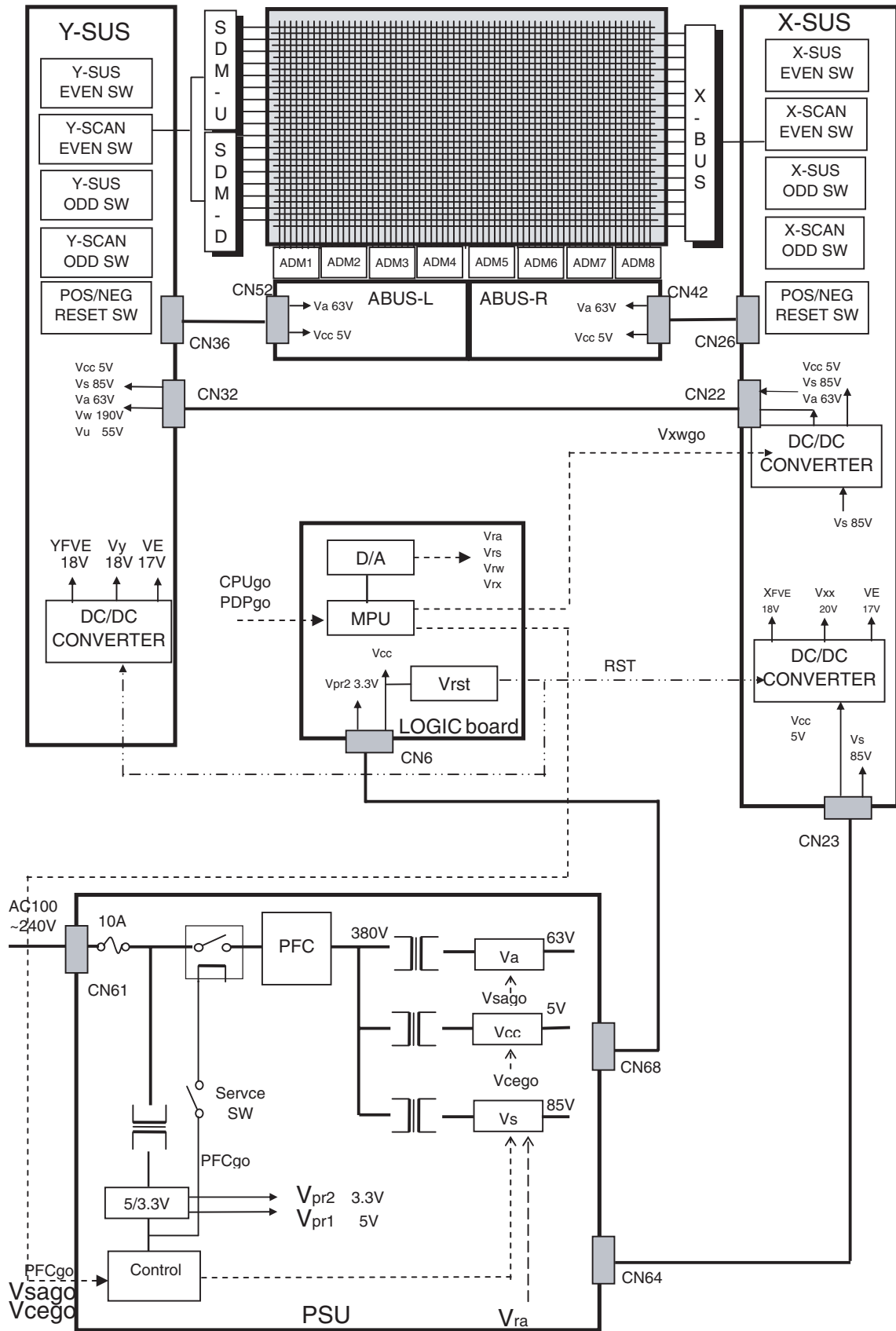
6. Block Diagrams, Test point Overview, and Wave Forms

6.1 Block Diagrams



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Figure 6-1 Signal block diagram



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Figure 6-2 Power block diagram

6.2 Test Points

Not available.

6.3 Wave Forms

Not available.

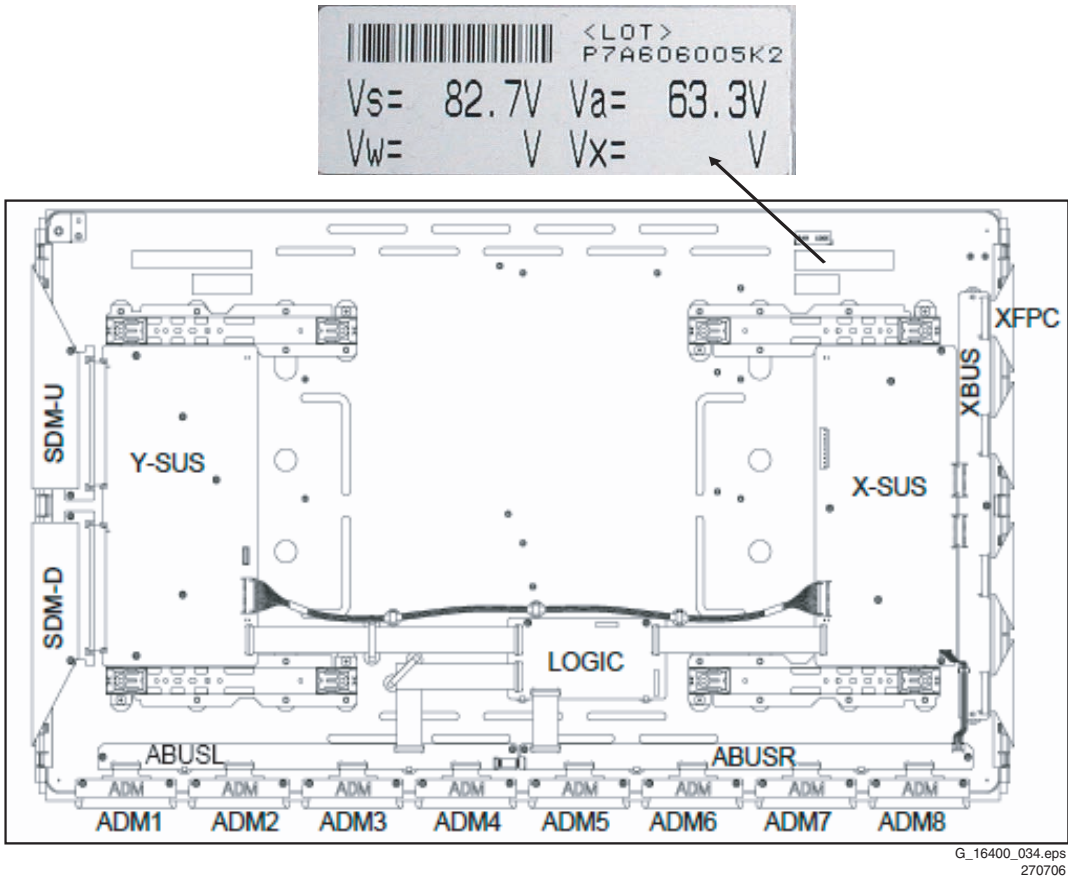
7. Circuit Diagrams and PWB Layouts

Not applicable.

8. Alignments

8.1 Voltage Setting Procedure

On the back of the PDP, in the top right hand corner, you find the Voltage Setting label:



This Voltage Setting label shows the following messages:

Table 8-1

Item	Adjustment items	Measurement point	Adjustment value (conditions)
1	Vs voltage adjustment	Pins 8-9-10 of CN23 on the X-SUS board	Voltage setting label indication value* ± 1%
2	Va voltage adjustment	Pin 1 of CN23 on the X-SUS board	Voltage setting label indication value* ± 1%

If the voltage adjustments Vs and Va on the Power Supply Unit must be performed, depends on the version of the Power Supply Unit.

9. Circuit Descriptions and Abbreviation List

9.1 Board Function Description

9.1.1 Logic Board Function

Data Processor

- Gamma adjustment (1 / 2.2 / 2.4 / 2.6 / 2.8).
- NTSC/EBU format (Colour matrix) Switch.
- RGB gain Control (White balance adjustment, amplitude limitation).
- Error diffusion technology (grey scale adjustment).
- Dither (grey scale adjustment).
- Burn-in pattern generation.

Data Converter

- Quasi out-line adjustment (luminous pattern control).

Scan Controller

- Address driver control signal generator (ADM).
- Scan driver control signal generator (SDM).
- X/Y sustain control signal generator.

Waveform ROM

- Waveform pattern for drive / timing memory.

MPU

- Synchronous detection.
- System control.
- Driving voltage (Va, Vs, Vr, Vw) adjustment.
- Abnormal watch (breakdown detection) / abnormal processing.
- I_s (sustain) current control (sustain pulse control).
- I_a (address) current control (sub-field control).
- External communication control.
- Flash memory (firmware).

EEPROM

- Control parameter memory.
- Counts operating time (number of hours).
- Abnormal status memory (16 places).

9.1.2 Function of X-SUS Board

DC/DC power supply block

- Vcc (+5V) -> Ve (+17V) / XFve (+18V, floating).

X Switching Block

- Switching during address period.
- Switching during sustain period.
- Switching during reset period.

Current Detector Block

- I_{sx} (sustain) current detection.
- I_{ax} (address) current detection.

9.1.3 Function of Y-SUS Board

DC/DC Power Supply Block

- Vcc (+5V) -> Ve (+17V) / YFve (+ 18V, floating)
- Vs (+85V) -> Vw (+185V)

Switching Block

- Switching during address period.
- Switching during sustain period.
- Switching during reset period.

Current Detector Block

- I_{sy} (sustain) current detection.
- I_{sp} (SDM) current detection.

9.1.4 Function of ADM Board

Address Driver Module

- Supplies voltage Va to the glass plate.

9.1.5 Function of SDM Board

Scan Driver Module

- Supplies voltage Vs to the glass plate.

9.1.6 Function of PSU Board

Stand-by Power Supply Block

- AC100-240: +5V & +3V3 Stand-by.

PFC Block (AD/DC Power Supply Block)

- AC100-240: +390V.

AD/DC Power Supply Block

- +380V, Vcc (+5V), Vs (+80V), Va (+60V).

Current Detection Block

- I_a (address) current detection.

Abnormal Voltage Monitoring

- Vs excess voltage monitoring.
- Va excess voltage monitoring.

9.2 Differences between the Versions A1, A2, A3, and A4

9.2.1 Specifications

Table 9-1 Specifications

Item	42A1	42A2	42A3	42A4
Dimensions (mm)	994 x 585 x 66	994 x 585 x 66	994 x 587 x 66	994 x 587 x 66
Weight (kg)	16	16	16	16
Resolution (h x v)	1024 x 1024	1024 x 1024	1024 x 1024	1024 x 1080
Brightness (cd/m ²) (display load 1%, standard)	1,100	1,200	1,400	1,400
Contrast (dark room)	1000 : 1	1000 : 1	3000 : 1	3000 : 1

9.2.2 Layouts

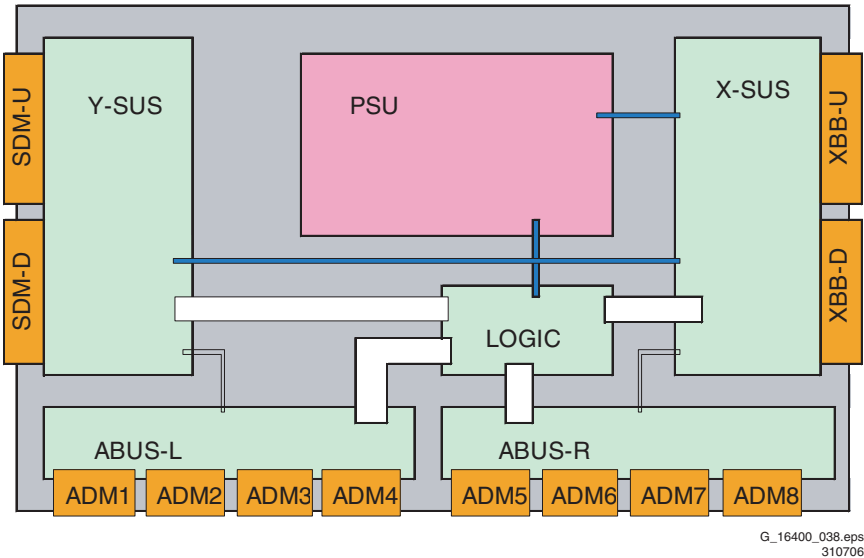


Figure 9-1 Layout 42A1

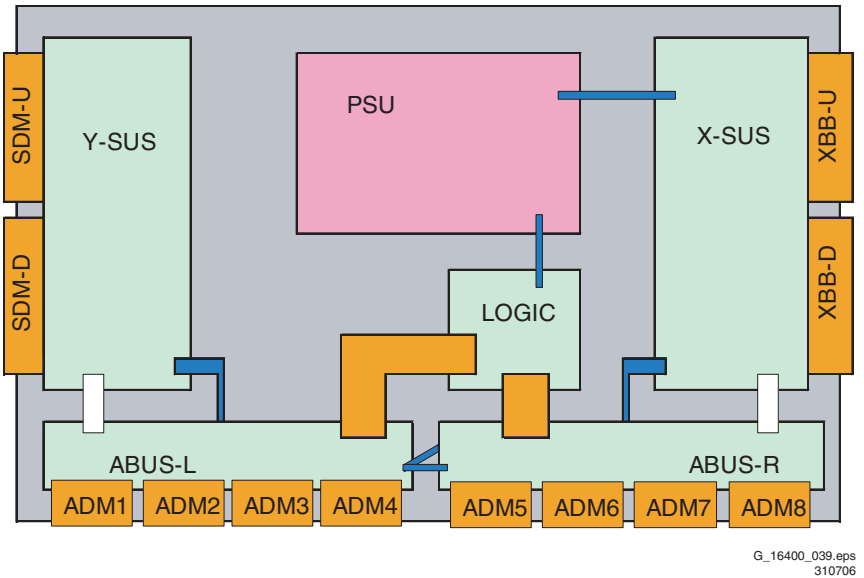


Figure 9-2 Layout 42A2

Differences with respect to 42A1:

- The signal cable arrangement has changed.
- The power cable arrangement has changed.
- An 80-pin FPC cable is used between Logic Board and ABUS-L and ABUS-R.
- The signal cable from the PSU to the Logic Board is standardised.
- The power cable from the PSU to the Logic Board is standardised.

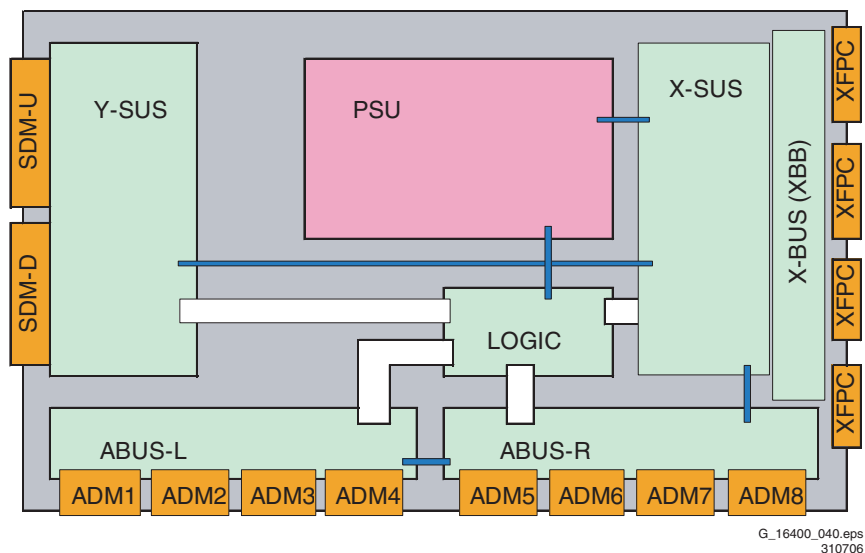


Figure 9-3 Layout 42A3

Differences with respect to 42A2:

- The signal cable arrangement has changed (now similar to 42A1).
- The power cable arrangement has changed (now similar to 42A1).
- The XBB has been replaced by XFPC and X-BUS.
- A new connector type is used on ABUS-L, ABUS-R, and X-BUS.

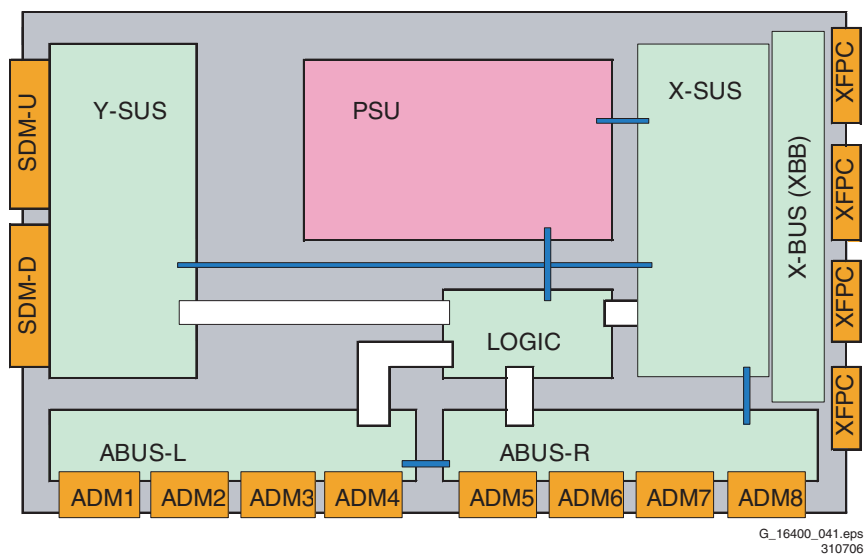


Figure 9-4 Layout 42A4

Differences with respect to 42A3:

- There are no differences in cable arrangements with respect to 42A3.

9.3 List of abbreviations

ADM	Address driver module
Burn-in rack	Test equipment of the shelf test in which the PDP unit is left to stand in drive condition
CPU	The unit for controlling the circuit operation
DOXE	The control voltage for even-numbered lines in the X direction
DOXO	The control voltage for odd-numbered lines in the X direction
DOYSD	Used in the drive voltage in the Y direction (down)
DOYSU	Used in the drive voltage in the Y direction (up)
External power ON	Running the external powers (Vcc, Va, Vs) on the designated voltage. Unless otherwise specified
External power OFF	Making the external powers (Vcc, Va, Vs) to stop their operation completely. Unless otherwise specified
Flexible cable	The cable to connect the electric circuit to the panel
Flicker	Continuous switching between bright and dark views by the PDP itself
Gradation	Shading of the display colour
OPUMP	The name of a circuit where the current from X/Y-SUS is returned
Oscilloscope	A device that allows the flow and strength of the running current to be visually checked and measured
Panel	The indication part of the plasma display panel (PDP)
Panel voltage	The voltage required operating the PDP normally
Parts	Each PC board and parts mounted in the PC boards
PDP	Plasma display panel abbreviated

Probe	A cable with contact finger that can transfer the status of the electric circuit to be measured to an oscilloscope
Protection cover	A cover made of aluminium to protect the PDP entirely during test
ROM	Memory that stores the drive sequence and other data
SCAVIO	Scaler Control Audio Video Output & Input
SDM	Scan driver module
SUS	X-SUS or Y-SUS
Tapping	Light impact
Unit of COM	The unit of circuits connected to the panel with flexible cable (YCOM UP/DOWN, X-BUS UP/DOWN, address sections, the unit of PC boards in ACOM 1 to 5).
Va	The power supply at 60 V, which is used to write data on the panel
Vcc	The power supply at 5 V, which is used to operate the logic section mainly
Vs	The power supply ranging from 127 V to 180 V, which is used to maintain display data. In addition, this can serve as the primary side for the secondary voltage (Vw, -Vy, Vsc)
Solid white	A condition when the screen display is entirely white
X-SUS	The name of the circuit that controls the panel operation in the X direction
YCOM	The circuit used to output a panel Y line selection signal and the voltage of a display data keep signal
YCOMDV	The name of the panel drives voltage signal output from YCOM UP/DOWN section
Y-SUS	The name of the circuit that controls the panel operation in the Y direction

10. Spare Parts List

For spare parts list see chapter 5

11. Revision List

This manual is a supplement to the following service manuals:

Table 11-1 Overview of chassis and manuals, covered by this manual

Display type	Model CTN	Chassis	12NC Manual
42" A4	42PF5331/10	LC4.41E AA	3122 785 16240
	42PF5411/10	LC4.41E AA	3122 785 16240
	42PF9531/79	BJ3.0A PA	3122 785 15980
	42PF9531/93	BJ3.0A PA	3122 785 15980
	42PF9531/98	BJ3.0A PA	3122 785 15980
	42PF9631D/10	BJ3.0E PA	3122 785 15960

11.1 Service Manual xxxx xxx xxxx.0

First release.

Service Service Service

LGE PDP 2K5

PDP42V7A062*

PDP42V7A462*

PDP42V7K062*

PDP42V7K462*

Service Manual

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Subject to modification

EN 3122 785 15593



PHILIPS

1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

1.1 Technical Specifications PDP42V7*

1.1 Technical Specifications PDP42V7*

The PDP Module is divided into a Panel part and a Drive part. The Panel part consists of Electrodes, Phosphor, various dielectrics, and gas, while the Drive part includes electronic circuitry and PWBs.

1.1.1 General Specification

Model Name	: PDP42V7*
Number Of Pixels (HxV)	: 852 (*3) x 480
Pixel Pitch (HxV μm)	: 1080 x 1080
Cell Pitch (HxV μm)	: 320 x 1080
	: (Base: Green Cell)
Display Area (HxV)	: 920.1x518.4 \pm 0.5 mm
Outline Dimension (HxVxD)	: 1005x597x60.6 \pm 1mm
Colour Arrangement	: RGB closed type
Number Of Colours (RxGxB)	: 1024 x 1024 x 1024
Weight	: 14.7 \pm 0.5 kg
Aspect Ratio	: 16:9
Peak Brightness	: Typical 1500 cd/m ² : (1/10 white window) : Average 100:1 : (Light room 100 Lx at centre)
Contrast Ratio	: Typical 10000:1 : (Dark room 1/10 white window, white window pattern at centre)
Power Consumption	: Typical 200 W : (Full White) ¹⁾
Lifetime	: Over 60,000 Hrs. (Initial brightness 1/2)

Note 1) It can increase to 300 W depending on input image.

1.1.2 Definitions

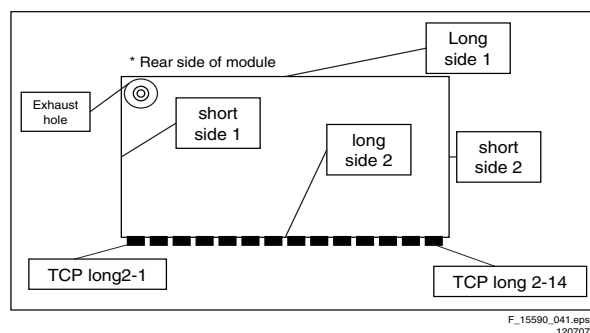


Figure 1-1 Definition of module position



Figure 1-2 Identification label

1. Model name.
2. Bar code (Code 128, contains the manufacture no.).
3. Manufacture no. (Module serial no.).
4. The trade name of LG Electronics.
5. Manufacture date (Year & Month).
6. The place of origin.
7. Model suffix.

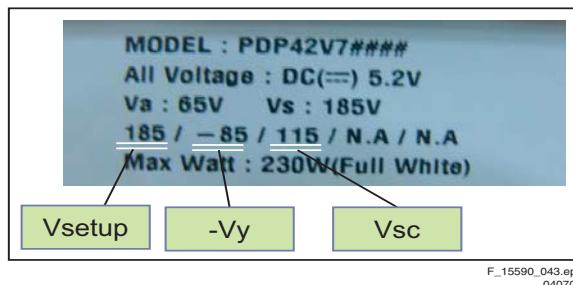


Figure 1-3 Voltage label (on rear side of module)

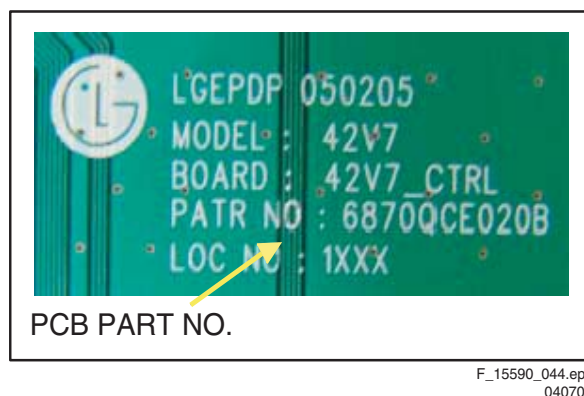


Figure 1-4 Part number printing (on board)

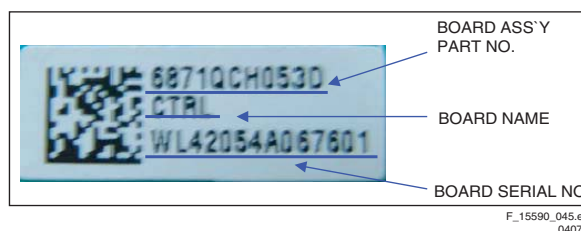


Figure 1-5 Part number label (on board)

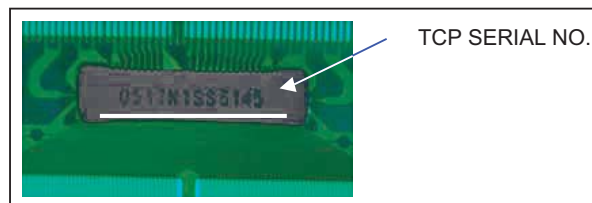


Figure 1-6 TCP serial no. (on TCP)

1.1.3 Connection Overview

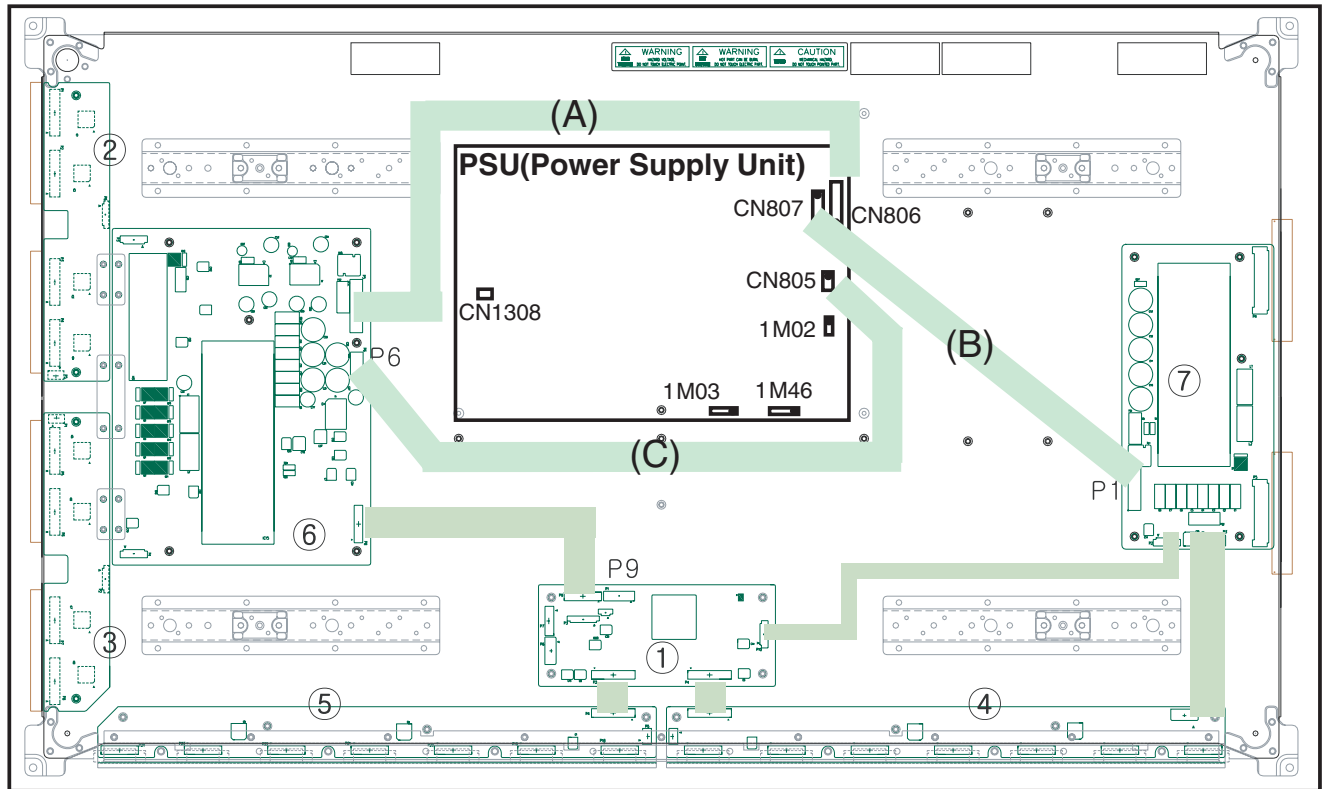
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Figure 1-7 Connector overview

Table 1-1 Connector signals

No	Connector	Input voltage & signal
P1	Z SUS board	5V, Va, Vs
P5	Y SUS board	Vs
P6	Y SUS board	5V
P9	CTRL board	Control signal

Table 1-2 PSU Cable Assies

No	LGE Part No.	Description
A	6631Q39032A	Cable assy 10p PSU->Y-SUS
B	6631Q39033A	Cable assy 8p PSU->Z-SUS
C	6631Q39034A	Cable assy 4p PSU->Y-SUS

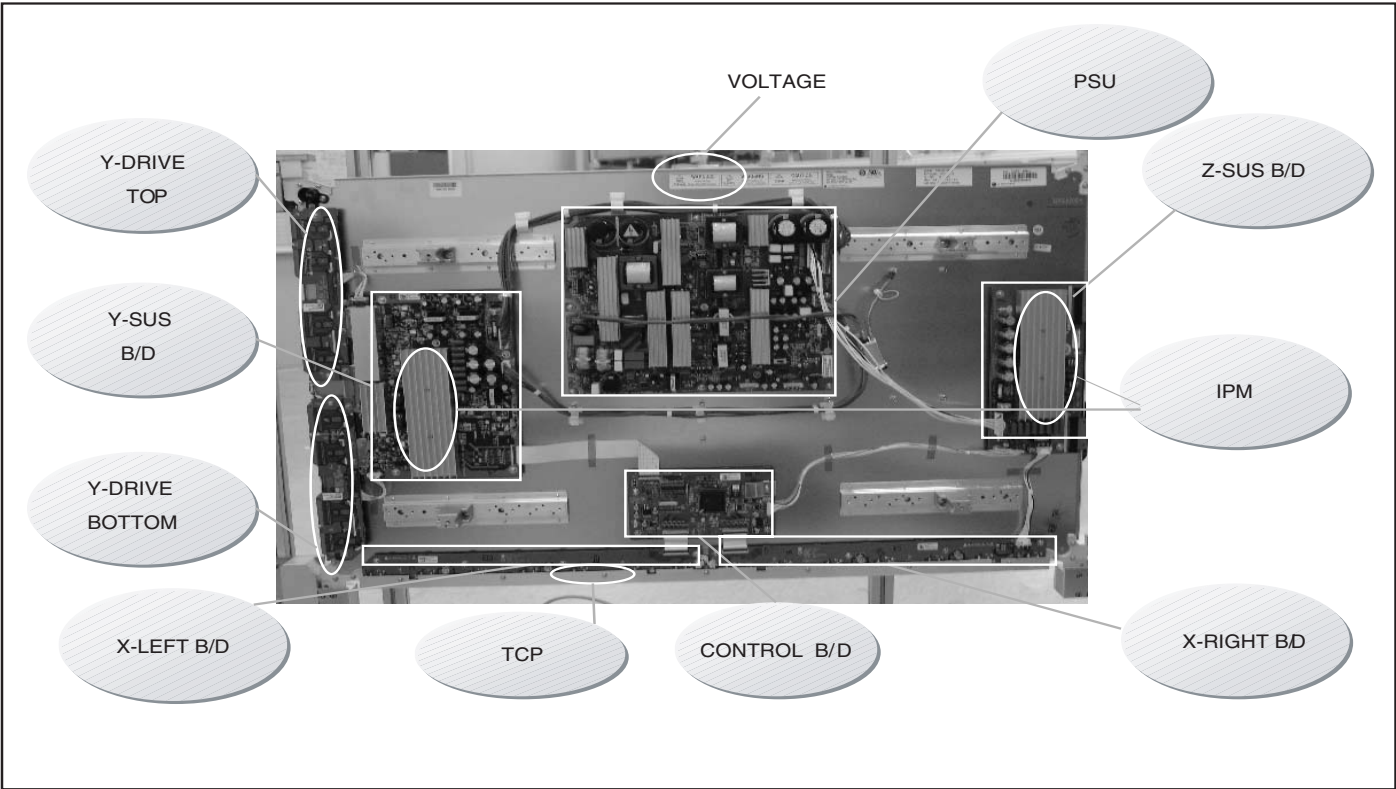
Table 1-3 PSU Connectors

No	Input voltage & signal
CN806	Vs: 187 V
CN807	Vs: 187 V, Va: 65 V, 5 V
CN805	5V
CN1308	AC 230 V
1M02	+Vsnd: +18 V, -Vsnd: -18 V
1M46	8V6: 8.6 V, +12V: 12 V, +5V2: 5.2 V, Vtun: 50 V
1M03	5V_sw: 5.2 V

Table 1-4 Board overview

No	Description of board assy
1	LVDS CTRL
2	Y-DRV TOP
3	Y-DRV BTM
4	X-R
5	X-L
6	Y-SUS
7	Z-SUS
For the correct ordercodes, see "Ch. 10 Spare Parts".	

1.1.4 Chassis Overview



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Figure 1-8 PWB location

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

2.1 Warnings

Notes:

- Only authorised persons should perform servicing of this module.
- When using/handling this unit, pay special attention to the PDP Module: it should not be enforced into any other way than next rules, warnings, and/or cautions.
- **"Warning"** indicates a hazard that may lead to death or injury if the warning is ignored and the product is handled incorrectly.
- **"Caution"** indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

2.1 Warnings

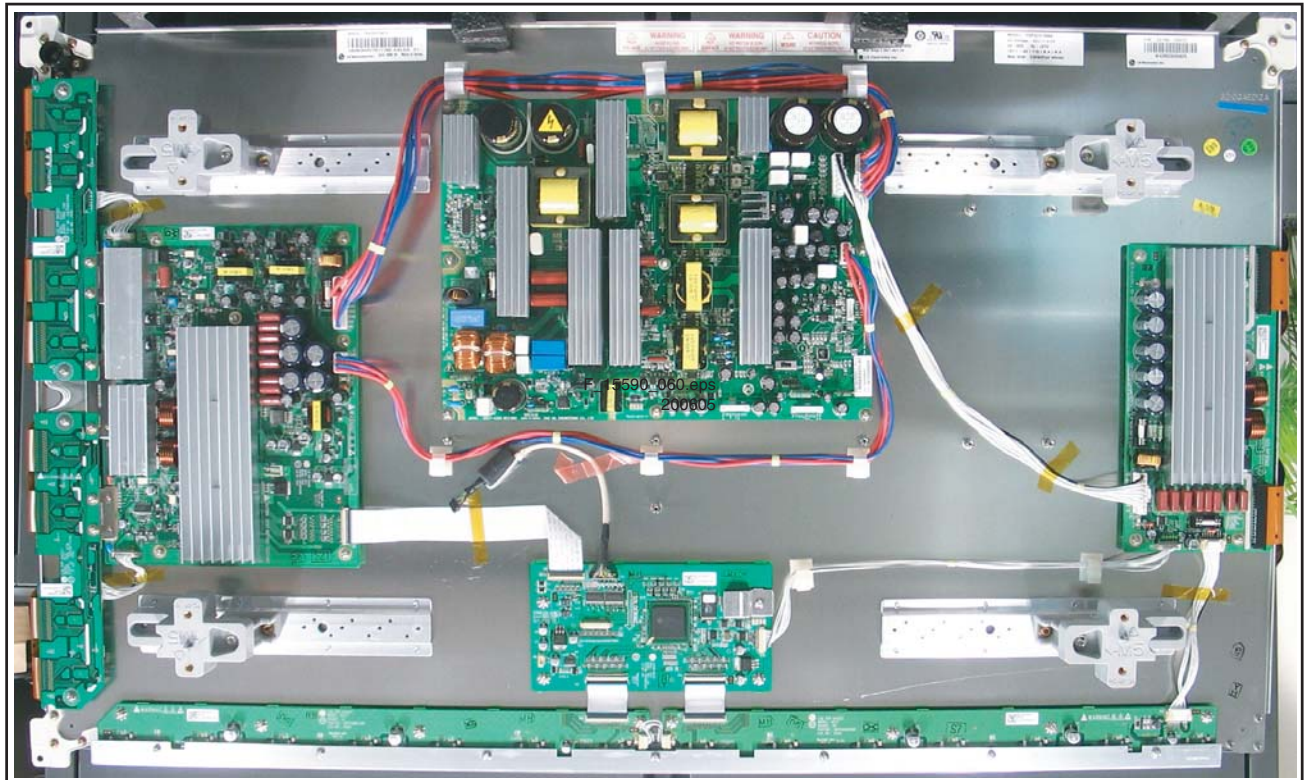
1. Do not touch the Signal and Power Connectors while this product operates. Do not touch EMI ground part and Heat Sink of Film Filter.
2. Do not supply a voltage higher than specified to this product. This may damage the product or can create hazardous situations.
3. Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where flammable materials surround it. Do not install or use the product in a location that does not satisfy specified environmental conditions. This may damage the product or can create hazardous situations.
4. If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn "off" the power. Continuing to use the product may cause electric shock or can create hazardous situations.
5. If the product emits smoke and abnormal smell, or makes an abnormal sound, immediately turn "off" the power. Continuing to use the product may cause electric shock or can create hazardous situations.
6. Do not (dis)connect the connector while power to the product is "on". It takes some time for the voltage to drop to a sufficiently low level after the power has been turned "off". Confirm that the voltage has dropped to a safe level before (dis)connecting the connector.
7. Do not pull out or insert the power cable from/to an outlet with wet hands. It may cause electric shock.
8. Do not damage or modify the power cable. It may cause electric shock or can create hazardous situations.
9. If the power cable is damaged, or if the connector is loose, do not use the product, otherwise, this can lead to hazardous situations or may cause electric shock.
10. If the power connector, or the connector of the power cable, is dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to hazardous situations.
11. The PDP module uses a high voltage (max. 450 V_{DC}). Keep the cautions concerning electric shock and do not touch the device circuitry handling the PDP unit. And because the capacitors of the device circuitry may remain charged at the moment of Power "off", standing for 1 minute is required in order to touch the device circuitry.
12. Because the PDP module emits heat from the glass panel part and the drive circuitry, the environmental temperature must not be over 40 deg. C. The temperature of the glass panel part is especially high owing to heat from internal drive circuitry. And because the PDP module is driven by high voltage, it must avoid conductive materials.
13. If inserting components or circuit boards in order to repair, be sure to fix a lead line to the connector before soldering.
14. If inserting high-power resistors (metal-oxide film resistor or metal film resistor) in order to repair, insert it 10 mm away from a board.
15. During repairs, high voltage or high temperature components must be put away from a lead line.
16. This is a cold chassis but you better use an isolation transformer for safety during repairs. If repairing the electricity source part, you **MUST** use the isolation transformer.
17. Do not place an object on the glass surface of the display. The glass may break or be scratched.
18. This product may be damaged if it is subjected to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses.
19. The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded.
20. This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.
21. Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.
22. Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.
23. Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction. Because this product uses a discharge phenomenon, it may take time to light (operation may be delayed) when the product is used after it has been stored for a long time. In this case, it is recommended to light all cells for about 2 hours (aging).
24. This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.
25. If faults occur due to arbitrary modification or disassembly, LG Electronics is not responsible for function, quality or other items.
26. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult LGE in advance.
27. Within the warranty period, general faults that occur due to defects in components such as ICs will be rectified by LGE without charge. However, IMAGE STICKING due to misapplying the above provision (12), is not included in the warranty. Repairs due to the other faults may be charged for depending on responsibility for the faults.
28. While assembling the PDP module into a set, use the EMI ground part of the Film Filter for grounding, **BEFORE** removing the protective film, to prevent that static electricity can damage the TCPs or boards

3. Directions for Use

Not applicable.

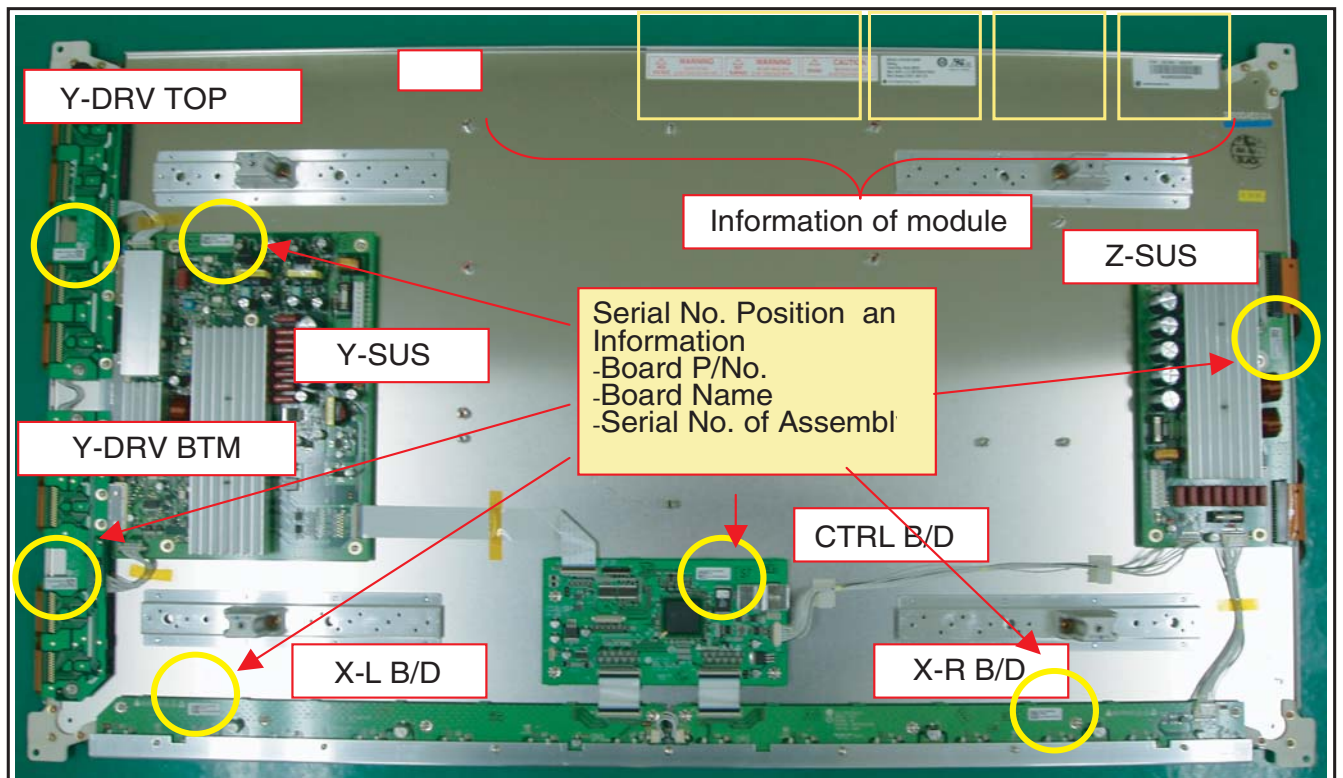
4. Mechanical Instructions

4.1 Mechanical Overview PDP42V7*



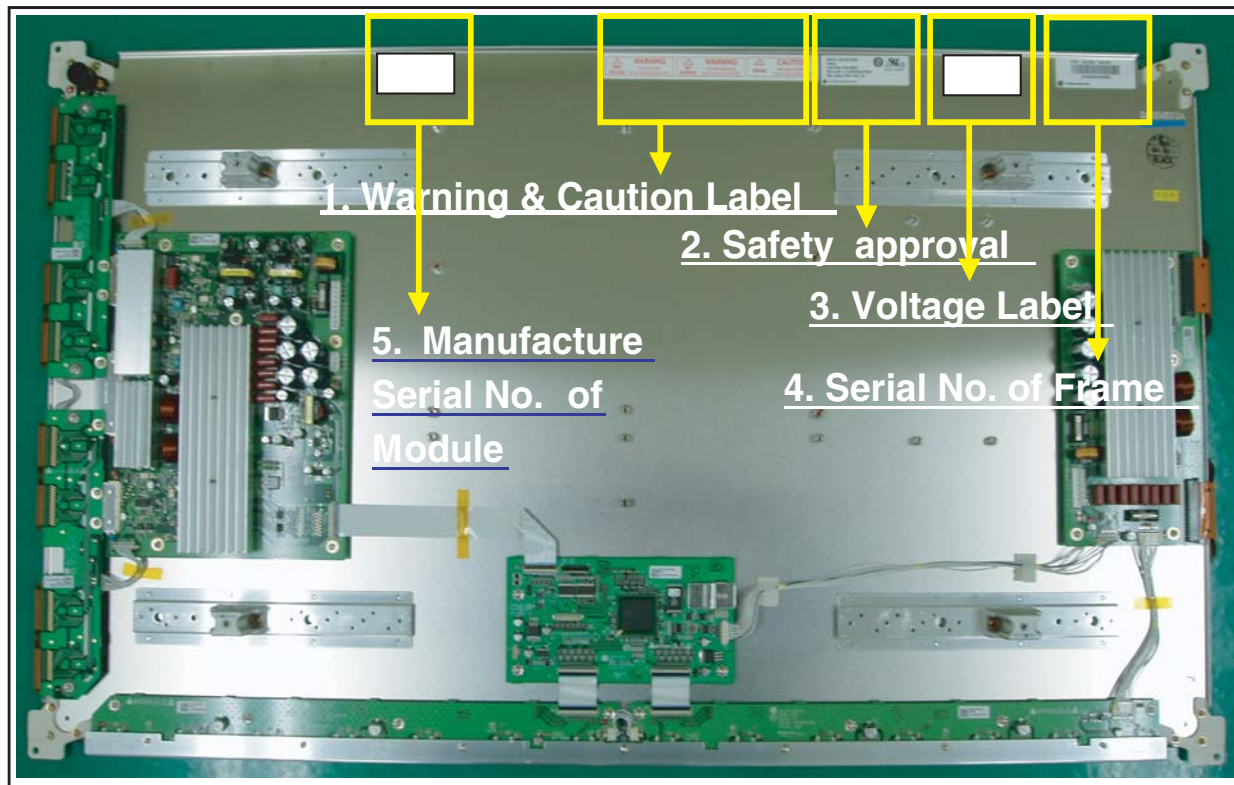
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010705

Figure 4-1 Cable dressing



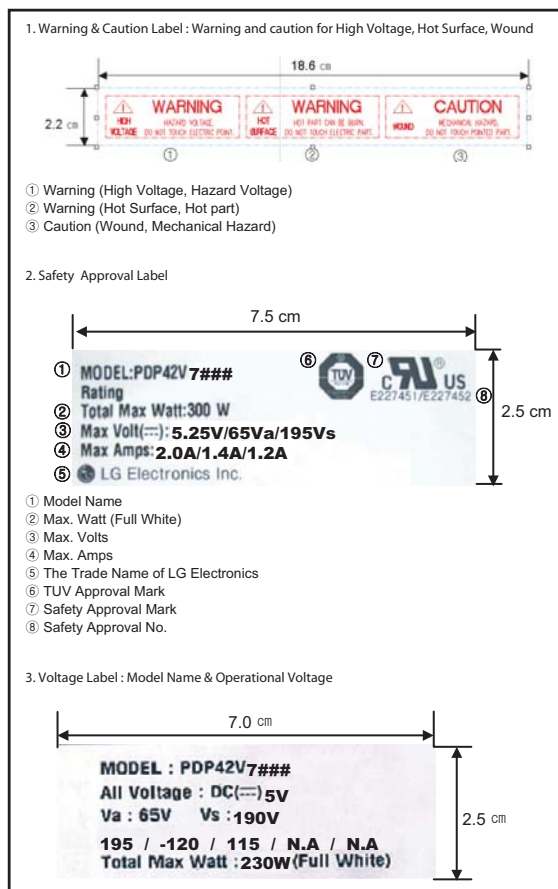
F_15590_110.eps
200306

Figure 4-2 Label location



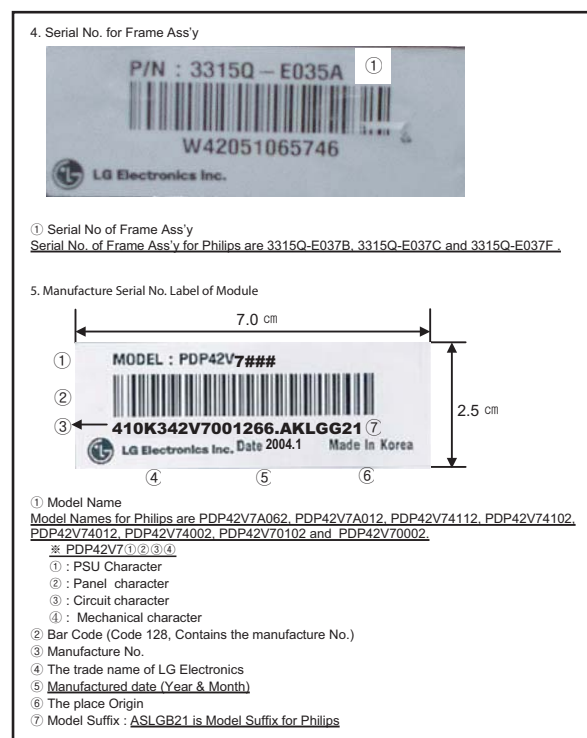
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070705

Figure 4-3 Label indication



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020806

Figure 4-4 Label information (1)



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080705

Figure 4-5 Label information (2)

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

- 5.1 Quick Module Check PDP42V7*
- 5.1.1 No Display
- 5.1.2 Bar Defect (Vertical)
- 5.1.3 Line Defect (Vertical)
- 5.1.4 Bar Defect (Horizontal)
- 5.1.5 Line Defect (Horizontal)
- 5.1.6 Mis-discharge Defect
- 5.2 Detailed Module Check PDP42V7*
- 5.2.1 No Display
- 5.2.2 Display Defects
- 5.2.3 Checking for Component Damage
- 5.3 Detailed PSU Check PDP42V7*
- 5.3.1 No Display

Notes:

- If it is not possible to repair the PDP by using the trouble-shooting and repair process described below, exchange the boards, mentioned in the service process "Exchanging boards" at the end of this chapter.
- If boards are exchanged, always re-align them, to make sure the PDP will perform correctly. This is also described in the service process "Exchanging boards" at the end of this chapter.

5.1 Quick Module Check PDP42V7*

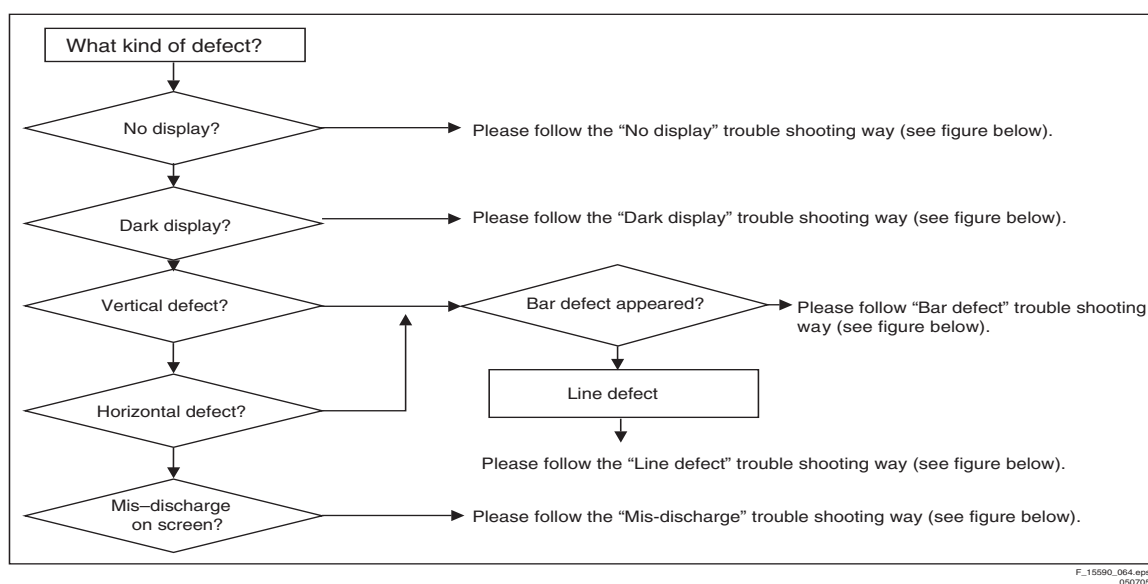


Figure 5-1 Logical judgement

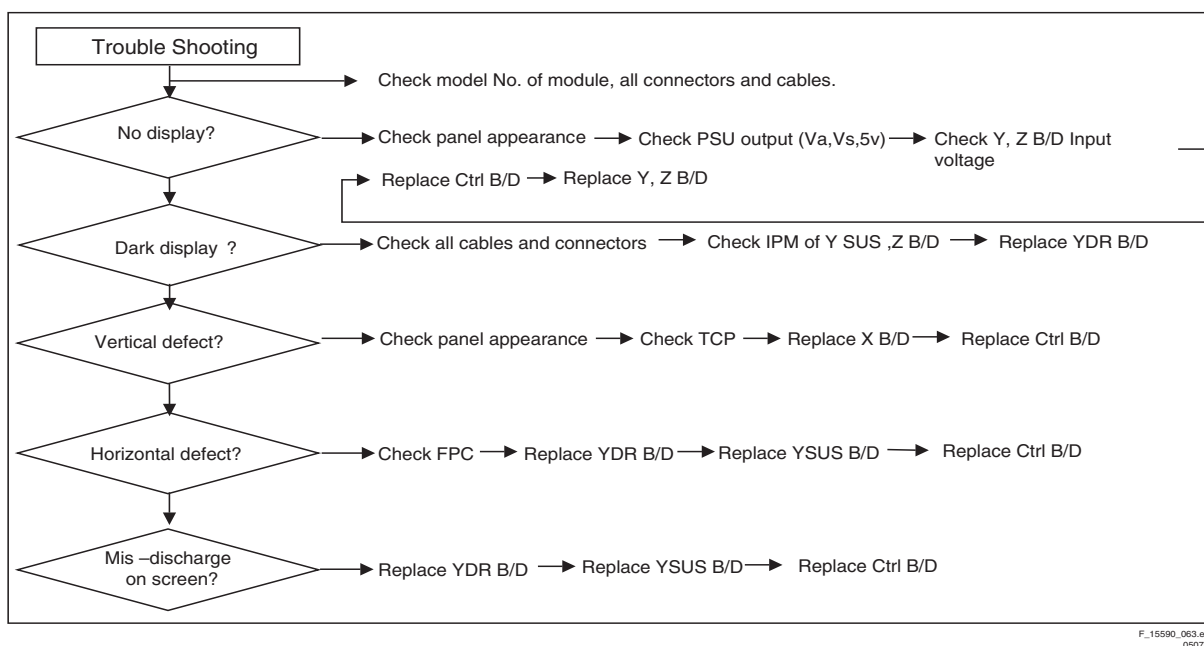


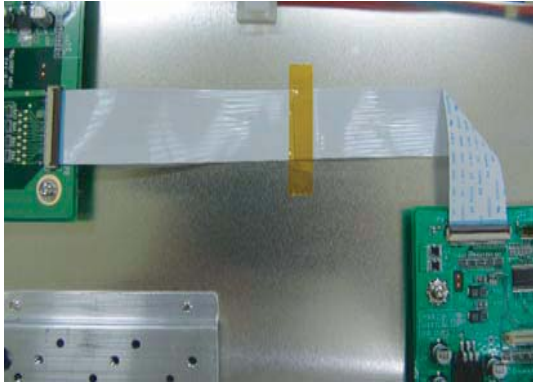
Figure 5-2 Quick check

5.1.1 No Display

Check each section with following method.
If there is a problem, replace or repair that part.
If it is not found, go to the next section.

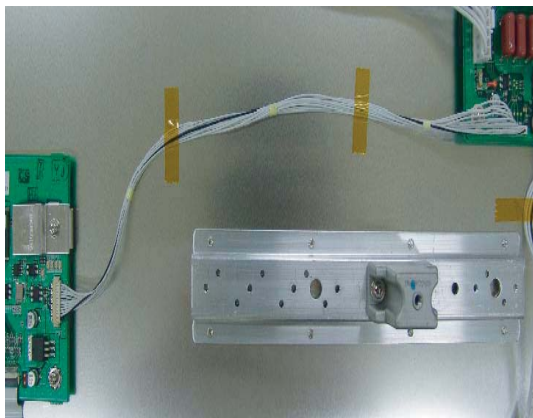
Connectors

Confirm all connectors (PSU, Y-SUS, CTRL, Z-SUS). The module may not function normally by misconnection (can not send signal and power). Also misconnection for a long time can have a specific board failed.



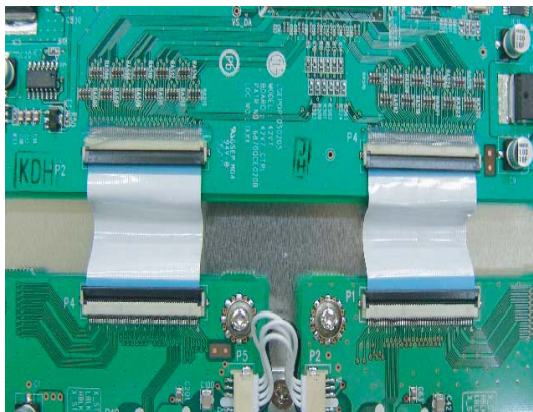
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Figure 5-3 Control + Y-SUS board



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290605

Figure 5-4 Control + Z-SUS board



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Figure 5-5 Control + X board



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Figure 5-6 Signal input (LVDS)

Exhaust Tip

Check the Exhausting Tip for cracks with the naked eye to check the vacuum state.

If there is a problem, replace the PDP module by a new one. In case of vacuum breakdown, the module makes a shaking noise because of inside gas ventilation.

There may be a small crack, which cannot be seen with the naked eye. This noise is different from capacitor noise.



NORMAL

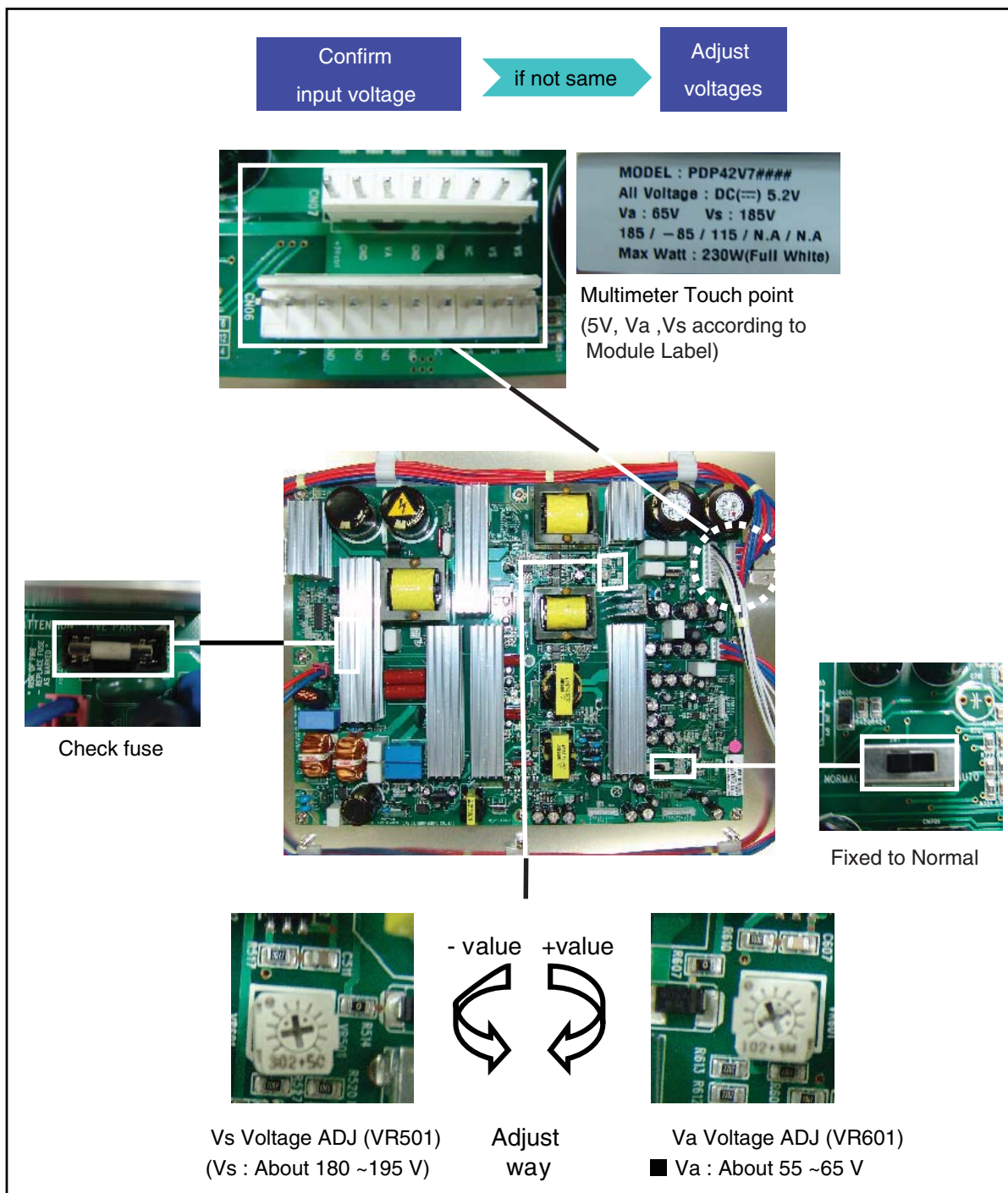
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Figure 5-7 Exhaust tip "normal"

PSU (see figure "PSU trouble shooting")

1. Check each unit part of PSU inside with naked eye (capacitor, FET, IC, resistor).
2. Check fuse and switch position (on "Normal").
3. Check output voltage, which is converted from AC to DC.
4. Voltage Check (5V, Va, Vs).

When PSU protection occurred: check for short between Y-SUS and Z-SUS board.



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120707

Figure 5-8 PSU trouble shooting

PSU Power Protection

There is a power protection when the power is switched "off" automatically within 2-3 min. from power "on". The power protection function protects the boards when a short occurs on circuits of the PDP module, or when a power problem occurs. If there is no power, even after replacing the PSU, find out where the short occurred.

In case of a PSU protection, the red LED will be "on" and an error code will be displayed via the green blinking LED (see also paragraph "Detailed PSU Trouble Shooting" further on). In case of a PSU protection, switch the service switch to "auto", disconnect the power supply connectors to the boards, to find if the boards are defective or the PSU itself.

Control Board (see figure "Control b/d trouble shooting")

1. Check LED status (normal status lightening or not)
2. If not, check OSC X1 output.
3. Check CTRL input voltage (connector P10).
4. Check each FET (3.3V, 5V, and 1.8V).

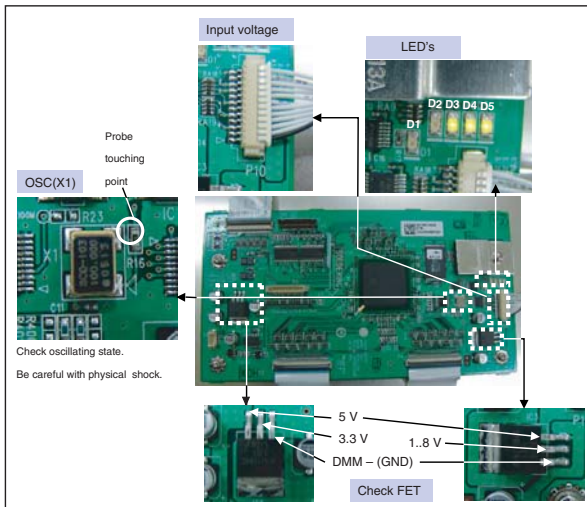
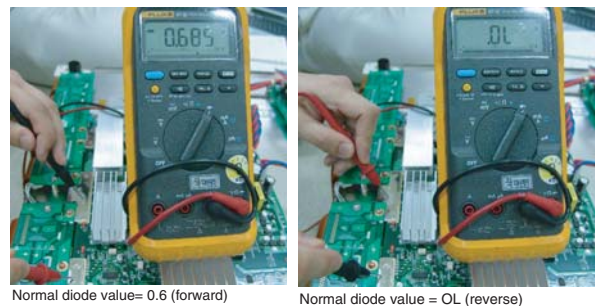


Figure 5-9 Control b/d trouble shooting

Y-SUS Board (see figure "Y-SUS b/d trouble shooting")

1. Check fuse: FS1 (5V), FS2 (Vs).
2. Check voltages (Vsetup, -Vy, and Vsc).
3. Check diode between GND and Y-SUS output.
4. Check whether output voltages agree with voltages on the label.



Normal diode value= 0.6 (forward)

Normal diode value = OL (reverse)

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Figure 5-10 Y-SUS board output diode check

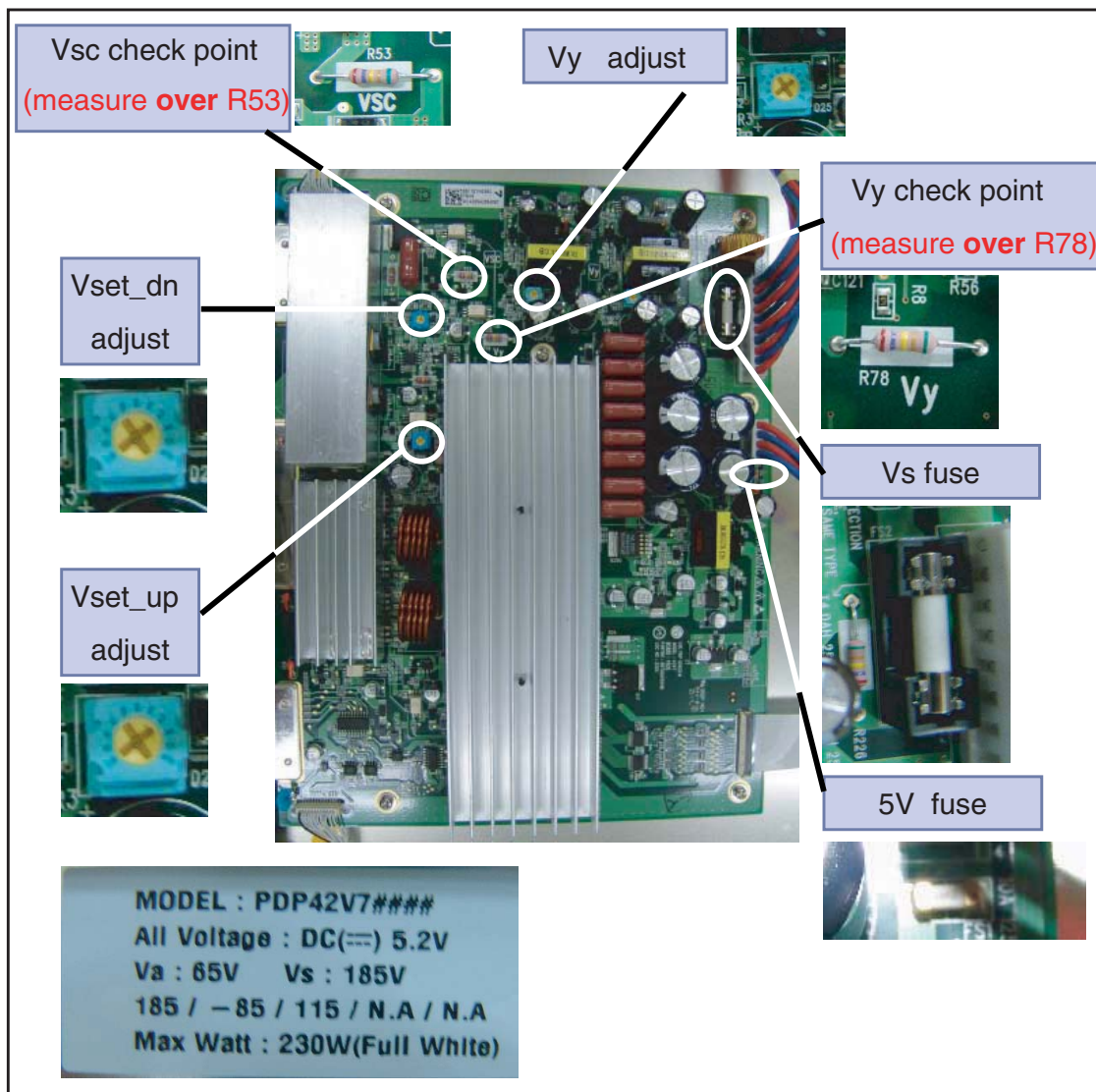
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060705

Figure 5-11 Y-SUS b/d trouble shooting

Z-SUS Board

1. Check the fuses.
2. Check input voltages (Va, 5V, and 15V)
3. Check FPC output diode value.

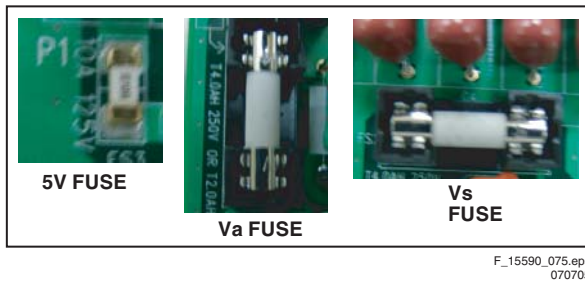


Figure 5-12 Z-SUS board fuse check

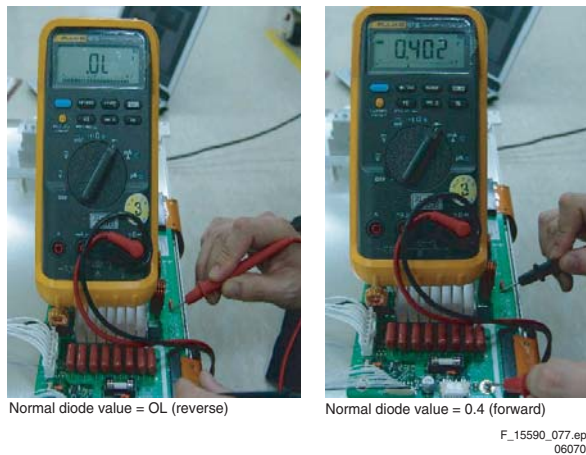


Figure 5-13 Z-SUS board FPC output diode check

5.1.2 Bar Defect (Vertical)

Check each section with following method. If there is a problem, replace or repair that part. If not go to the next section.

Connector

Check the TCP connector and cables. If not connected well, it will result in a bar defect and abnormal display behaviour.

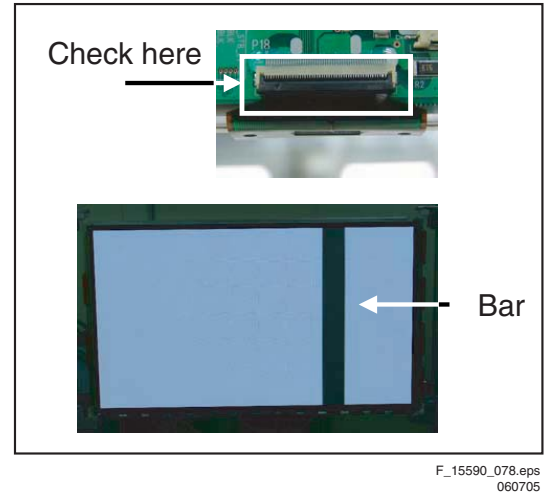


Figure 5-14 Connector check (1)

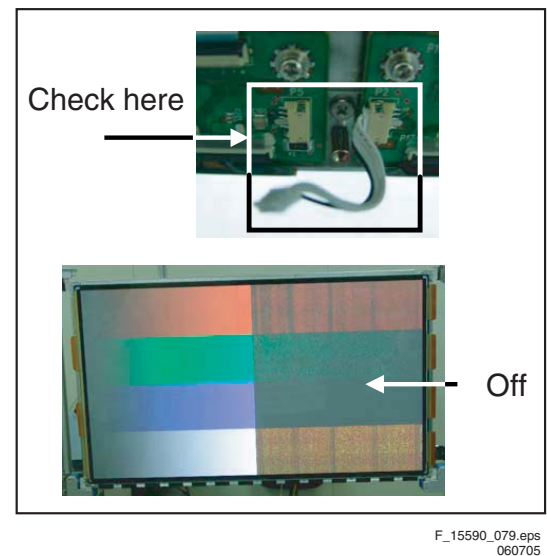


Figure 5-15 Connector check (2)

Checking TCP

Confirm whether the TCP was torn or chopping.

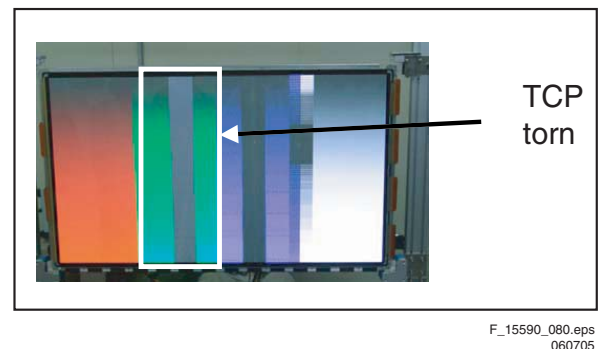


Figure 5-16 TCP torn

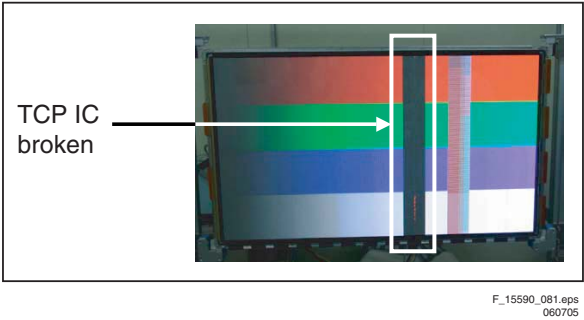


Figure 5-17 TCP IC broken

Control Board

The Control board supplies the video signal to the TCP. So, if there is a bar defect on screen, it may be a Control board problem.

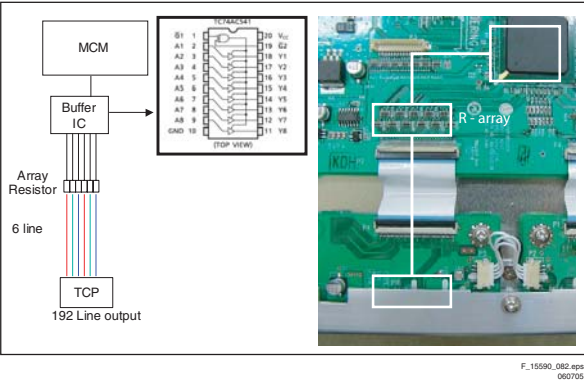


Figure 5-18 Control board address flow

5.1.3 Line Defect (Vertical)

In case of one line open or shorted, check dirt (foreign substances) in TCP connector. First, try to remove the dirt with compressed air. If, after this, the same line appears again, replace the panel.

Line Open or Short

This phenomenon is due to TCP IC inside short or electrode problem. In this case, replace the panel.

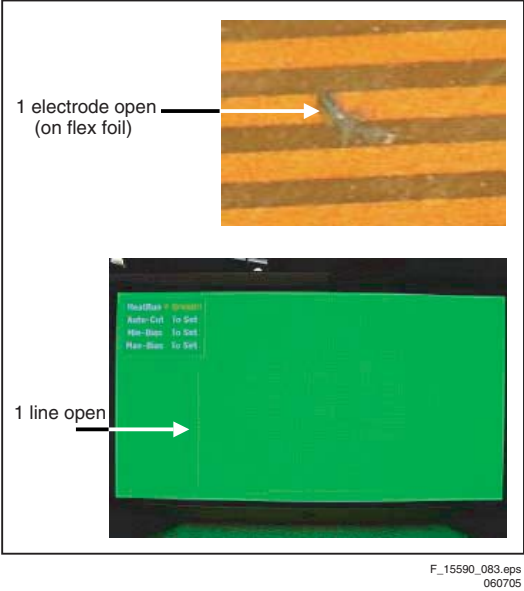


Figure 5-19 Single line defect

Line Open or Short with the Same Distance

This is MCM of Control board defect. The MCM cannot be replaced separately. So replace the Control board.

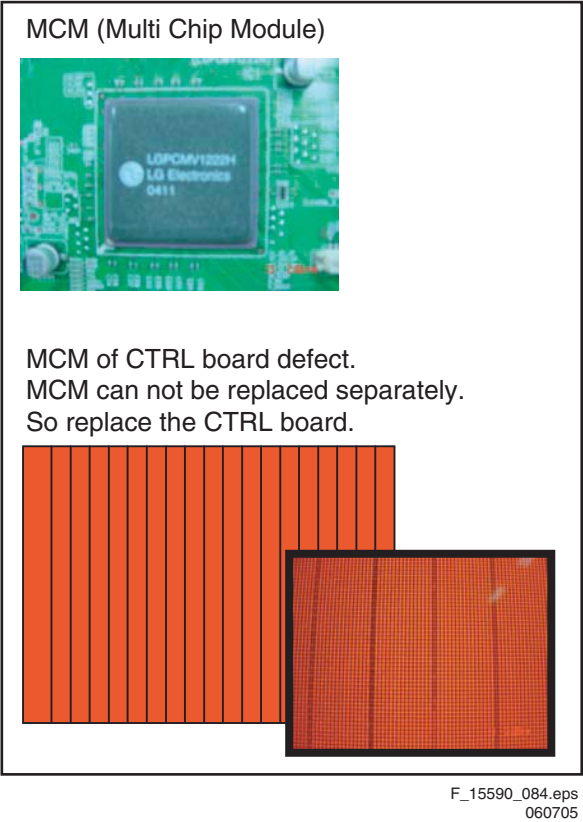


Figure 5-20 Evenly repeated lines

5.1.4 Bar Defect (Horizontal)

Most horizontal defects can be repaired. In case of adherence part of the film and rear panel electrode, or panel electrode open/short, replace the PDP panel.

Connector

If the connector on Y board and Z board are not plugged in well, it can result in a horizontal bar, because the sustain voltage cannot be supplied to panel. So check connectors FPC and Ydrv-Ydrv first.

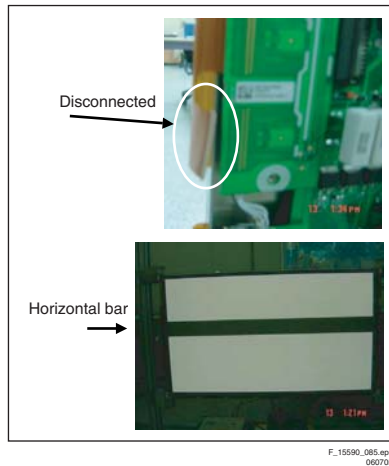


Figure 5-21 Check FPC connectors

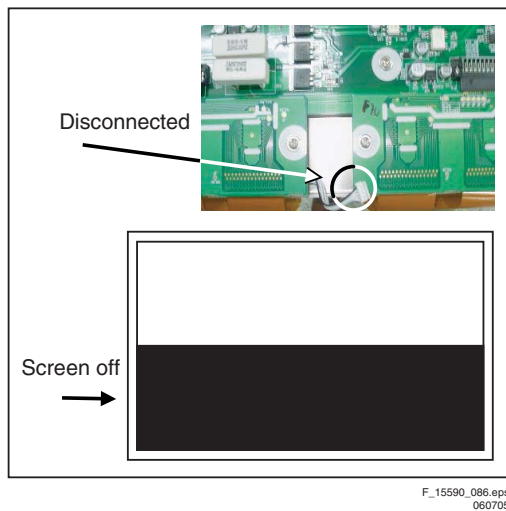
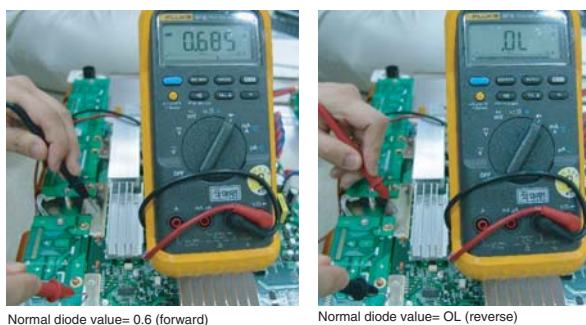


Figure 5-22 Check drive connectors

Scan IC Check

Check diode value of the right side part of the output pin.



Normal diode value= 0.6 (forward)

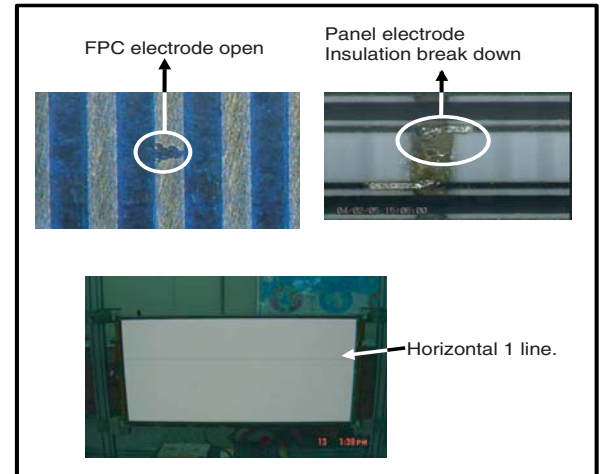
Normal diode value= OL (reverse)

Figure 5-23 Scan IC output diode check

5.1.5 Line Defect (Horizontal)

FPC Check

In case of one or more horizontal lines, this is probably due to FPC or panel inside the Control board. Y board is just normal.

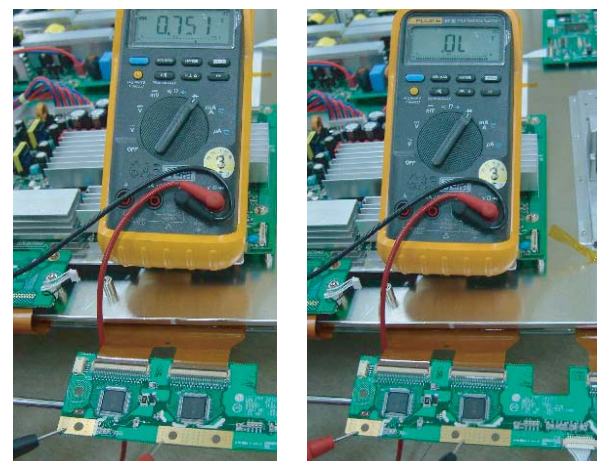


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Figure 5-24 Open FPC electrode / Panel electrode breakdown

Scan IC Check

Check diode value of the right side part of the output pin.



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Figure 5-25 Scan IC output diode check

5.1.6 Mis-discharge Defect

Most of mis-discharge appearance is a problem of Y-DRV, Y-SUS, or Z board.

Check these boards when mis-discharge occurs.

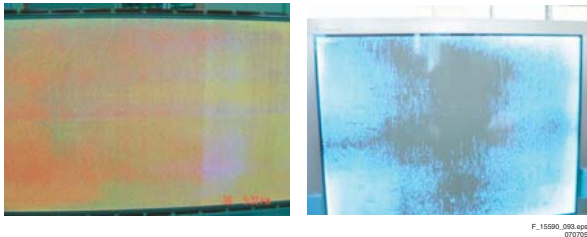


Figure 5-26 Mis-discharge

Checking Order

1. Check Y- and Z-SUS signal cable.
2. Check if Y-DRV IC is defective.
3. Check Y-SUS board voltages ($-V_y$, V_{scw})
4. Check if Y- and/or Z-SUS IPM are defective (see paragraph "How to Check IPM" below).
5. Replace Control board

How to Check IPM

Forward direction

Measure between:

- GND (+) and Sus-out (-).
- Sus-out (+) and V_s (-).

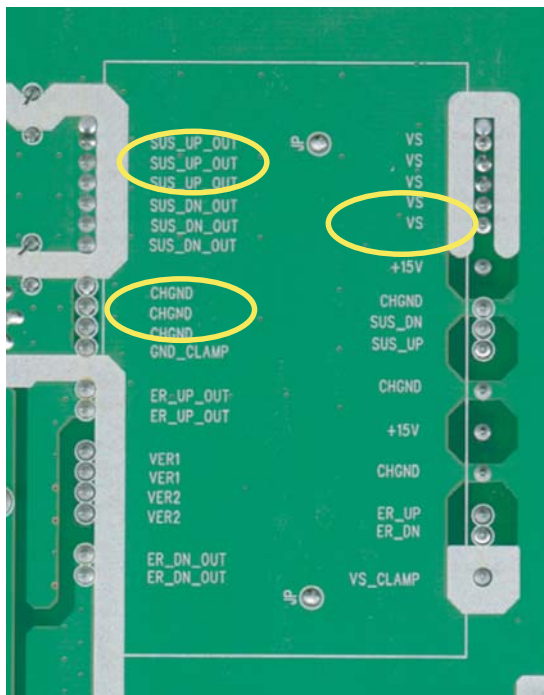
When each two test diode values is over 0.4V => OK.

Reverse direction

Measure between:

- GND (-) and Sus-out (+).
- Sus-out (-) and V_s (+).

When each 4 nodes test diode values is infinite => OK



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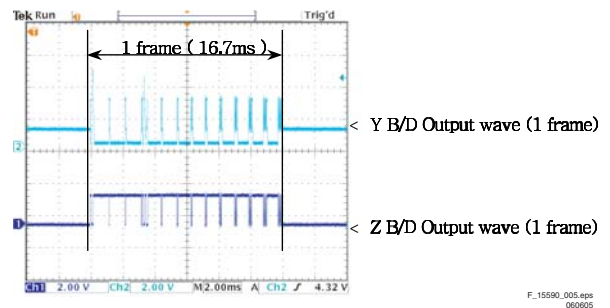
Figure 5-27 IPM check

5.2 Detailed Module Check PDP42V7*

5.2.1 No Display

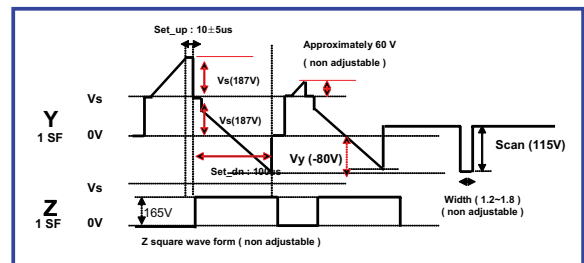
The Screen Does Not Display a Picture

1. Check whether on the CTRL board LED (D1, D2, D3, D4, and D5) is turned "on" or not.
2. Check the power and signal cable of the CTRL board.
3. Check if the X, Y, and Z boards are plugged in correctly.
4. Check the connection of the X, Y, and Z boards to the CTRL board.
5. Measure the output wave of X, Y, and Z boards with an oscilloscope (> 200 MHz) and find the trouble board by comparing the output wave with below figure.
 - Measure point for Y board: Bead B39.
 - Measure point for Z board: Bead B28.
 - Measure point for X board: P3.
6. Check the SCAN (Y side) IC.
7. Check the DATA (X side) TCP IC.
8. Replace the CTRL board.
9. Check if the fuse of Y and/or Z board is open and replace when open.
10. Check the input voltage ($V_{cc} = 5\text{ V}$, $V_a = 65\text{ V}$, $V_s = 187\text{ V}$).



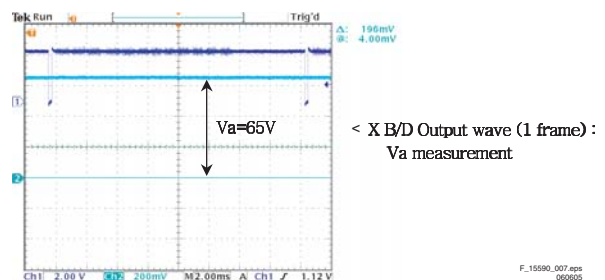
F_15590_005.eps
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Figure 5-28 Y and Z board output waveform (1 Frame)



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120707

Figure 5-29 Y and Z board output waveform (1 Sub Frame)



F_15590_007.eps
060605

Figure 5-30 X board output waveform (1 Frame)

5.2.2 Display Defects

All, or Half of the Screen is Not Shown

- In case the entire screen is not shown:
 - Confirm if the 8-pin connection of the X to Z board is plugged in correctly.
- In case half of the screen is not shown:
 - On the XR board:
 - Confirm if the 60-pin connection of the CTRL board to the XR board is plugged in correctly.
 - On the XL board:
 - Confirm if the 5-pin connection of the XR board to the XL board is plugged in correctly.
 - Confirm if the 60-pin connection of the CTRL board to the XL board is plugged in correctly.
 - Replace relevant X board.

Notes:

Relationship between Screen and X board:

Screen	X-board
Left half of the screen	Right X-board
Right half of the screen	Left X-board

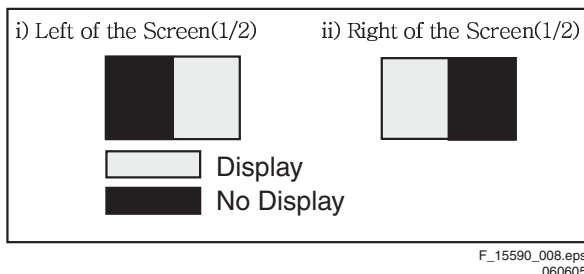


Figure 5-31 Screen display "1/2 display"

Vertical Parts of the Screen are Missing

- This can be related to a problem between Data TCP and X board.
- Confirm that the connector of the Data TCP is well connected to the X board (it corresponds to the part that screen that is not shown).
- Confirm whether the Data TCP is failed (inclusion examination with the naked eye of blown ICs or others).
 - If the IC failed: replace the module.
 - In case of X board shorting or open PWB pattern: when TCP IC is not defective, replace the X board.

Notes:

- Example of screen display (anyone of the 14 Data TCPs can be shown).

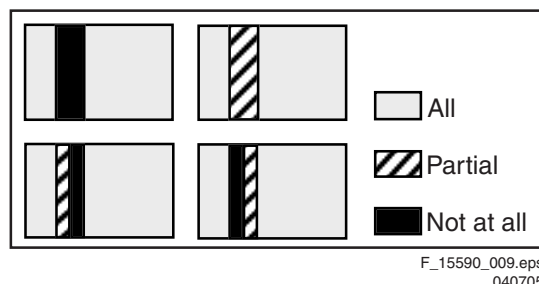


Figure 5-32 Screen display "Vertical parts missing"

- How to examine Data TCP IC
 - Change [1] "Va Power" into CATHOD, [2] "GND" into ANODE, and then examine the diode in forward or reverse direction.

- Examine with the naked eye traces of blown ICs [3] or others.

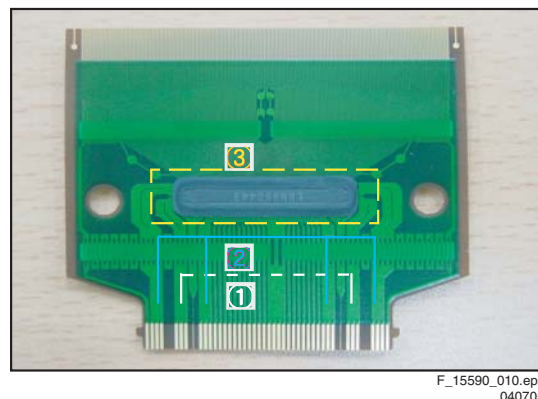


Figure 5-33 Data TCP IC examination

Unusual Pattern on Display

- In case of generating unusual pattern of Data TCP IC unit as shown in below picture, there is problem in the signal (CLK, data STB) or connector that is input of Data TCP IC.
- In case of "Case 1":
 - Confirm the connection between Data TCP connector and IC.
 - Replace the relevant X board.
- In case of "Case 2" or "Case 3":
 - Confirm the Data TCP connectors and the connection from CTRL to X board.
 - Check the CTRL board and X board.
 - Replace the relevant X board or CTRL board.
- In case of "Case 4" or "Case 5":
 - Check the connector from CTRL board to X board.
 - Replace the relevant X board or CTRL board.
 - Check the connection between Z and XR board (8-pin), and between XR and XL board (5-pin power connector).

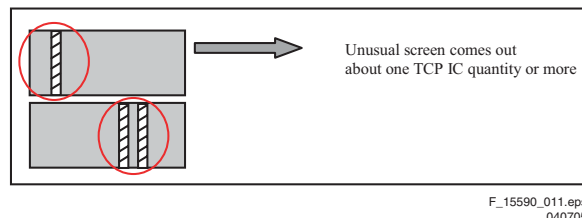


Figure 5-34 Case 1

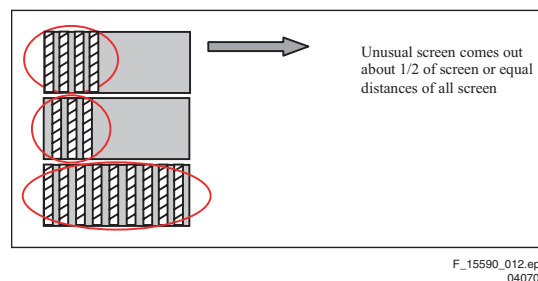


Figure 5-35 Case 2

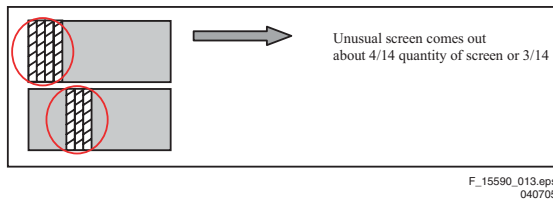


Figure 5-36 Case 3

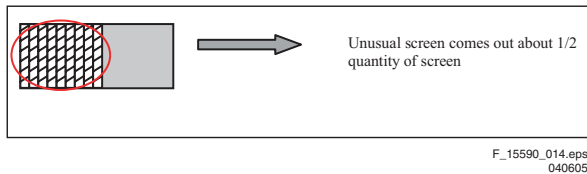


Figure 5-37 Case 4

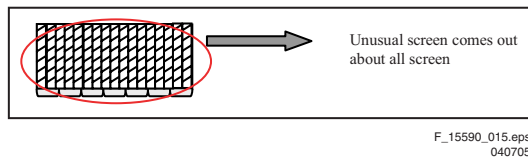


Figure 5-38 Case 5

Regular Stripe on Display

1. In case of the generation of regular vertical stripes around the location of one Data TCP IC (or more), check the connections.
2. Confirm if the connection of X board or CTRL board to X board correspond to unusual screen.
3. Replace the relevant X board or CTRL board.

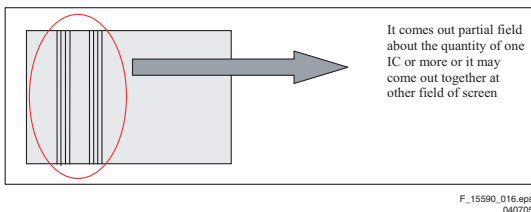


Figure 5-39 Screen display "Regular stripes"

Scan FPC Problem

1. Check the connection between Y DRV board and Scan FPC.
2. If the Scan IC is defective, replace the Y DRV board.



- The screen display is very good
 - The screen display is poor
- F_15590_017.eps
060605

Figure 5-40 Screen display "Scan FPC problem"

- Check method of the SCAN IC
 - Change the Vpp pin into ANODE and GND pin into CATHOD, and then test the diode in forward or reverse direction.



Figure 5-41 Scan IC

Vertical Line with Regular Gap (Vertical Stripe Flash at Special Colour)

- Replace the CTRL board.

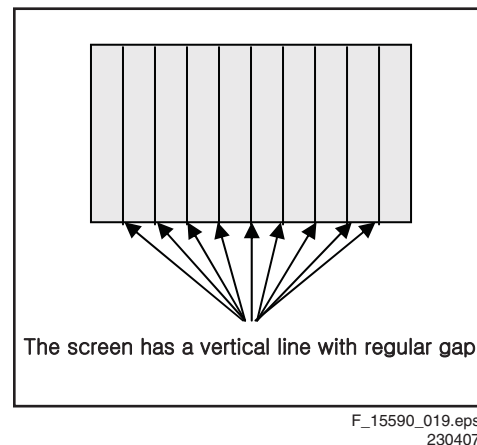


Figure 5-42 Screen display "Vertical lines with regular gap"

Data Copy into Vertical Direction

- Replace the Y-DRV board or Y board.

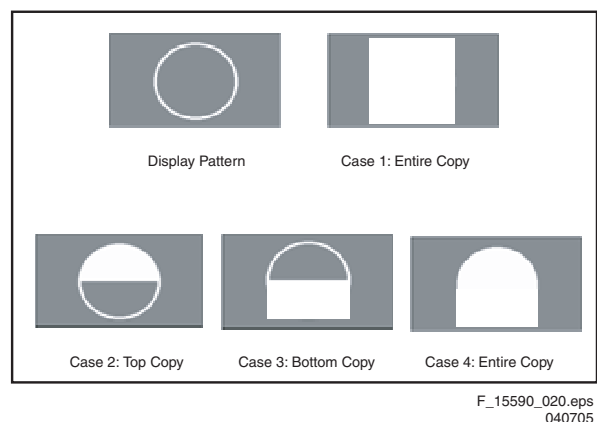


Figure 5-43 Screen display "Data copy in vertical direction"

One or Several Vertical Line(s) on the Screen

1. It may be caused by:
 - Open or short on DATA TCP FPC attached panel.
 - Defect on DATA TCP attached panel.
2. Replace Module.

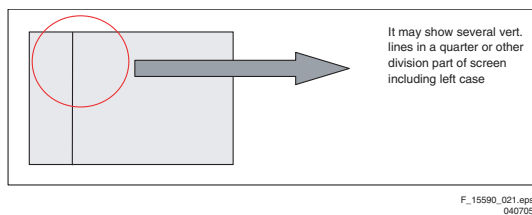


Figure 5-44 Screen display "Vertical lines"

One or Several Horizontal Lines on the Screen

1. It may be caused by:
 - Open or short on SCAN FPC attached panel.
 - Defect on SCAN IC attached panel.
2. Replace Y DRV board.

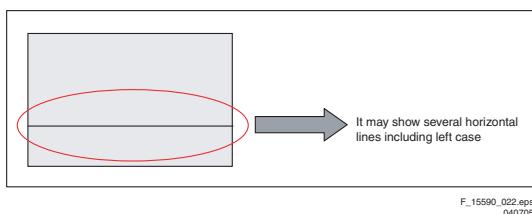


Figure 5-45 Screen display "Horizontal lines"

Low Brightness of Displayed Picture

1. In this case, Z board operation is not correct.
2. Check the power cord of Z board.
3. Check the connector of Z board and CTRL board.
4. Replace the CTRL board or Z board.

Partially Other Colour on Full White Screen or Partially Discharge on Full Black Screen.

1. Check the declination of Y board set-up and set-down wave.
2. Measure each output wave with oscilloscope (> 200 MHz) and compare the data with below figure data. Adjust the Y board Set_up (A) and Set_down (B) declination by changing VR1 and VR2 as written on the adjustment label.
 - Measuring Point of Y board: B39

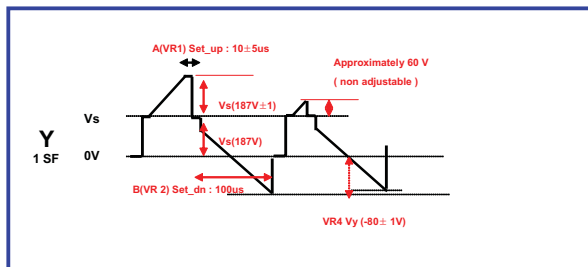


Figure 5-46 Y output voltage waveform

No Specified Brightness at Specified Colour

1. Check the connector of CTRL board input signal.
2. Replace the CTRL board.

5.2.3 Checking for Component Damage**Y IPM (IC 15) or Z IPM (IC 2)**

When the internal Sustain_IGBT or ER_FET of Y IPM (IC15) or Z IPM (IC2) is damaged, VS fuse is open and there will be no picture.

- Test Point: B32-GND (Y board), B28-GND (Z board).
- Wave format: B32 (Y board) or B28 (Z board) has no output wave.
- Measure position: Sustain section, B32 wave of Y board and B28 wave of Z board (full white pattern).

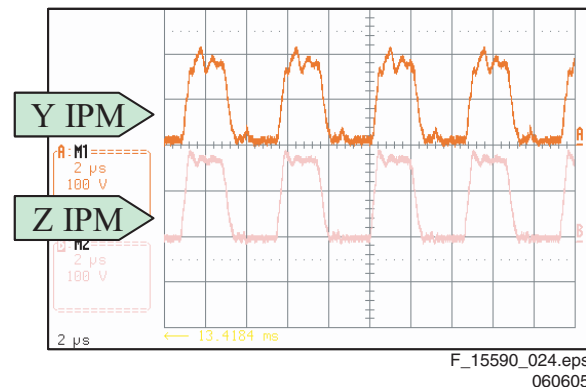


Figure 5-47 IPM normal output

Pass_Top FET (Y board: HS2)

When the Pass_Top FET is damaged, electric discharge of the entire screen is generated.

- Test Point: GND-B32 (Y board)
- Wave format: When the Set_dn does not descend until -Vy.

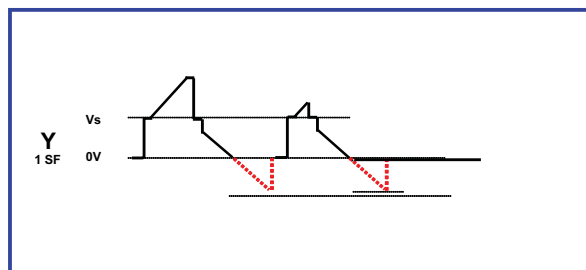


Figure 5-48 Pass-Top FET defective

FET Assy (Y board: HS1)

When Set_Up FET is damaged, there will be no picture.

1. Test Point: GND-B32 (Y board)
 - Wave format: Set_up waveform is not generated.
2. When Set_Down FET is damaged, electric discharge of entire screen is generated.
 - Test Point: GND-B32 (Y board)
 - Wave format: Set_down waveform is not generated.
 - Measure position: Reset wave of B32 (Y board) (full white pattern)

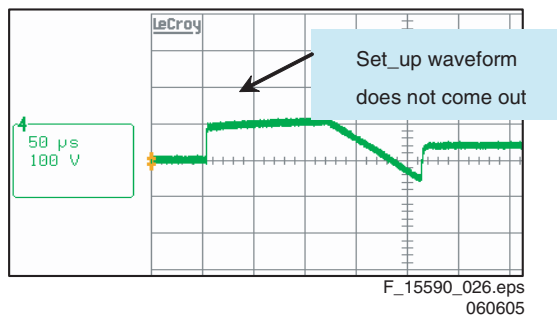


Figure 5-49 Set_Up FET defective

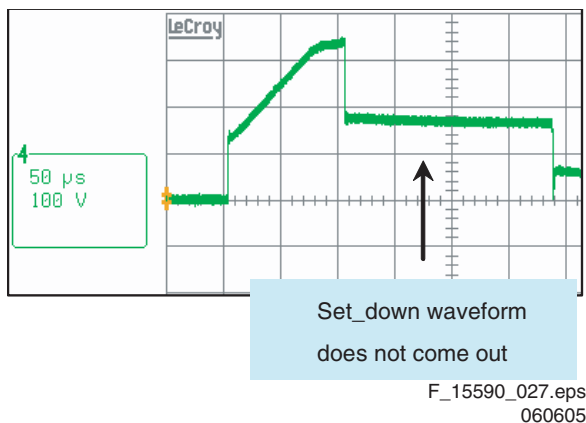


Figure 5-50 Set_Down FET defective

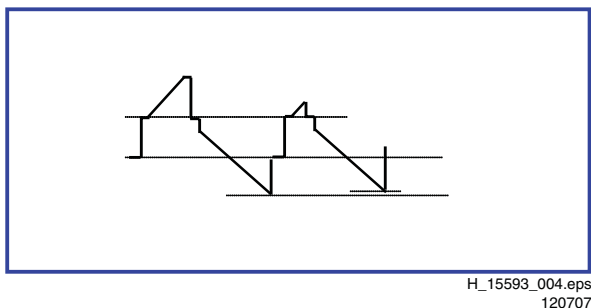


Figure 5-51 Reset section normal output

SCAN IC (Y-DRV board: IC1-8)

- In case of the SCAN IC is damaged, one horizontal line may be open on the screen.
 - Test Point: ICT measurement of GND-Y DRV board output.
 - Wave format: As shown below figure.
- When the SCAN IC is damaged (poor, external electricity, or spark), there might be no picture.
 - Test Point: ICT measurement of GND-Y DRV board output
 - Wave format: Output wave format is not generated (you can see if Y DRV board Top or Bottom's SCAN IC is damaged).
- Screen shaken horizontally when Y DRV board Top and Bottom cable is damaged.
 - Test Point: ICT measurement of GND-Y DRV board output.
 - Wave format: As shown in figure "Y DRV board Top and Bottom cable damaged".
- Overlap of two horizontal lines on the screen in case of shorted SCAN IC output.

- Test Point: ICT measurement of GND-Y DRV board output.
- Wave format: As shown in figures "SCAN IC shorted output" and "SCAN IC normal output".
- Measurement point: SCAN section, output ICT of Y DRV board (full white pattern).

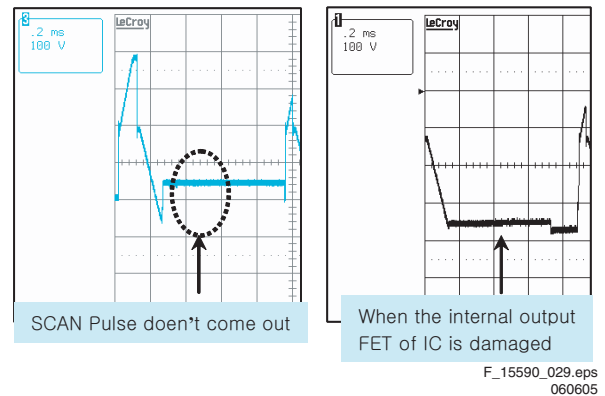


Figure 5-52 SCAN IC defective

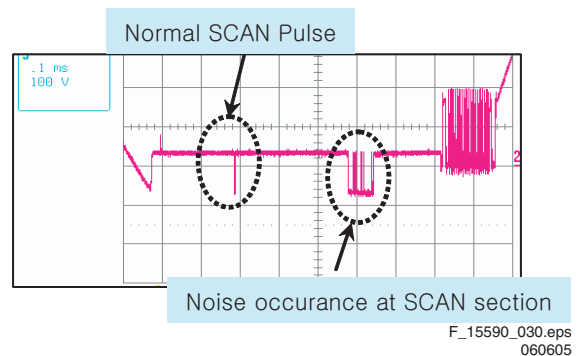


Figure 5-53 Y DRV board Top and Bottom cable damaged

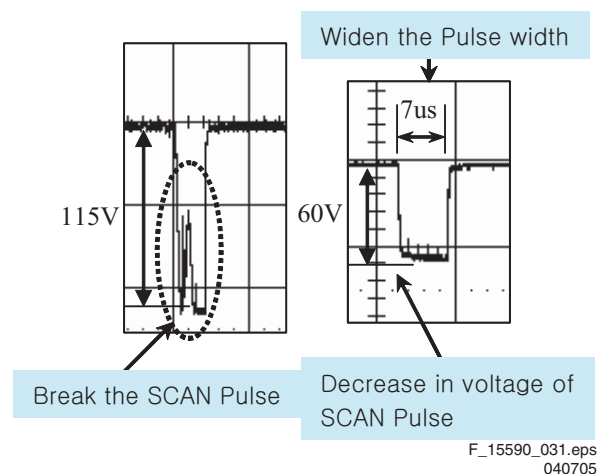


Figure 5-54 SCAN IC shorted output

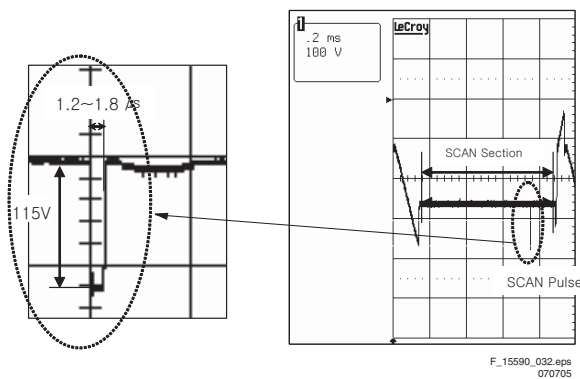


Figure 5-55 SCAN IC normal output

TCPs

1. In case of shorting or opening of TCP IC output, it may show one or several vertical lines.
 - Test Point: Output TP of GND-TCP
 - Wave format: As shown in figure below. In case of normal wave output, when STB signal is generated, the output must maintain "high". When STB signal is generated again, the output must fall to "low". But when the TCP IC is damaged, the STB signal is not generated, and the output falls to "low".
2. In case of a damaged TCP IC or power resistance, the screen is not shown or discharges partially.
 - Test Point: Output TP of GND-TCP
 - Wave format: Output wave is not generated.

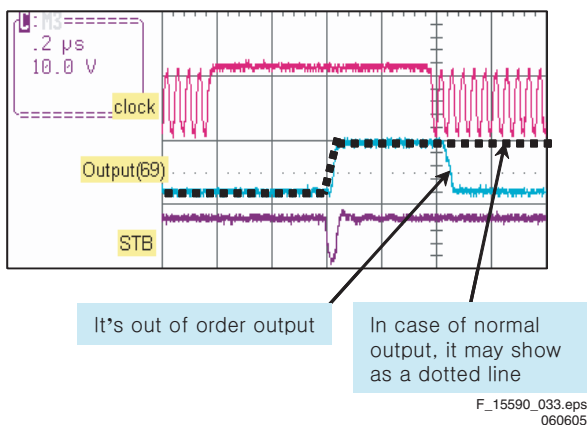


Figure 5-56 COF IC output defective

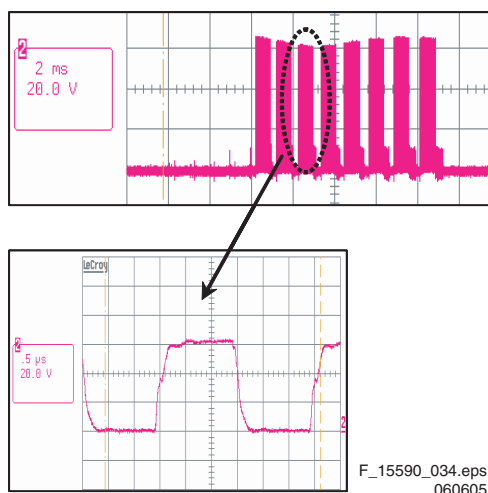


Figure 5-57 TCP normal output

Crystal (CTRL board: X1)

1. When a crystal is damaged, the screen is not shown.
 - Test Point: Measuring 3-pin of GND-Crystal (CTRL board: X1).
 - Wave format: Output wave is not generated.
2. In case of unusual start-up of the crystal, the screen may blink.
 - Wave format: As shown in figure below.
 - Measurement position: Measuring output 3-pin of crystal (X1: 100 MHz) on CTRL board (full white pattern).

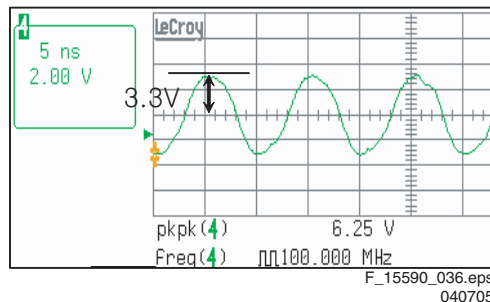


Figure 5-58 Crystal normal output

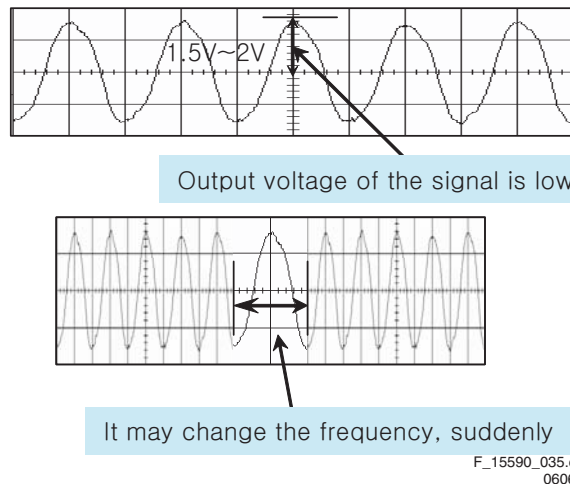


Figure 5-59 Crystal defective output

5.3 Detailed PSU Check PDP42V7*

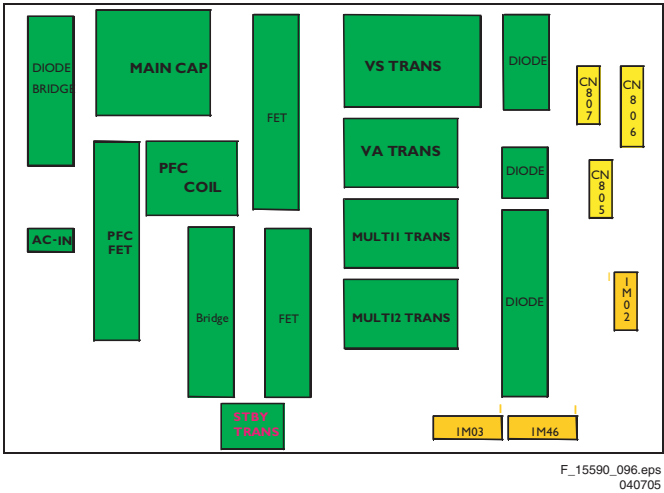


Figure 5-60 PSU top view

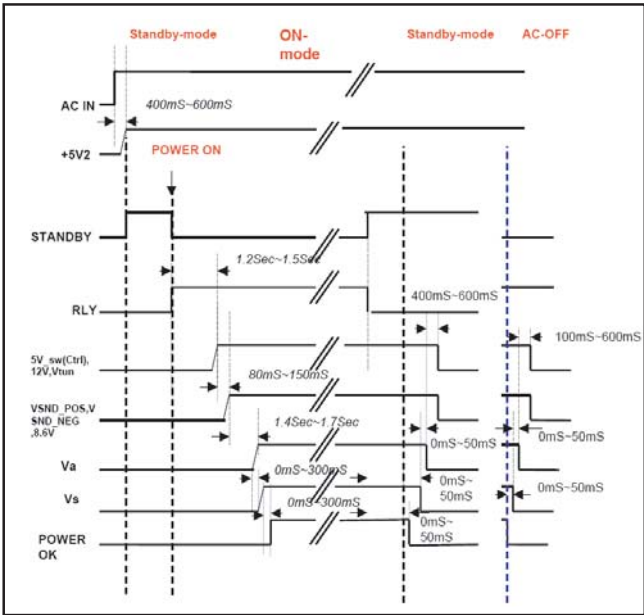


Figure 5-62 PSU "on/off" sequence in "Normal" mode

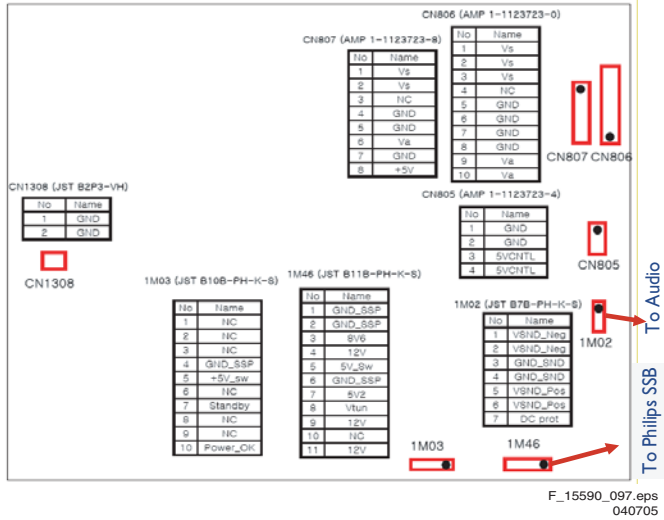


Figure 5-61 PSU Connector I/O pin assignment

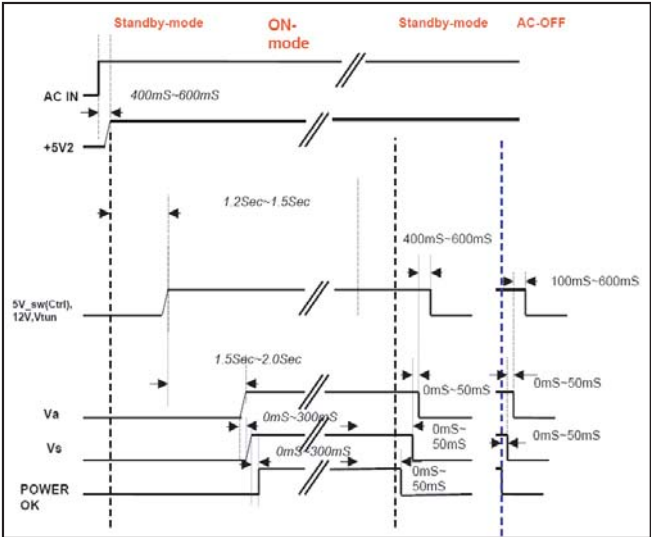


Figure 5-63 PSU "on/off" sequence in "Auto" mode

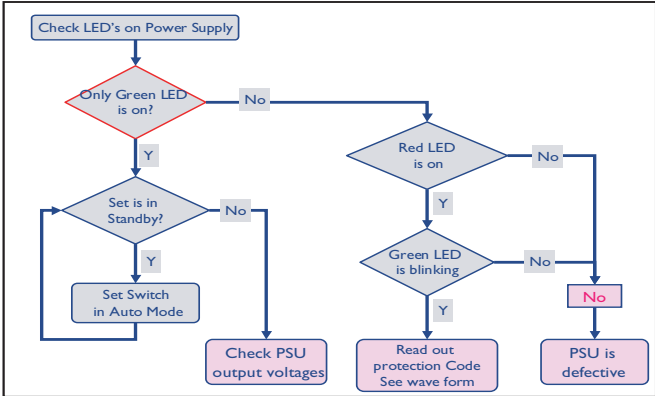


Figure 5-64 PSU Fault finding tree

5.3.1 No Display

1. Check whether the LED1 of the PSU is turned "on" or not.
2. Check the power and signal cables of the PSU.
3. Check the connection of the X board, Y board, and Z board to the Control board.
4. Replace the PSU
5. Check the output voltages of the PSU ($V_{cc}=5V$, $V_a=65V$, $V_s=187V$).
6. When 5V2 is not present, check whether the fuse is shorted or opened in AUTO/NORMAL mode.
7. When the PSU is in protection mode, check waveform and count of LED1 as shown in the figures below.

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
Continuous flicker	LED OFF → LED ON →	LED OFF → LED ON →

*Time period : LED ON/OFF repeat an interval 200ms

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Figure 5-65 DC-port signal (1M02) protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
2	LED OFF → LED ON →	LED OFF → LED ON →

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040705

Figure 5-66 Vs output protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
3		LED OFF → LED ON →

F_15590_103.eps
040705

Figure 5-67 Va output protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
4		

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040705

Figure 5-68 5V output circuit protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
5		

F_15590_105.eps
040705

Figure 5-69 12V and V_{tun} circuit protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
6		

F_15590_106.eps
040705

Figure 5-70 +18V circuit protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
7		

F_15590_107.eps
040705

Figure 5-71 +8V6 circuit protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
8		

F_15590_108.eps
040705

Figure 5-72 -18V circuit protection

LED Count	OCP [Over Current Protection]	OVP [Over Voltage Protection]
9		

F_15590_109.eps
040705

Figure 5-73 PFC circuit protection

5.4 Exchanging of Boards

5.4.1 Service Process

If the PDP gives no picture, or if there is panel mal-discharge, first try the Quick Module Check and all the other repair procedures at the beginning of this chapter. However, if it is not possible to repair and/or re-align the PDP via the procedures described earlier, various boards will have to be exchanged (see the three steps below). Which of the boards will have to be exchanged, depends on the PDP model.

Important: If boards are exchanged, it is always necessary to re-align the PDP ! See Chapter 8, Alignment.

1. On PDP models **PDP42V7A062.ASLGB**, **PDP42V7A062.ASPHB**, and **PDP42V7A462.ASPHB**, exchange the following boards: Y-SUS, Z-SUS, CTRL, XRLT, and XRRT.
Use the following replacement kits:
 - 9965 000 38493 (Y-SUS, Z-SUS, CTRL).
 - 9965 000 32365 (XRLT).
 - 9965 000 32366 (XRRT).
2. On PDP model **PDP42V7K462.ASPHB** exchange the following boards: Y-SUS, Z-SUS, CTRL.
Use the following replacement kit:
 - 9965 000 38493 (Y-SUS, Z-SUS, CTRL).
3. Attach the new voltage label from the kit to the PDP, close to the old voltage label, and cross out the -Vy value on the old label.
4. Check the -Vy and Vz_b voltages of the PDP, to see if they correspond to the values on the new label (see Chapter 8, Alignment).

Any other adjustments (like V_{sc}, V_{setup} and V_{setdown}) must also be carried out (see Chapter 8, Alignment).

5.5 Defect Description Form

This form must be used by the workshops for warranty claims:

Defect Description Form LCD PLASMA v4.0 final					Date last modified: 28/03/2006	
To be filled in by <u>WORKSHOP / WORK CENTER</u>						
Country:		PHILIPS LCD & Plasma <u>DEFECT DESCRIPTION</u> <u>FORM</u>		Type nr./Model nr. set		
Customer Account nr.:				Serial nr. set		
Job sheet nr.:				Type nr. display		
				Serial nr. display		
				Part nr display (12nc)		
				Return number		
GENERAL REPAIR DATA	Condition	<input type="checkbox"/> Constantly <input type="checkbox"/> Intermittently <input type="checkbox"/> After a while			<input type="checkbox"/> In hot environment <input type="checkbox"/> In cold environment Other: <div style="border: 1px solid black; height: 20px; width: 100%; margin-top: 5px;"></div>	
	Symptom(s)	<input type="checkbox"/> No backlight <input type="checkbox"/> No picture <input type="checkbox"/> Picture too bright <input type="checkbox"/> Scratches (LCD only acc. Pixel criteria sheet V4.0) <input type="checkbox"/> Only partial picture <input type="checkbox"/> Unstable picture			<input type="checkbox"/> Flickering / flashing picture <input type="checkbox"/> Lines across/down image <input type="checkbox"/> Inactive row(s) <input type="checkbox"/> Inactive column(s) <input type="checkbox"/> Missing colour(s) <input type="checkbox"/> Light leakage Other: <div style="border: 1px solid black; height: 80px; width: 100%; margin-top: 5px;"></div>	
PANEL REPAIR	Pixel Defect(s):	Dark dots Bright dots	<u>Qty of dots:</u>	Mark Defect(s):		
	Symptoms <u>Out of warranty</u>	Following defect symptoms are out of warranty: <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> - Broken glass / Broken polarizer - Scratch(es) on display / polarizer </div> <div style="width: 45%;"> - Number of dark/bright pixels within spec. - Burn in (Plasma TV) / Sticking image (LCD TV) - MURA </div> </div>				These symptoms are not claimable.
BOARD REPAIR	Defect Board			New Board		
	Spare Part Nr.	Serial Nr.		Spare Part Nr.	Serial Nr.	
	1.					
	2.					
	3.					
	4.					
<p>Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected.</p> <p style="text-align: right;">DE10WEG</p> <p>Owner: PHILIPS CE EUROSERVICE</p>						

Figure 5-74 Defect Description Form (DDF)

6. Block Diagrams, Test Point Overviews, and Waveforms

Not applicable

7. Circuit Diagrams and PWB Layouts

Not applicable

8. Alignments

Index of this chapter:

8.1 General

8.2 Alignment PDP42V7*

8.1 General

Notes:

- Important:** if the PSU board, the Y-SUS board or the Z-SUS board is replaced, the technician should check if the voltages delivered by these boards are correct. If not, the boards should be re-aligned in order to avoid bad performance of the PDP.
- Allow the set to warm up according conditions below for at least 10 minutes before adjusting.
 - Service signal: 100% Full White.
 - Service DC voltage: $V_{cc}= 5\text{ V}$, $V_a= 65\text{ V}$, $V_s= 187\text{ V}$.
 - DC/DC Pack voltage: $V_{sc}= 115\text{ V}$, $-V_y= -85\text{ V}$
 - Preliminaries environment: Temp ($25 \pm 5\text{ deg. C}$), Relative Humidity ($65 \pm 10\%$).
- Module adjustment should follow below sequence.
 - First, set up the $V_{sc} / -V_y$ voltage ($V_{sc}= 115\text{ V}$, $-V_y= -85\text{ V}$).
 - Then, adjust the voltage waveform (refer to adjustment).

Caution: Do not leave a still image for more than 10 minutes (especially The Digital pattern or Cross Hatch Pattern which has clear gradation) on the display, because this will cause burn-in effects.

8.2 Alignment PDP42V7*

8.2.1 Connection Diagram and Set-Up

- For the connection diagram of the measuring instrument, refer to Fig. "Measuring equipment connection diagram".
- Set-up the initial voltage (voltage label) $V_{cc}= 5\text{ V}$, $V_a= 65\text{ V}$, $V_s= 187\text{ V}$. Note that the initial set-up voltage can be changed according to the module's characteristic.

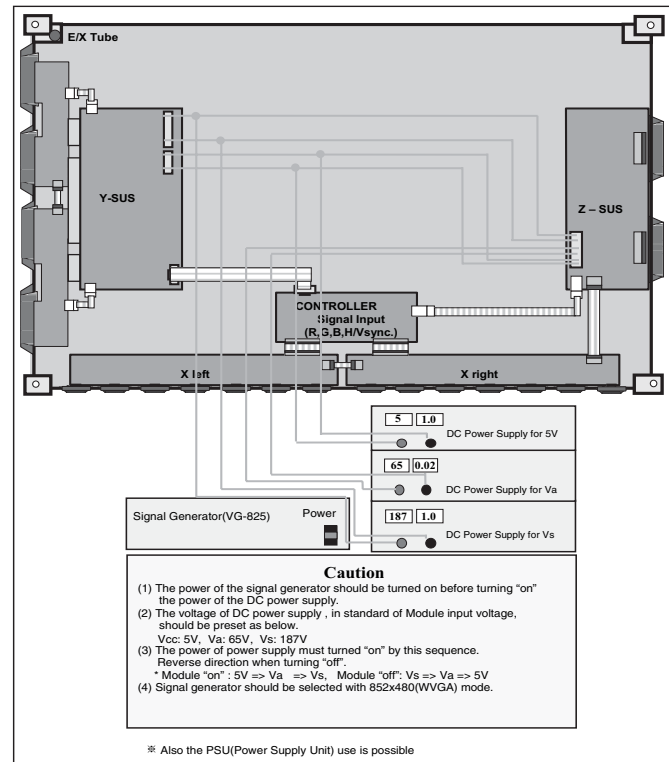


Figure 8-1 Measuring equipment connection diagram

8.2.2 Tools

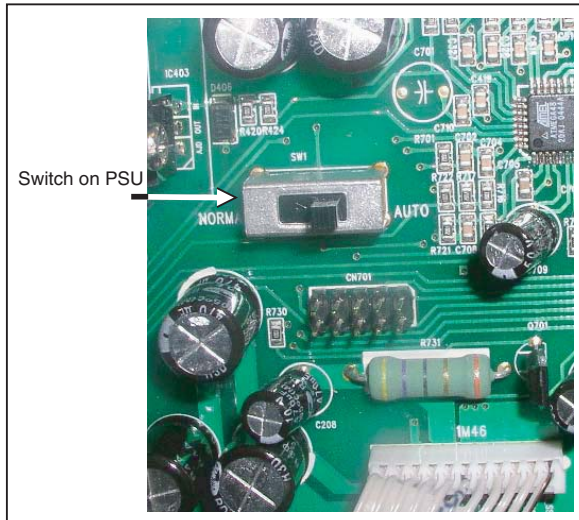
- Digital oscilloscope: $> 200\text{ MHz}$.
- DVM (Digital Multimeter): Fluke 87 or similar.
- Signal generator: VG-825 or similar.
- DC power supply or PSU:
 - DC power supply for V_s (1): $0 - 200\text{ V}$, $> 10\text{ A}$.
 - DC power supply for V_a (1): $0 - 100\text{ V}$, $> 5\text{ A}$.
 - DC power supply for 5 V (1): $0 - 10\text{ V}$, $> 10\text{ A}$.
 - DC/DC converter jig (1): The jig with an equivalent voltage output of PDP42V7#### module after taking the V_s , V_a , and 5 V voltage.
 - Voltage stability of power supply: Within $\pm 1\%$ for V_s and V_a , within $\pm 3\%$ for 5 V .

8.2.3 Alignments

Vs Alignment on PSU

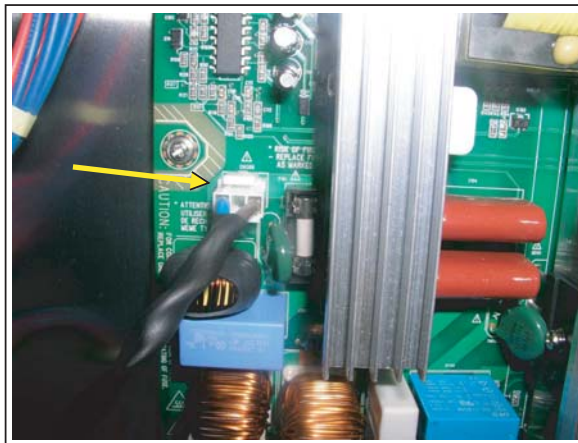
This describes the Vs alignment on the PSU:

1. Set the switch on the PSU to "AUTO", see Figure "Switch setting".
2. Connect Mains/AC Power (from Mains Filter) to the PSU board (CN1308), see Figure "Connect Mains".
3. Connect a multimeter between CN06-Vs and ground (e.g. frame), see Figure "Vs & Va measure and alignment points".
4. Align Vs with the upper potmeter on the PSU (VR501) to:
 - 184 V for the PDP42V7A062 and PDP42V7K062 models (different from label !).
 - 187 V for the other V7 models (as printed on label).
5. Set the switch on the PSU back to "NORMAL".



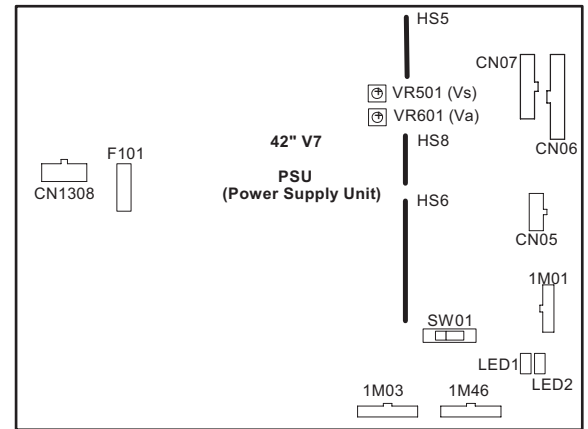
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120705

Figure 8-2 Switch setting (Vs & Va alignment step 1)



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120705

Figure 8-3 Connect Mains (Vs & Va alignment step 2)



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120707

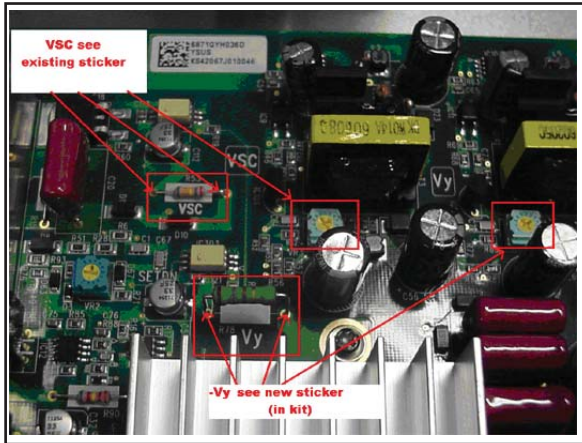
Figure 8-4 Vs & Va measure and alignment points (step 3 &4)

Va Alignment on PSU

This describes the Va alignment on the PSU:

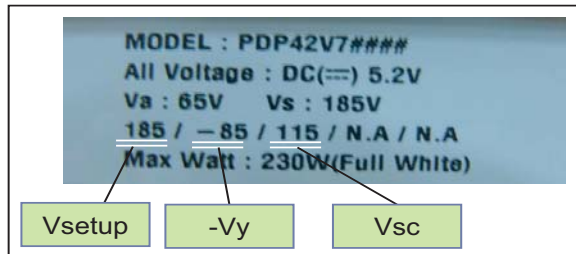
1. Set the switch on the PSU to "AUTO", see Figure "Switch setting".
2. Connect Mains/AC Power (from Mains Filter) to the PSU board (CN1308), see Figure "Connect Mains".
3. Connect a multimeter between CN06-Va and ground (e.g. frame), see Figure "Vs & Va measure and alignment points".
4. Align Va with the lower potmeter (VR601) to the value indicated on the PSU label.
5. Set the switch on the PSU back to "NORMAL".

Vscan Voltage Alignment on Y-SUS board



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120707

Figure 8-5 Vsc & Vy measuring and adjustment on Y-SUS board



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Figure 8-6 Existing Voltage label (on rear side of PDP module)



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120707

Figure 8-7 New Voltage label from replacement kit

This describes the Vsc (Vscan) alignment on the Y-SUS board:

1. Convert the signal of the signal generator to a 100% Full White signal, or use the internal test pattern.
2. Measure the Vscan voltage (115 ± 1 V) across R53 on the Y-SUS board, see Figure "Vsc & Vy measuring and adjustment on the Y-SUS board".
3. Align Vscan to the value indicated on the existing voltage label (see Figure "Existing voltage label") with potentiometer "Vsc" on the Y-SUS board.

Vy Voltage Alignment on Y-SUS board

This describes the Vy alignment on the Y-SUS board:

1. Convert the signal of the signal generator to a 100% Full White signal, or use the internal test pattern.
2. Measure the Vy voltage (-85 ± 1 V or, if the Y-SUS board has been replaced: -80 ± 1 V) across R78 on the Y-SUS board, see Figure "Vsc & Vy measuring and adjustment on the Y-SUS board".
3. Align Vy to the value indicated on the existing label (if the Y-SUS board has not been replaced) or to the value indicated on the **new** voltage label from the replacement kit (if the Y-SUS board has been replaced) with potentiometer "Vy" on the Y-SUS board (see Figure "New voltage label from replacement kit").

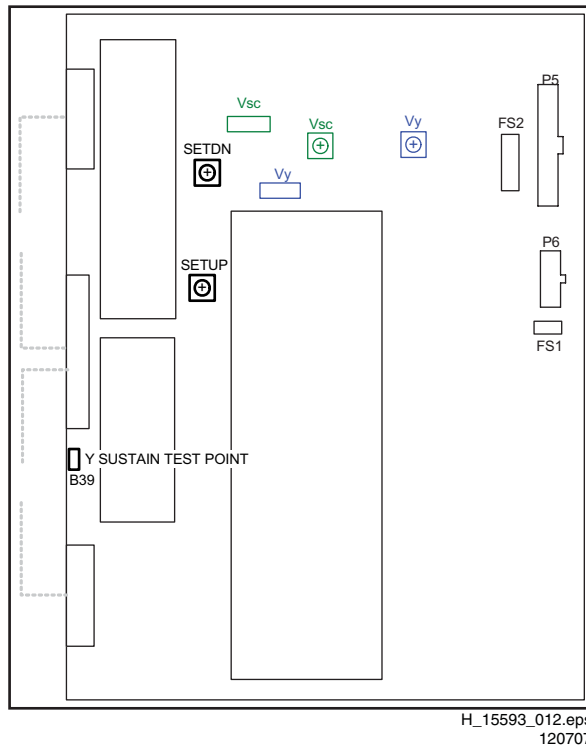
Vset-up Alignment on Y-SUS board

Figure 8-8 Vsetup & Vsetdown alignment on Y-SUS board

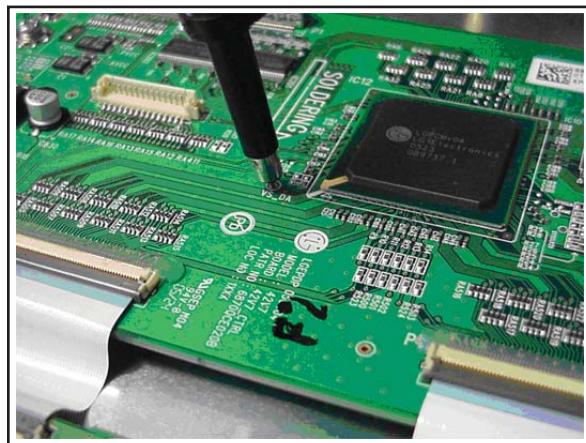


Figure 8-9 VS-DA trigger point on Control board

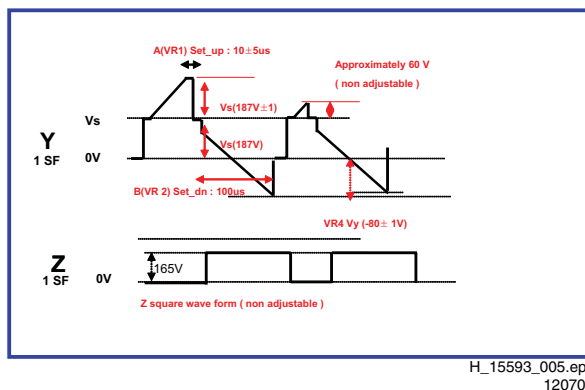


Figure 8-10 Y, Z set-up waveform

Note:

When aligning the PDP, use a grey pattern generator, set to 10 grey steps.

Adjusting Vset-up voltage wave form:

1. Connect the measuring instruments according to Figure "Measuring equipment connection diagram" at the beginning of this chapter.
2. Turn on the measuring instruments with "Caution" of Figure "Measuring equipment connection diagram".
3. Connect the oscilloscope measuring probe to test point B39 (Bead) of Y-SUS board bottom and GND (for the location of B39, see Figure "Vsetup & Vsetdown alignment on Y-SUS board").
4. Connect the oscilloscope triggering probe to trigger point VS-DA on the Control board (see Figure "VS-DA trigger point on Control board").
5. Turn potentiometer SETUP/VR1 on the Y-SUS board, and make the "A" waveform according to Fig. "Y, Z set-up waveform" to be $10 \pm 2 \mu s$.

Vset-down Alignment on Y-SUS board**Adjusting Vset-down voltage wave form:**

1. Turn potentiometer SETDOWN/VR2 on the Y-SUS board and make the "B" waveform according to Fig. "Y, Z set-up waveform" to be $100 \pm 2 \mu s$.

Vzb voltage Alignment on Z-SUS board

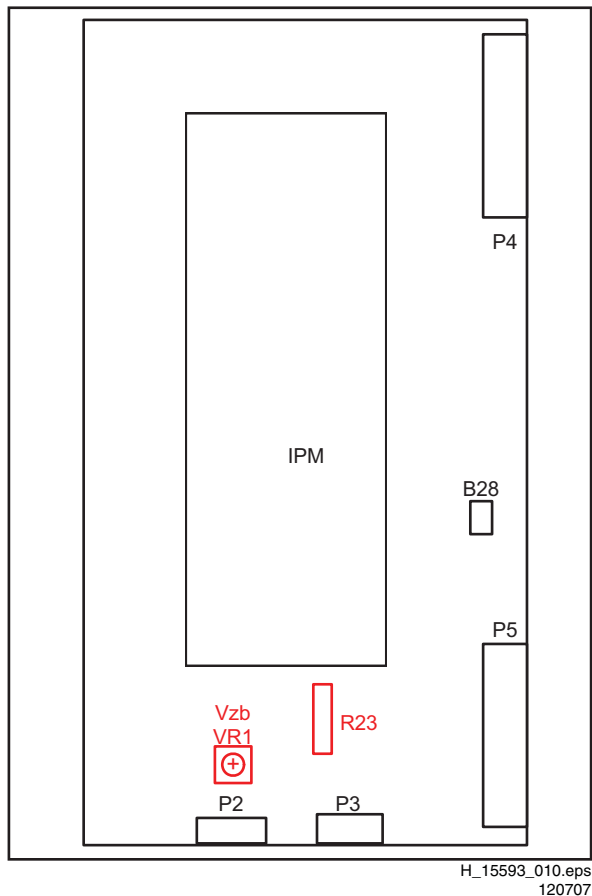


Figure 8-11 Vzb Voltage Alignment on the Z-SUS board

Adjusting Vzb voltage:

1. Measure the Vzb voltage ($165\text{ V} \pm 1\text{ V}$) across R23 on the Z-SUS board (see Figure "Vzb Alignment on the Z-SUS board").
2. Turn potentiometer VR1/Vzb on the Z-SUS board until the voltage is obtained, indicated on the existing voltage label on the PDP (if the Z-SUS board has not been replaced) or to the voltage indicated on the **new** label from the replacement kit (if the Z-SUS board has been replaced).

8.2.4 Internal Test Patterns

The CTRL board is capable of generating its own video test patterns. There are two possibilities, both based on jumper positions R406 and R407:

- **Black screen:** R406 is open and R407 is fitted (= standard setting). Now, if the PDP module does not receive any video signal, a full-black screen with **very low** light output is generated; this can be used for testing the PDP.
- **Automatic Test Patterns:** R406 is fitted and R407 is open (desolder R407 and mount it on pos. R406). Now, the test patterns are shown in an automatic loop.

Alternatively (and somewhat safer for the fragile tracks and components) the following method can be used to switch the PDP to its automatic test pattern mode: remove R407, switch on the set, and shorten position R406 for a moment.

Caution: The components and tracks mentioned above are very fragile, so take care not to damage anything!

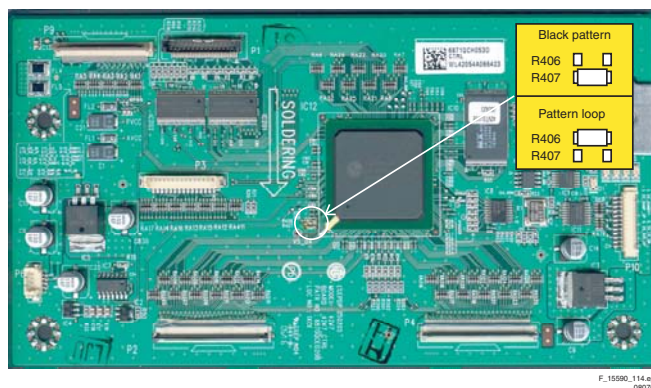


Figure 8-12 Internal test pattern mode

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

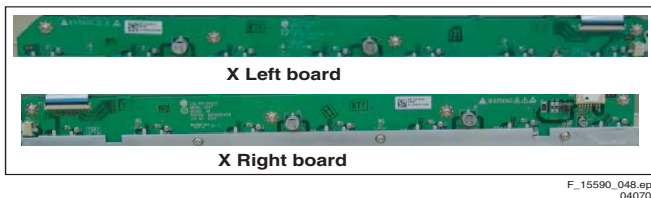
Index of this chapter:

- 9.1 X Board
- 9.2 Z Sustain Board
- 9.3 Y Drive Board
- 9.4 Y Sustain Board
- 9.5 Control Board
- 9.6 DC/DC Converter Part
- 9.7 FPC (Flexible Printed Circuit)
- 9.8 FFC (Flat Flexible Cable)
- 9.9 TCP (Tape Carrier Package)
- 9.10 IPM (Intelligent Power Module)
- 9.11 Abbreviation List
- 9.12 IC Data Sheets

9.1 X Board

9.1.1 Purpose

Receiving LOGIC signal from the CONTROL board and make ADDRESS PULSE (generates Address discharge) by ON/OFF operation, and then supplies this waveform to TCP (data).

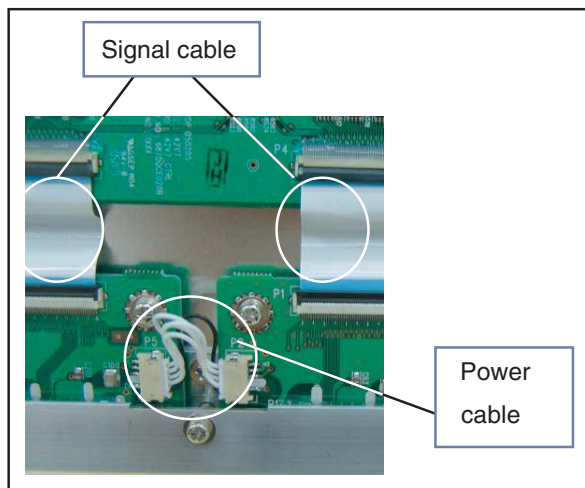


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040705

Figure 9-1 X boards

9.1.2 Dismantling

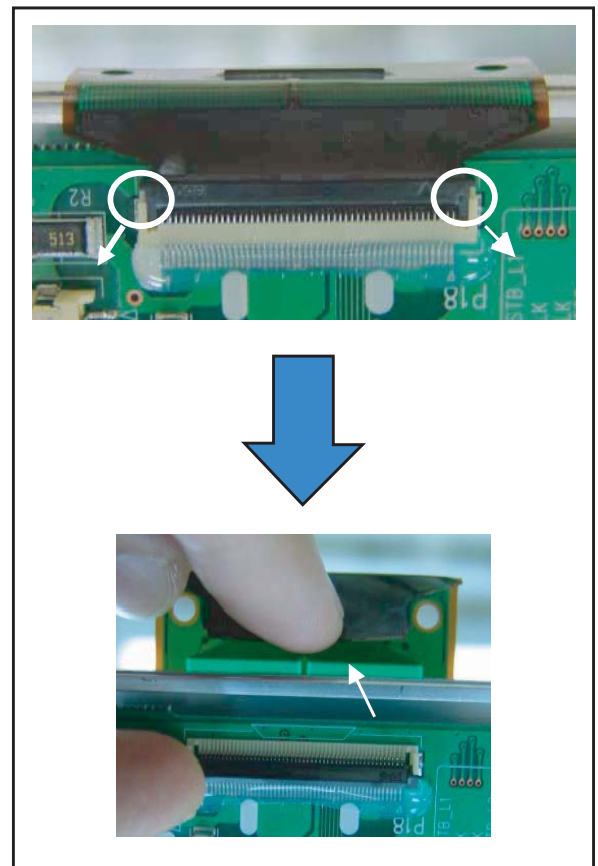
1. Remove connections between the boards:



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070705

Figure 9-2 Between CONTROL board and X board

1. Lift up lock as indicated by the arrows (handle with care, as this part is easy to break).
2. Pull TCP as indicated (handle with care, as the TCP film part is easy to damage).



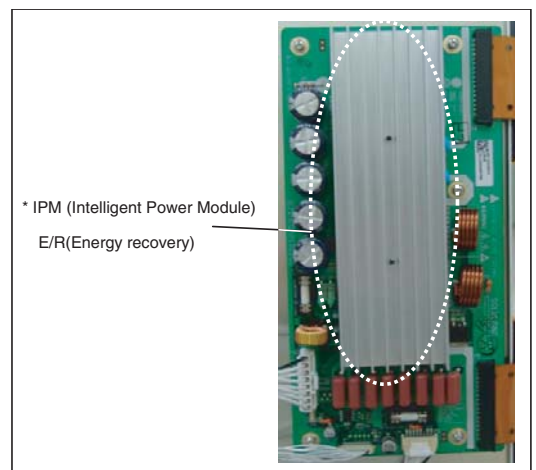
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Figure 9-3 TCP Separating

9.2 Z Sustain Board

9.2.1 Purpose

To make the SUSTAIN and ERASE pulses that generates SUSTAIN discharge in the panel by receiving LOGIC signal from CONTROL board. This waveform is then supplied to the panel through FPC (Z).



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040705

Figure 9-4 Z Sustain Board

9.2.2 Main Components

IPM, FET, DIODE, electrolytic capacitor, and E/R coil.

9.2.3 Dismantling

1. Pull out Locks as indicated by the arrows.
2. Condition in Lock part is pulled.
3. Pull FPC as shown by arrow.

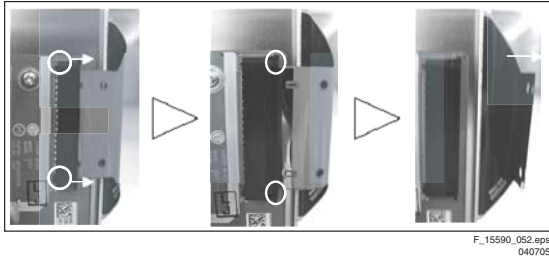


Figure 9-5 FPC Separating

9.3 Y Drive Board

9.3.1 Purpose

- To supply SUSTAIN, RESET waveform which are made by the Y SUSTAIN board and are supplied to the PDP through the SCAN DRIVER IC.
- To supply a waveform that selects the horizontal electrode (Y SUSTAIN electrode) sequentially.
 - Potential difference is 0 V between GND and Vpp of DRIVER IC in SUSTAIN period.
 - Being generated potential difference between GND and Vpp only in SCAN period.

Note: In case of 42" V7, used DRIVER SCAN ICs are in total of 8 EA (TOP, BOTTOM: each 4 EA).

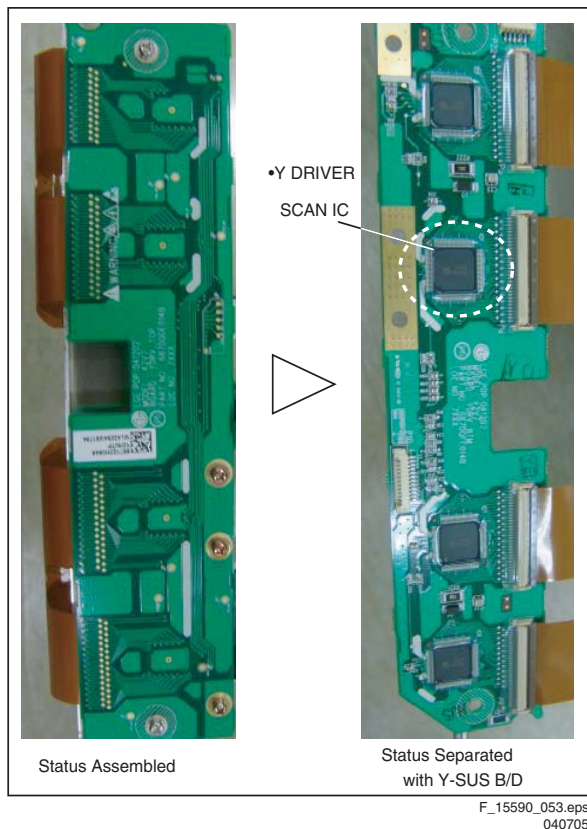


Figure 9-6 Y Drive board

9.4 Y Sustain Board

9.4.1 Purpose

Generates SUSTAIN, RESET, and Vsc (SCAN) voltages, and supplies them to the Y DRIVE board.

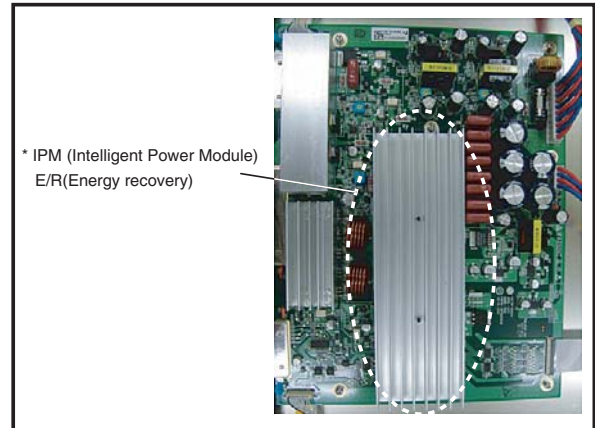


Figure 9-7 Y Sustain board

9.4.2 Main Components

IPM, diode, electrolytic capacitor, and FET.

9.5 Control Board

9.5.1 Purpose

Creates signal processing, and controls many FET on each DRIVER board with R, G, and B signals. Firstly receive 5 V, and then use two voltages (3.3 V / 1.8 V).

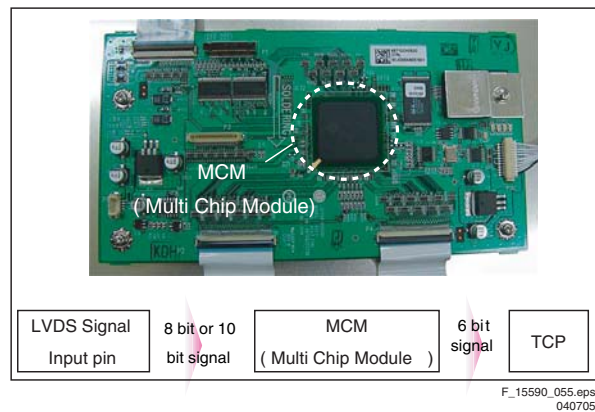


Figure 9-8 Control board

9.6 DC/DC Converter Part

9.6.1 Purpose

From 5V, Vs, and Va (from PSU), the DC/DC converter makes 5V, 15V, Vy, Vsc, 5Vf, and Va, which are essential for each board.

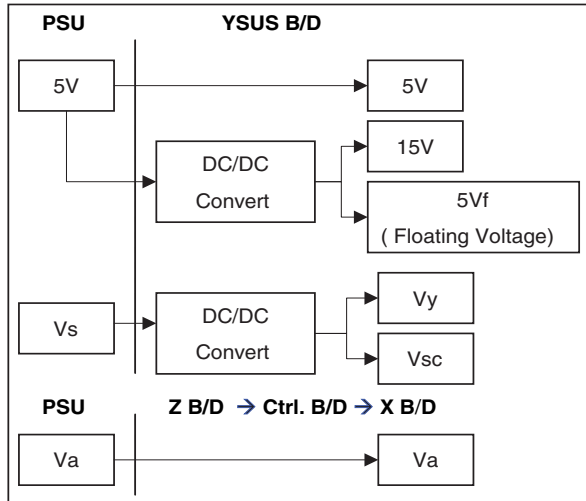


Figure 9-9 DC/DC Converter block diagram

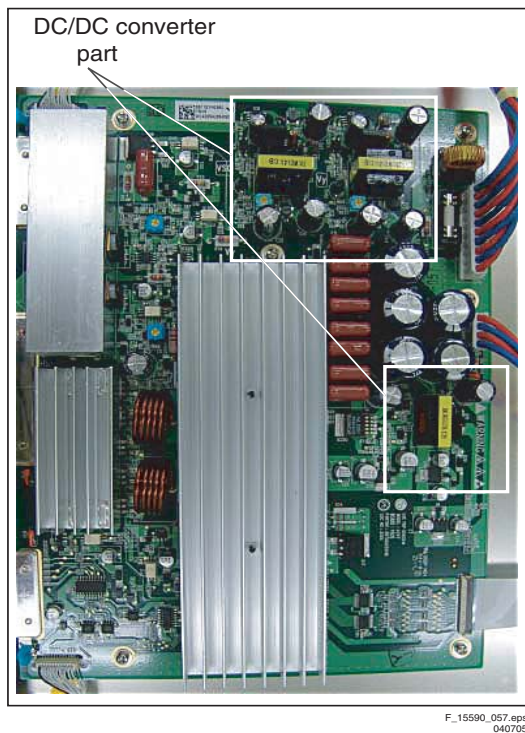


Figure 9-10 DC/DC Converter part

9.7 FPC (Flexible Printed Circuit)

9.7.1 Purpose

To supply a driving waveform to the PDP by connecting a PAD electrode of the PDP with a PWB (Y and Z boards).

- There are two types of this for the Y board: One is single-sided; the other is double-sided (these have a pattern on it).
- For Z board there is no pattern, single-sided, and Beta type (all of copper surface).

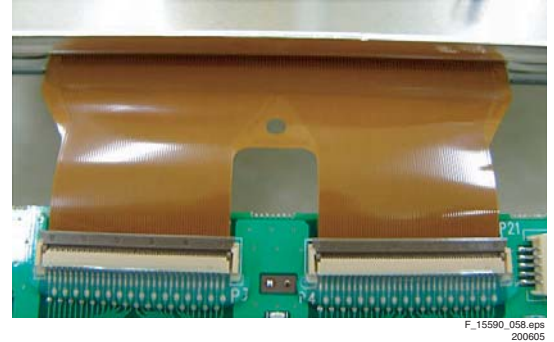


Figure 9-11 Flexible Printed Circuit

9.8 FFC (Flat Flexible Cable)

9.8.1 Purpose

For connecting LOGIC signals between boards. There are two types

- 0.5 mm pitch, 50-pin type.
- 0.5 mm pitch, 60-pin type.

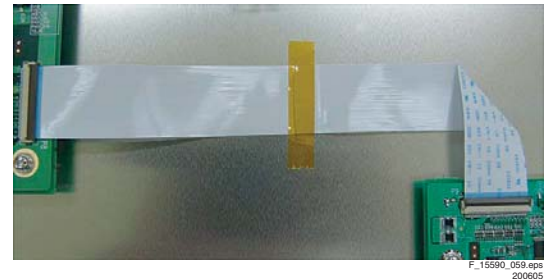


Figure 9-12 Flat Flexible Cable

9.9 TCP (Tape Carrier Package)

9.9.1 Purpose

To supply a waveform which is made by the X board to the PDP, and to select an output pin that is controlled by TCP when "on" or "off" (192 output pins per IC).

- TCP is package type, which is made by Direct Bonding between IC and electrode film.
- It is more effective than Wire Bonding type by increasing number of Data Driver IC output pins (96-pin -> 192-pins, pitch < 80 μm).



Figure 9-13 Tape Carrier Package

9.10 IPM (Intelligent Power Module)

9.10.1 Purpose

Attached to Z board and Y board, to make Sustain waveform.
Sustainer: supply a square wave to the PDP to make video.

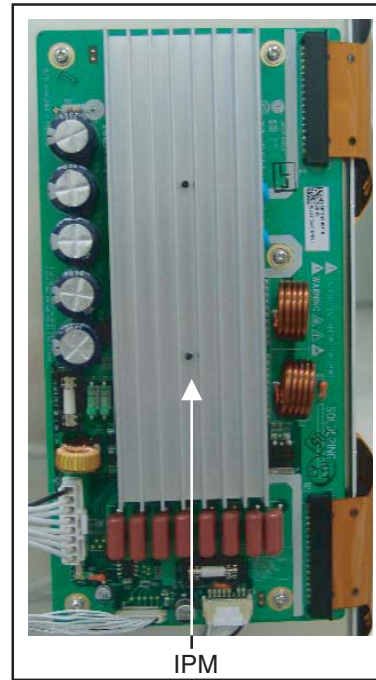


Figure 9-14 Intelligent Power Module

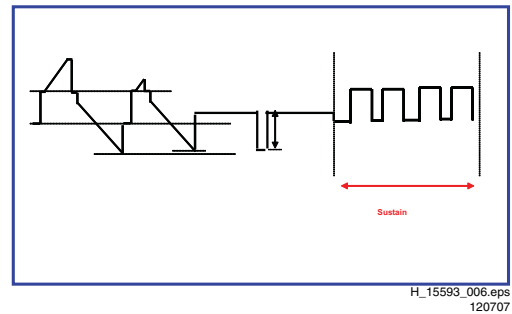


Figure 9-15 Sustain pulse (example, form is dependent on ROM)

9.10.2 Main Components

Heatsink, capacitor, diode, IC, resistor, transistor, and FET.

9.11 Abbreviation List

AC	Alternating Current
B/D	Board
CLK	Clock signal
CTRL	Control (board)
DC	Direct Current
FET	Field Effect Transistor
FPC	Flexible Printed Circuit
I/O	Input/Output
IC	Integrated Circuit
IPM	Intelligent Power Module
LED	Light Emitting Diode
LGE	Lucky Goldstar Electronics (supplier)
MCM	Multi Chip Module
PCB	Printed Circuit Board (same as PWB)
PDP	Plasma Display Panel
PFC	Power Factor Corrector circuit
PSU	Power Supply Unit
PWB	Printed Wiring Board (same as PCB)
RGB	Red, Green, Blue colour space
STB	Stand-by signal
TCP	Tape Carrier Package

9.12 IC Data Sheets

Not applicable

10. Spare Parts List

Please refer to the Philips Service website, for an actual overview (monthly updated).

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- Spare parts overview - PWBs added.

Manual xxxx xxx xxxx.2

- Spare parts overview - PWBs added.

Manual xxxx xxx xxxx.3

- Spare parts overview removed from manual, because this information can be found on the Philips Service website (monthly updated).
- Information on re-alignment of various PDP voltages updated (necessary if e.g. boards are replaced).

Service Service Service

LGE PDP 2K6 PDP42X3*

Service Manual

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1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

- 1.1 Technical Specifications PDP42X3*
- 1.1.1 General Specification
- 1.1.2 Definitions
- 1.1.3 Chassis Overview

1.1 Technical Specifications PDP42X3*

The PDP Module is divided into a Panel part and a Drive part.
The Panel part consists of Electrodes, Phosphor, various dielectrics, and gas, while the Drive part includes electronic circuitry and PWBs.

1.1.1 General Specification

Table 1-1 General Specifications

Model Name	PDP42X3*
Number Of Pixels (H x V)	1024 (*3) x 768
Pixel Pitch (H x V μm)	900 x 676
Cell Pitch (H x V μm)	300 x 676 (base: Green Cell)
Display Area (H x V mm)	921.6 x 519.2 \pm 0.5
Outline Dimension (H x V x D mm)	1005 x 597 x 61.2 \pm 1
Colour Arrangement	RGB closed type
Number Of Colours (R x G x B)	1024 x 1024 x 1024 (1,073,741,824)
Weight	15.3 \pm 0.5 kg
Aspect Ratio	16 : 9
Peak Brightness	Typical 1200 cd/m ² (1 % white window) Average 140 : 1 (Light room 100 Lx at centre)
Contrast Ratio	Typical 10000 : 1 (Dark room 1 % white window, white window pattern at centre)
Power Consumption	Max. 330 W (Full White)
Lifetime	Over 60,000 hours (initial brightness 1/2)

1.1.2 Definitions

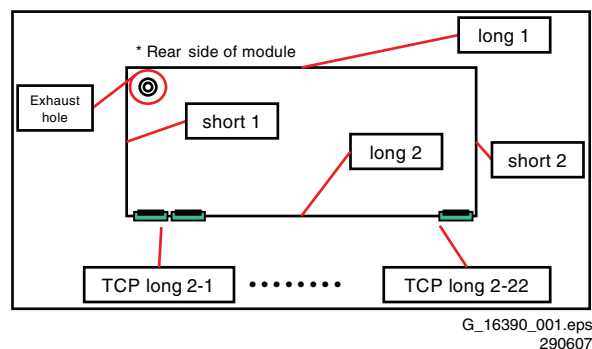


Figure 1-1 Definition of module position



Figure 1-2 Identification label

1. Model name.
2. Bar code (Code 128, contains the manufacture no.).
3. Manufacture no. (Module serial no.).
4. The trade name of LG Electronics.
5. Manufacture date (Year & Month).
6. The place of origin.
7. Model suffix.

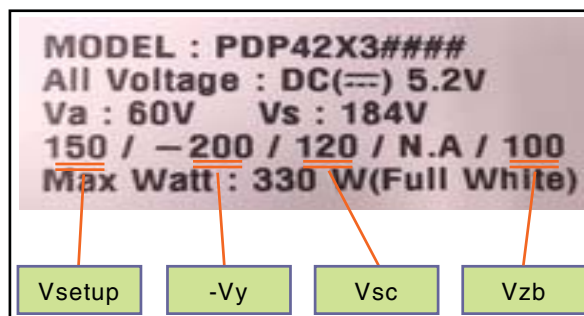


Figure 1-3 Voltage label (on rear side of module)

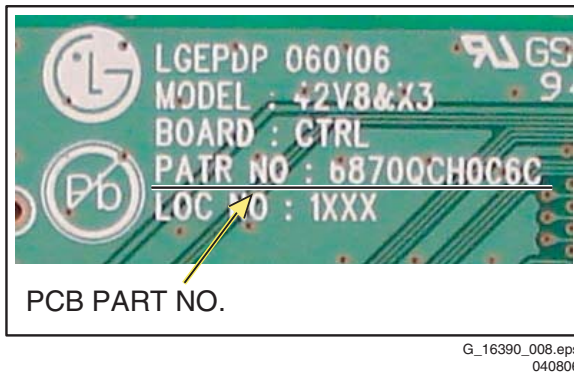


Figure 1-4 Part number printing (on board)

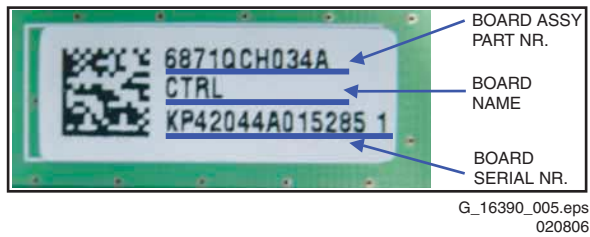


Figure 1-5 Part number label (on board)

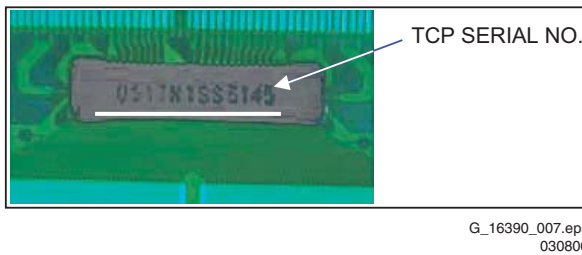


Figure 1-6 TCP serial number (on TCP)

1.1.3 Chassis Overview

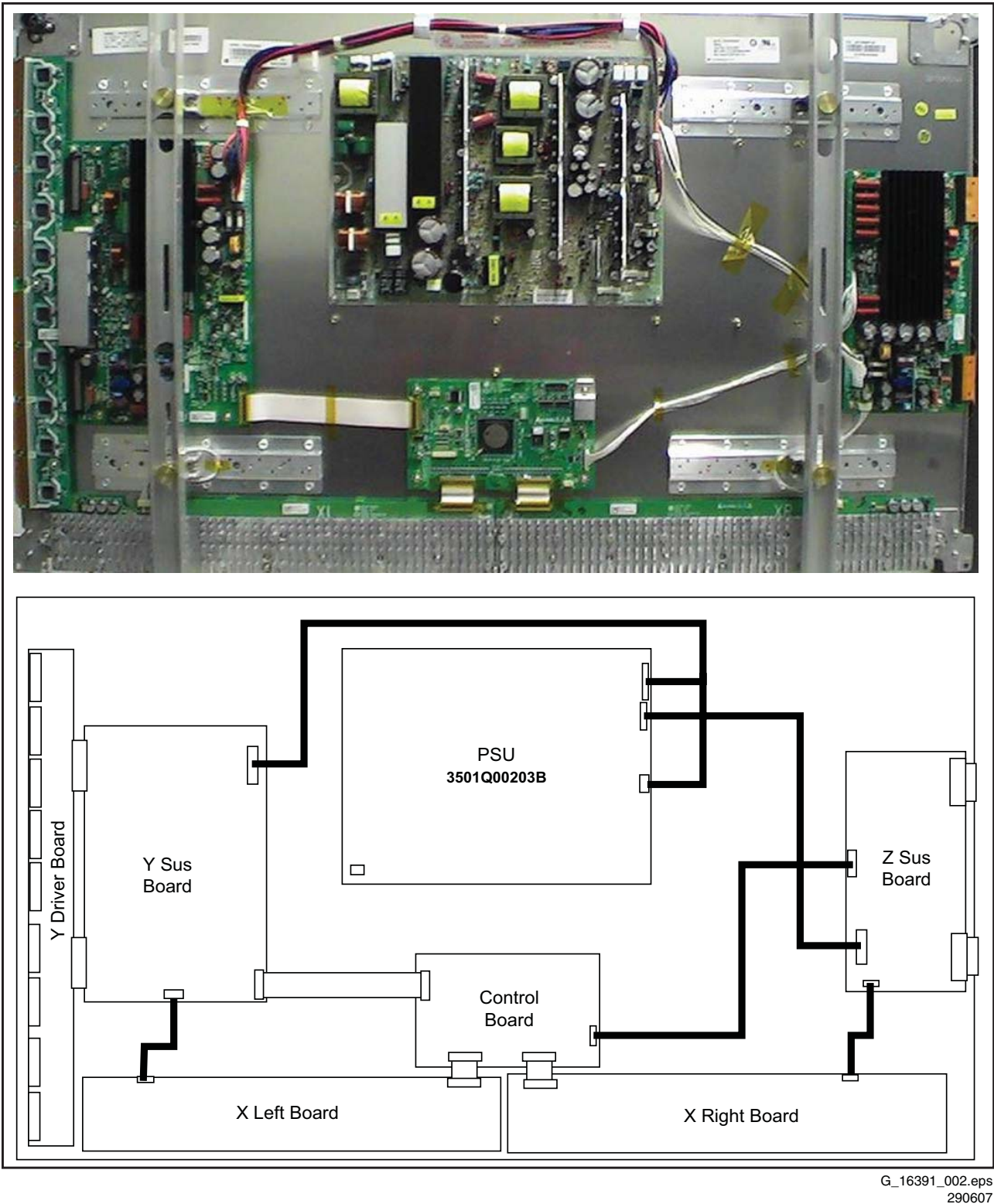


Figure 1-7 PWB location

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

2.1 Warnings

Notes:

- Only authorised persons should perform servicing of this module.
- When using/handling this unit, pay special attention to the PDP Module: it should not be enforced into any other way than next rules, warnings, and/or cautions.
- **"Warning"** indicates a hazard that may lead to death or injury if the warning is ignored and the product is handled incorrectly.
- **"Caution"** indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

2.1 Warnings

1. Do not touch the Signal and Power Connectors while this product operates. Do not touch EMI ground part and Heat Sink of Film Filter.
2. Do not supply a voltage higher than specified to this product. This may damage the product or can create hazardous situations.
3. Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where flammable materials surround it. Do not install or use the product in a location that does not satisfy specified environmental conditions. This may damage the product or can create hazardous situations.
4. If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn "OFF" the power. Continuing to use the product may cause electric shock or can create hazardous situations.
5. If the product emits smoke and abnormal smell, or makes an abnormal sound, immediately turn "OFF" the power. Continuing to use the product may cause electric shock or can create hazardous situations.
6. Do not (dis)connect the connector while power to the product is "ON". It takes some time for the voltage to drop to a sufficiently low level after the power has been turned "OFF". Confirm that the voltage has dropped to a safe level before (dis)connecting the connector.
7. Do not pull out or insert the power cable from/to an outlet with wet hands. It may cause electric shock.
8. Do not damage or modify the power cable. It may cause electric shock or can create hazardous situations.
9. If the power cable is damaged, or if the connector is loose, do not use the product, otherwise, this can lead to hazardous situations or may cause electric shock.
10. If the power connector, or the connector of the power cable, is dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to hazardous situations.
11. The PDP module uses a high voltage (max. 450 V_{DC}). Keep the cautions concerning electric shock and do not touch the device circuitry handling the PDP unit. And because the capacitors of the device circuitry may remain charged at the moment of Power "OFF", standing for 1 minute is required in order to touch the device circuitry.
12. Because the PDP module emits heat from the glass panel part and the drive circuitry, the environmental temperature must not be over 40 deg. C. The temperature of the glass panel part is especially high owing to heat from internal drive circuitry. And because the PDP module is driven by high voltage, it must avoid conductive materials.
13. If inserting components or circuit boards in order to repair, be sure to fix a lead line to the connector before soldering.
14. If inserting high-power resistors (metal-oxide film resistor or metal film resistor) in order to repair, insert it 10 mm away from a board.
15. During repairs, high voltage or high temperature components must be put away from a lead line.
16. This is a cold chassis but you better use an isolation transformer for safety during repairs. If repairing the electricity source part, you **MUST** use the isolation transformer.
17. Do not place an object on the glass surface of the display. The glass may break or be scratched.
18. This product may be damaged if it is subjected to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses.
19. The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded.
20. This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.
21. Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.
22. Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.
23. Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction. Because this product uses a discharge phenomenon, it may take time to light (operation may be delayed) when the product is used after it has been stored for a long time. In this case, it is recommended to light all cells for about 2 hours (aging).
24. This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.
25. If faults occur due to arbitrary modification or disassembly, LG Electronics is not responsible for function, quality or other items.
26. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult LGE in advance.
27. Within the warranty period, general faults that occur due to defects in components such as ICs will be rectified by LGE without charge. However, IMAGE STICKING due to misapplying the above provision (12), is not included in the warranty. Repairs due to the other faults may be charged for depending on responsibility for the faults.
28. While assembling the PDP module into a set, use the EMI ground part of the Film Filter for grounding, **BEFORE** removing the protective film, to prevent that static electricity can damage the TCPs or boards

3. Directions for Use

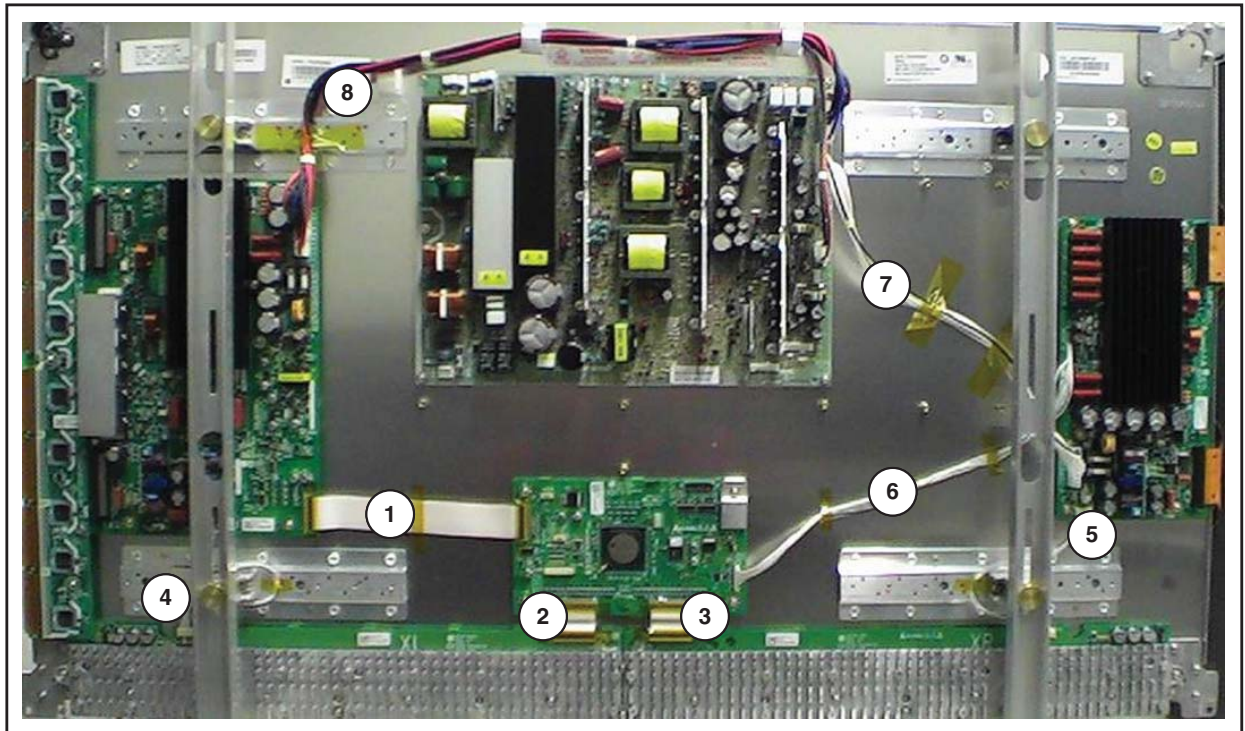
Not applicable.

4. Mechanical Instructions

Index of this chapter:

- 4.1 Mechanical Overviews
- 4.2 Panel/assy removal
 - 4.2.1 Power Supply Unit
 - 4.2.2 Control Board
 - 4.2.3 Y Sustain Board
 - 4.2.4 Y Driver Board
 - 4.2.5 Z-Sustain board
 - 4.2.6 X-board

4.1 Mechanical Overviews

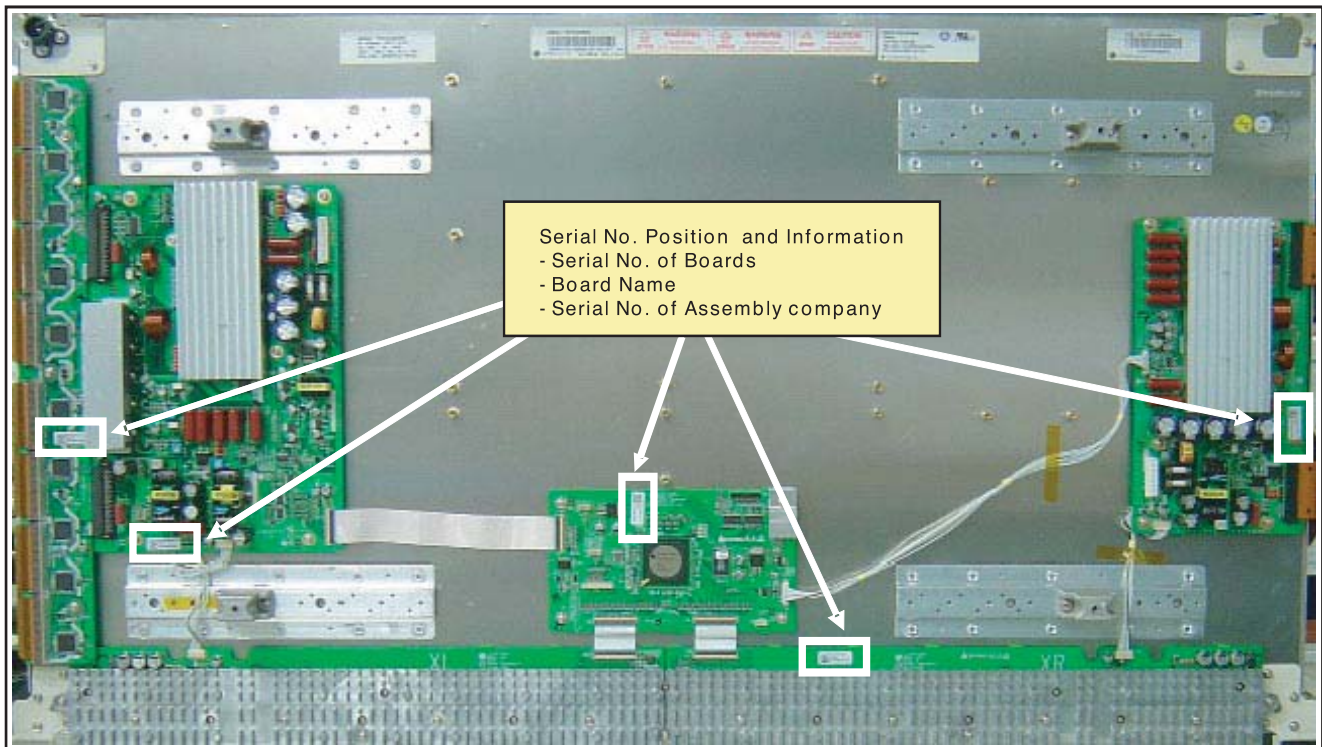


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Figure 4-1 Cable dressing

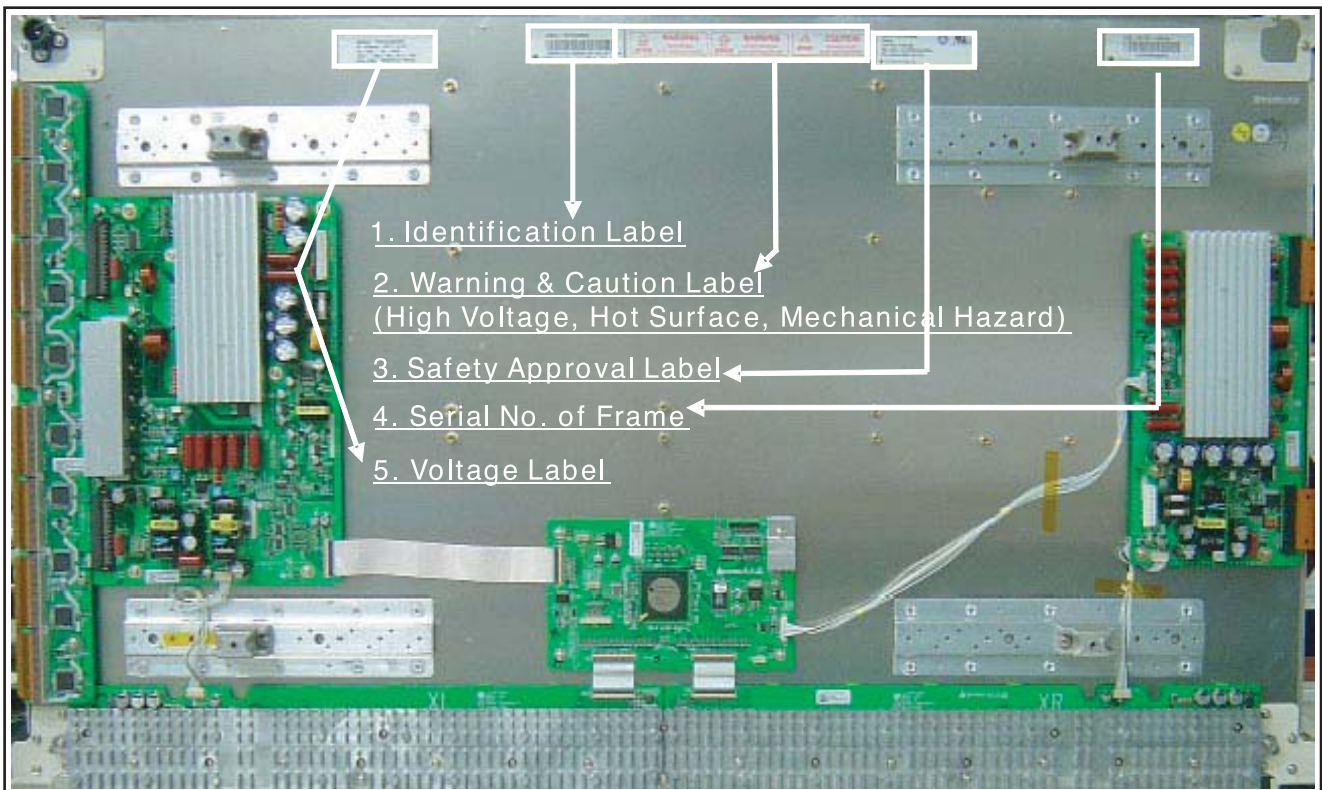
Table 4-1 Cable function

Cable No.	Function
1	Drive signal for Y waveform
2 & 3	RGB data to be transferred to panel
4 & 5	5V and Va supply for X-boards Left and Right
6	Drive signal for Z-waveform
7 & 8	Va, Vs and 5 V supply for PDP operation



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Figure 4-2 Label location on PWB's



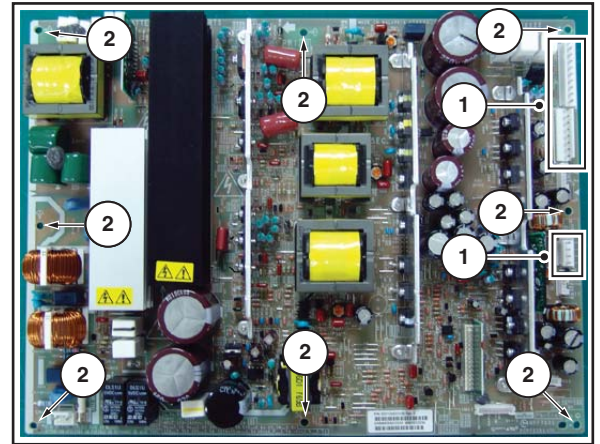
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Figure 4-3 Label indication

4.2 Panel/assy removal

4.2.1 Power Supply Unit

1. Unplug the connectors [1].
2. Remove the fixation screws [2].

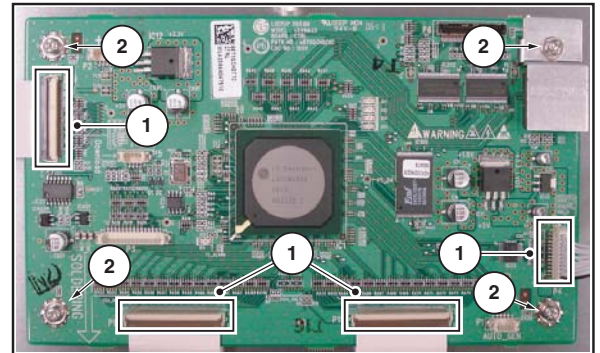


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220806

Figure 4-6 PSU removal

4.2.2 Control Board

1. Unplug the connectors [1].
2. Remove the fixation screws [2].



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Figure 4-7 Control board removal

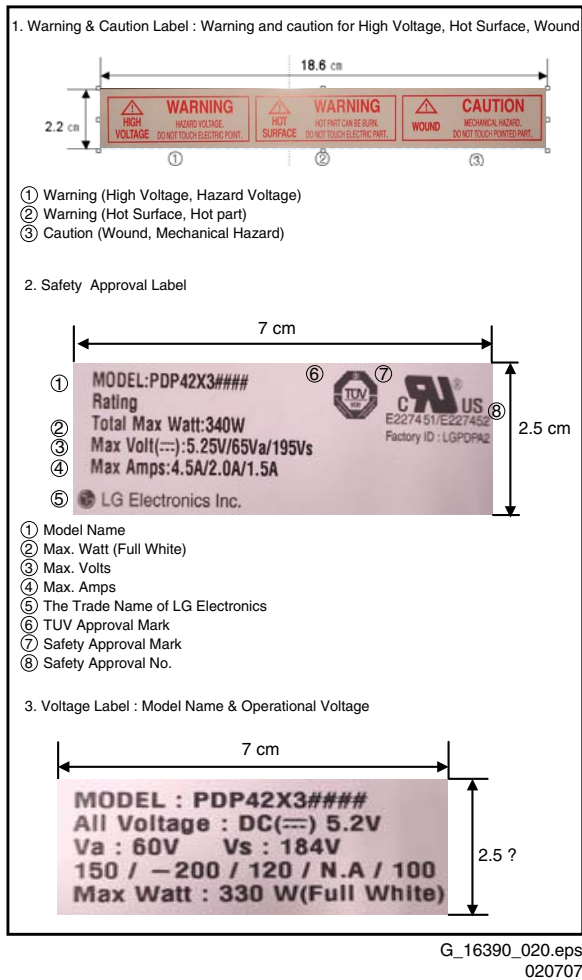


Figure 4-4 Label information (1)

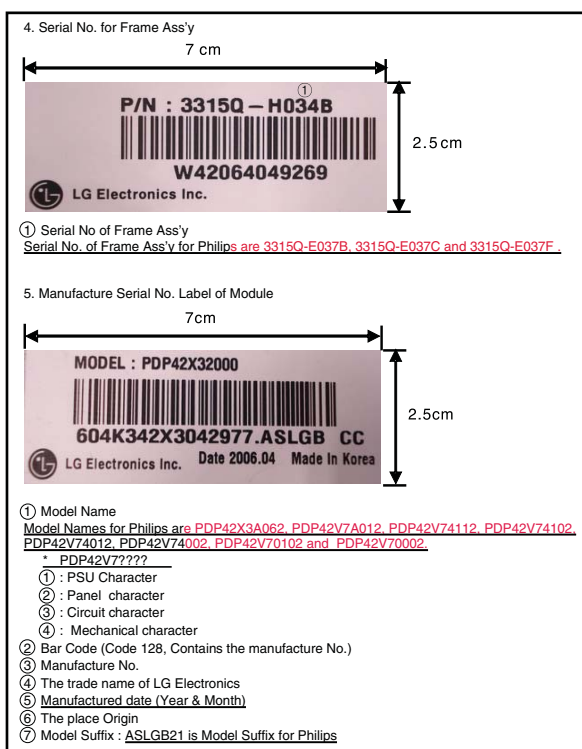


Figure 4-5 Label information (2)

4.2.3 Y Sustain Board

1. Unplug the connectors [1].
2. Remove the fixation screws [2].
3. Slide the board to the right, while unplugging connectors [3]. **Do not touch the heatsink!**

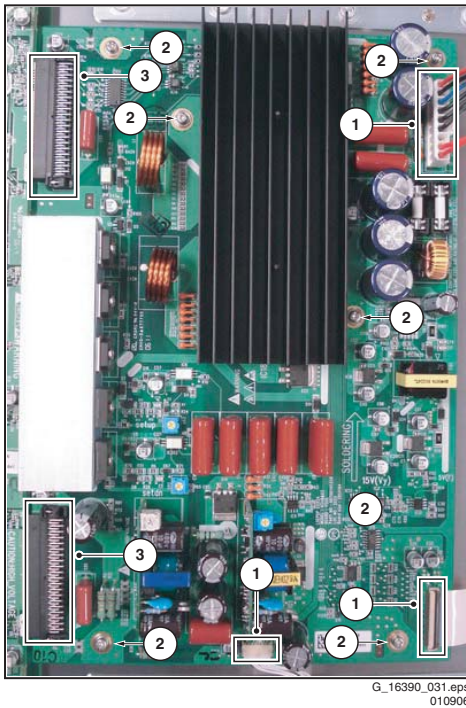


Figure 4-8 Y-SUS board removal

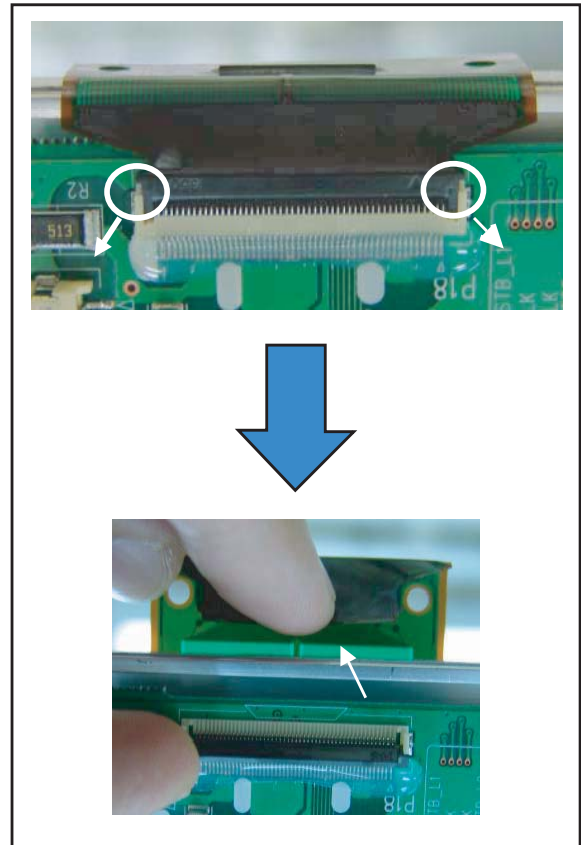


Figure 4-10 TCP Separation

4.2.4 Y Driver Board

1. Remove the Y-SUS board [1], as described previously.
2. Remove the fixation screws [2].
3. Separate the TCP's [3].

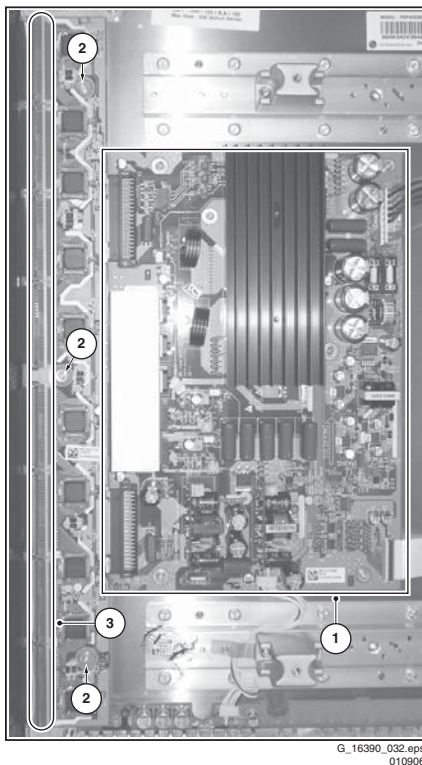
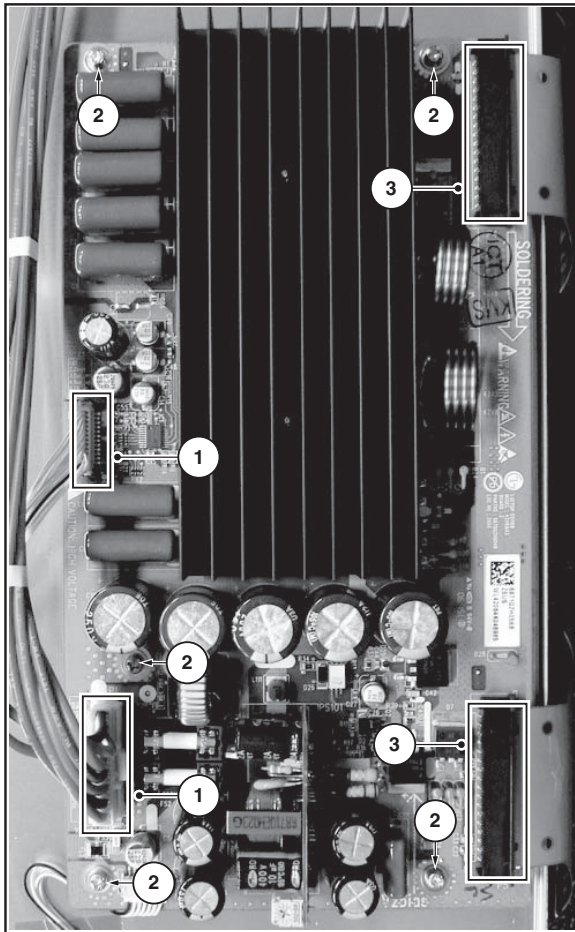


Figure 4-9 Y driver board removal

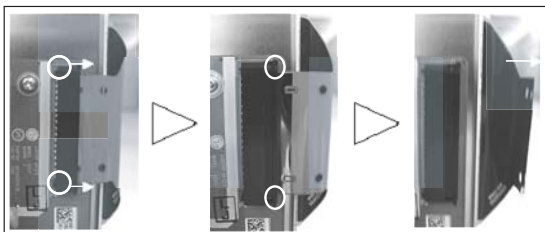
4.2.5 Z-Sustain board

1. Unplug the connectors [1].
2. Remove the fixation screws [2].
3. Slide the board to the right, while unplugging connectors [3]. **Do not touch the heatsink!**
4. Pull out the locks of the FPC's [3] as indicated by the arrows.
5. Condition in Lock part is pulled.
6. Pull FPC as shown by arrow.



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0108069

Figure 4-11 Z-SUS board removal

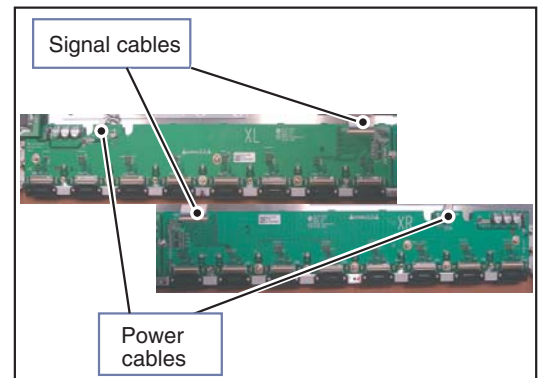


F_15590_052.eps
040705

Figure 4-12 FPC removal

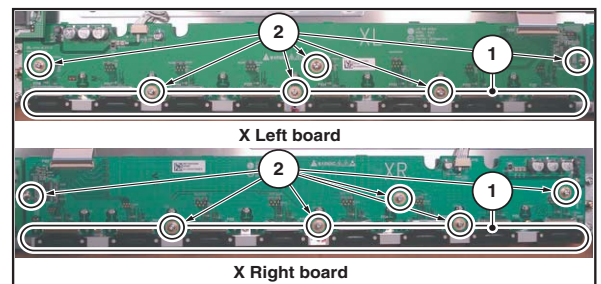
4.2.6 X-board

1. Unplug the power cable.
2. Unplug the signal cable.
3. Remove the heatsink.
4. Separate the TCP's [1].
5. Remove the fixation screws [2].



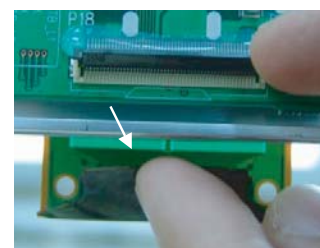
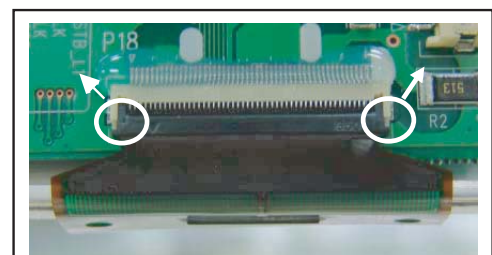
G_16390_028.eps
010906

Figure 4-13 X board removal 1/2



G_16390_027.eps
220806

Figure 4-14 X board removal 2/2



G_16390_034.eps
100806

Figure 4-15 TCP Separation

5. Service Modes, Error Codes, and Fault Finding

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5.3 Defect Description Form

5.1 Quick Module Check

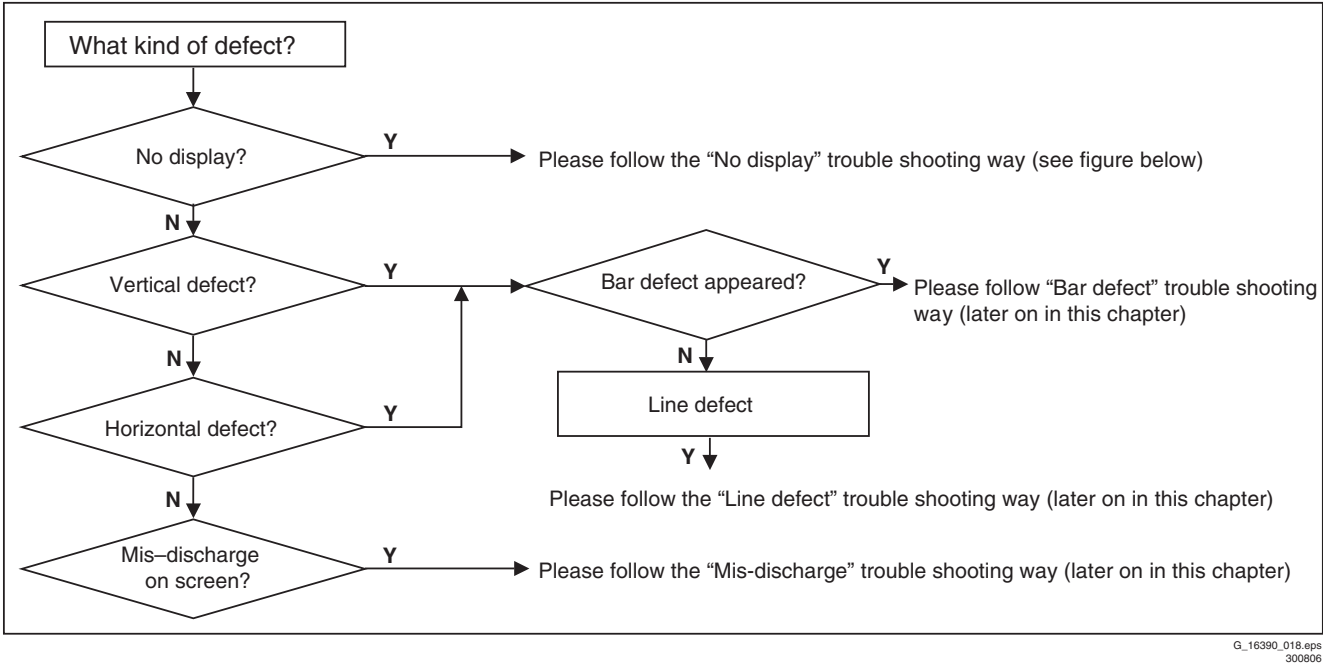


Figure 5-1 Logical judgement

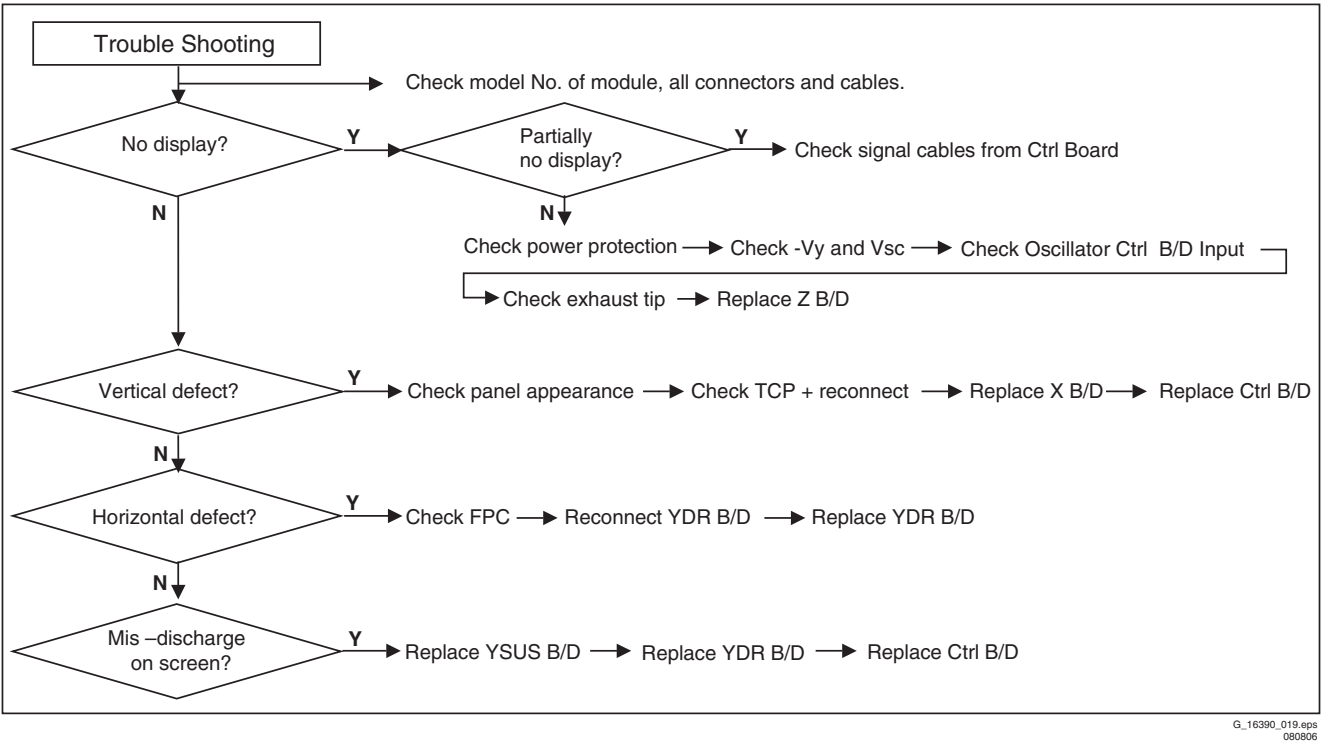


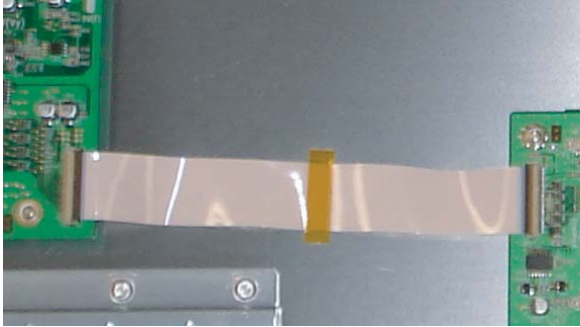
Figure 5-2 Quick check

5.1.1 No Display

Check each section with following method.
If there is a problem, replace or repair that part.
If it is not found, go to the next section.

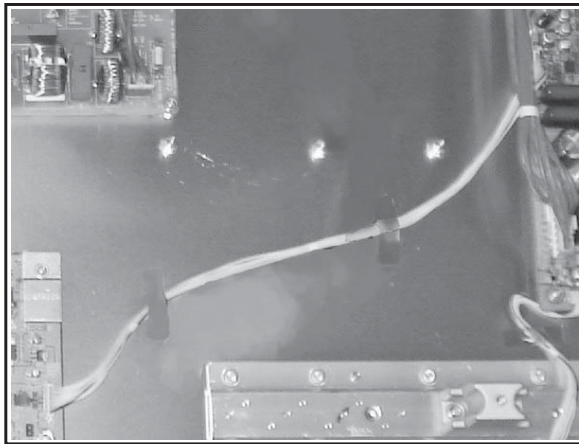
Connectors

Check all connectors (PSU, Y-SUS, CTRL, Z-SUS). The module may not function normally by a misconnection (can not send signal and/or power). Also misconnection for a long period can cause a specific board to fail.



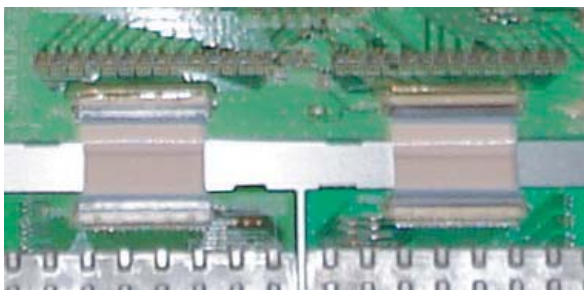
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Figure 5-3 Control + Y-SUS board



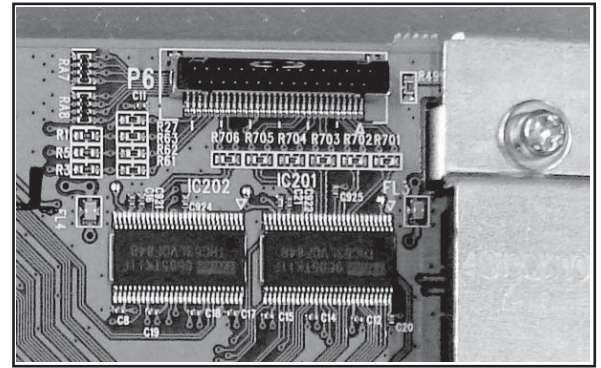
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Figure 5-4 Control + Z-SUS board



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110806

Figure 5-5 Control + X board



G_16390_042.eps
010906

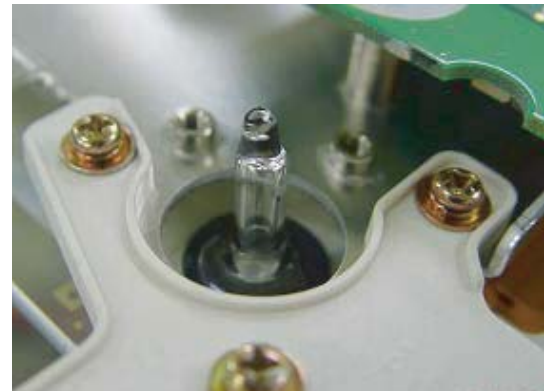
Figure 5-6 Signal input (LVDS)

Exhaust Tip

Check the Exhaust Tip for cracks with the naked eye to check the vacuum state.

If there is a problem, replace the PDP module by a new one. In case of vacuum breakdown, the module makes a shaking noise because of inside gas ventilation.

There may be a small crack, which cannot be seen with the naked eye. This noise is different from capacitor noise.



NORMAL

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050705

Figure 5-7 Exhaust tip "normal"

PSU (see figure "PSU trouble shooting")

1. Check each unit part of PSU inside with naked eye (capacitor, FET, IC, resistor).
2. Check fuse.
3. Check output voltage, which is converted from AC to DC.
4. Voltage Check (5V, Va, Vs).

When PSU protection occurred: check for a short circuit between the Y-SUS and the Z-SUS board.

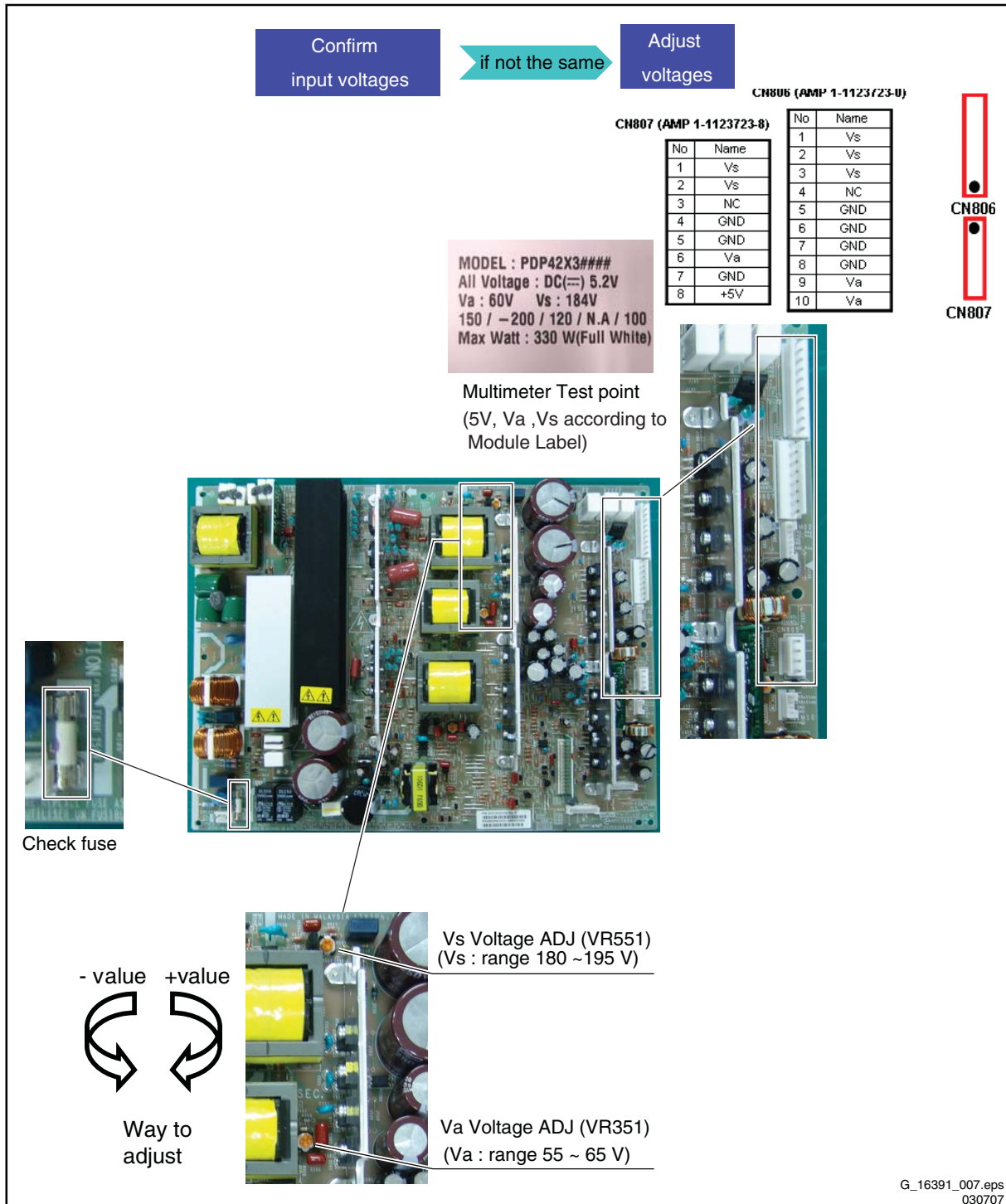


Figure 5-8 PSU trouble shooting

PSU Power Protection

When the power protection gets active, the power is switched "OFF" automatically within 2-3 min. from power "ON". The power protection function protects the boards when a short occurs on circuits of the PDP module, or when a power problem occurs. If there is no power, even after replacing the PSU, find out where the short occurred.

In case of a PSU protection, the red LED will be "ON" and an error code will be displayed via the green blinking LED (see also paragraph "Detailed PSU Trouble Shooting", further on). In case of a PSU protection, disconnect the power supply connectors to the boards, to find if the boards are defective or the PSU itself.

5.1.2 Bar Defect (Vertical)

Check each section with the following method. If there is a problem, replace or repair that part. If not go to the next section.

Connector

Check the TCP connector and cables. If not connected well, it will result in a bar defect and abnormal display behaviour.

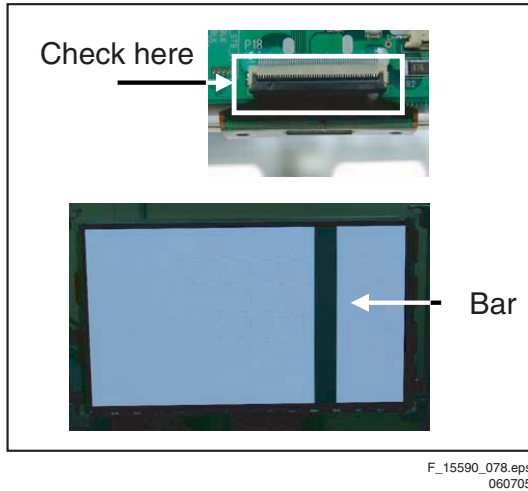


Figure 5-9 Connector check (1)

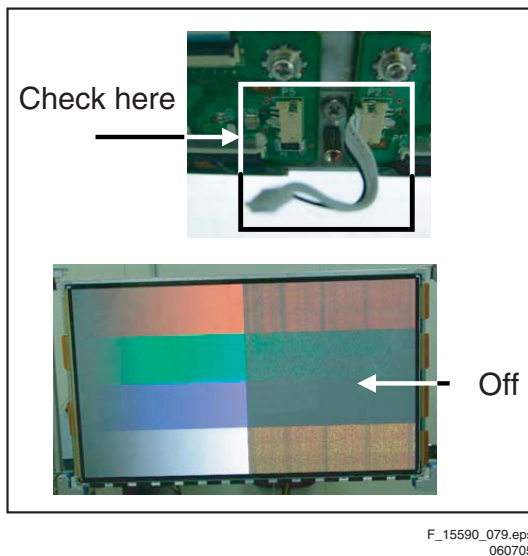


Figure 5-10 Connector check (2)

Checking the TCP

Confirm whether the TCP was torn or chopped.

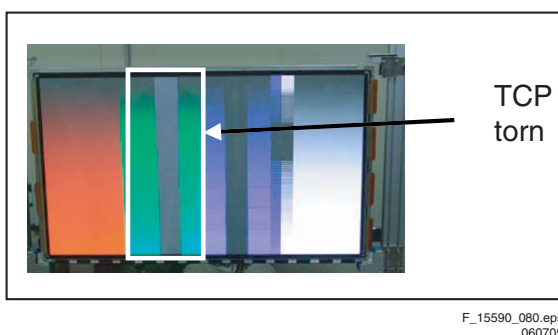


Figure 5-11 TCP torn

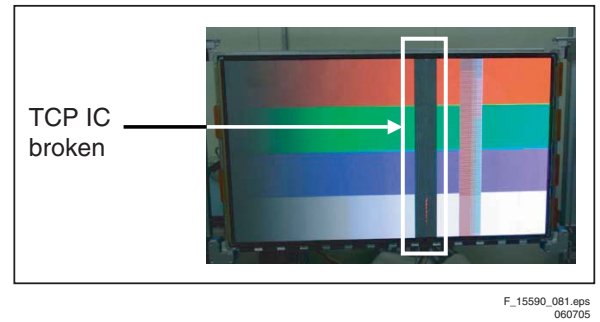


Figure 5-12 TCP IC broken

Control Board

The Control board supplies the video signal to the TCP. So, if there is a bar defect on screen, it may be a Control board problem.

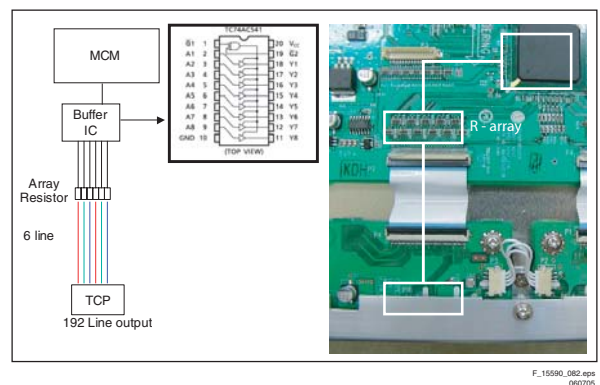


Figure 5-13 Control board address flow

5.1.3 Line Defect (Vertical)

In case of one line open or shorted, check for dirt (foreign substances) in TCP connector. First, try to remove the dirt with compressed air. If, after this, the same line appears again, replace the panel.

Line Open or Short

This phenomenon is due to a TCP IC internal short or electrode problem. In this case, replace the panel.

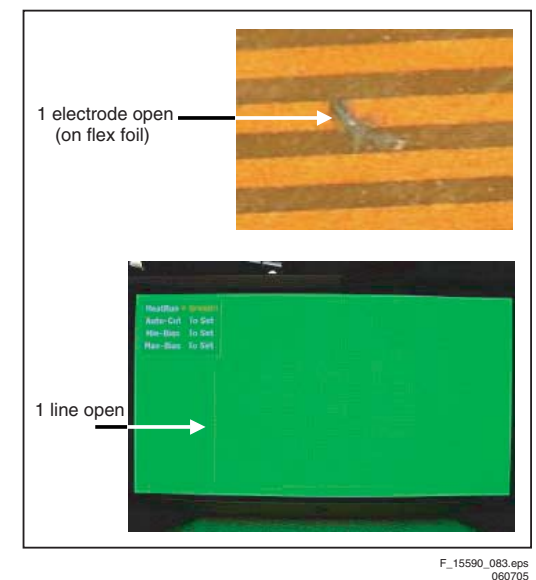


Figure 5-14 Single line defect

Line Open or Short with the Same Distance

This is an MCM of Control board defect. The MCM cannot be replaced separately. So replace the Control board.

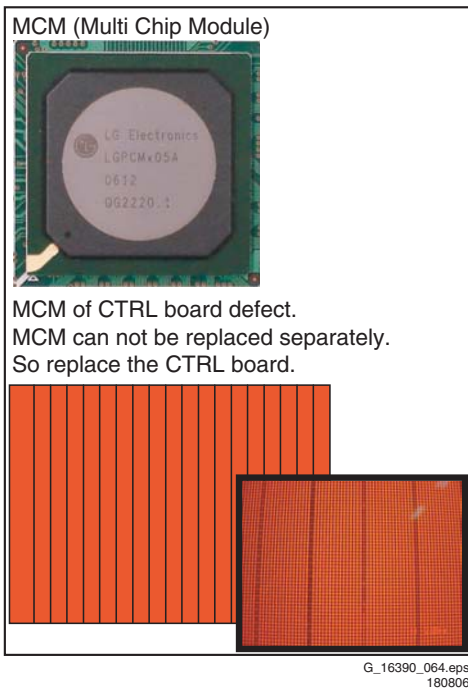


Figure 5-15 Evenly repeated lines

5.1.4 Bar Defect (Horizontal)

Most horizontal defects can be repaired. In case of adherence between a part of the film and the rear panel electrode, or a panel electrode open/short, replace the PDP panel.

Connector

If the connectors on the Y board and Z board are not plugged in well, it can result in a horizontal bar, because the sustain voltage cannot be supplied to the panel. So check the FPC connectors and YSUS<->YDRV first.

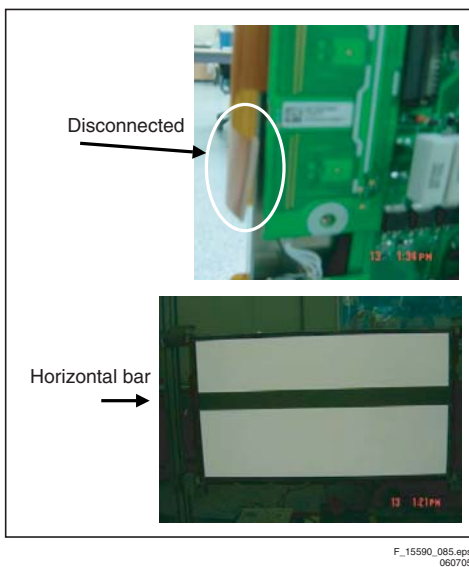


Figure 5-16 Check FPC connectors

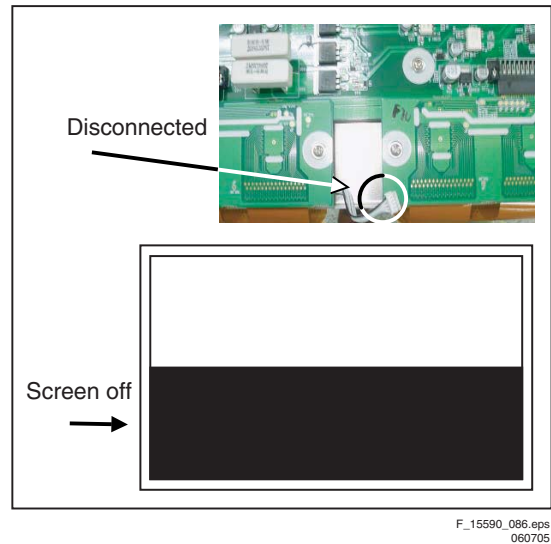


Figure 5-17 Check drive connectors

Scan IC Check

Check the diode value of the right side part of the output pin.

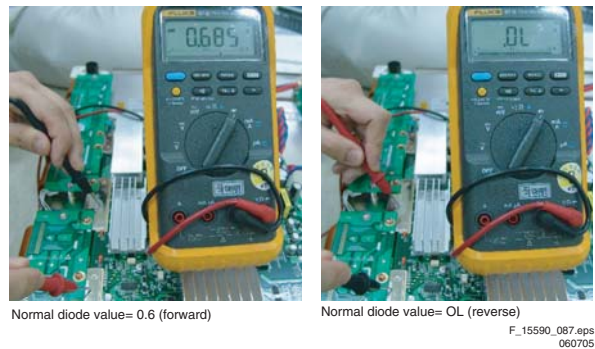


Figure 5-18 Scan IC output diode check

5.1.5 Line Defect (Horizontal)**FPC Check**

In case of one or more horizontal lines, this is probably due to FPC or panel inside the Control board. Y board is just normal.

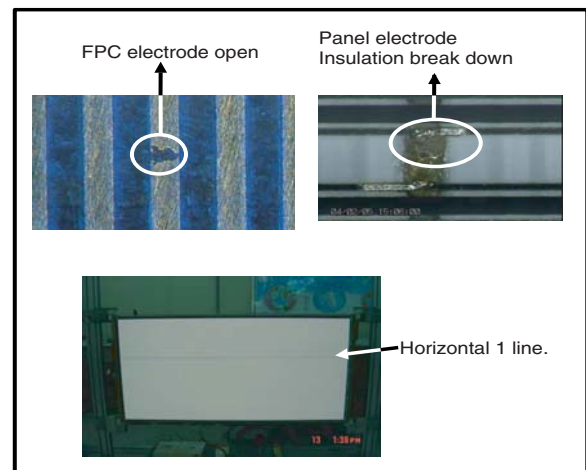
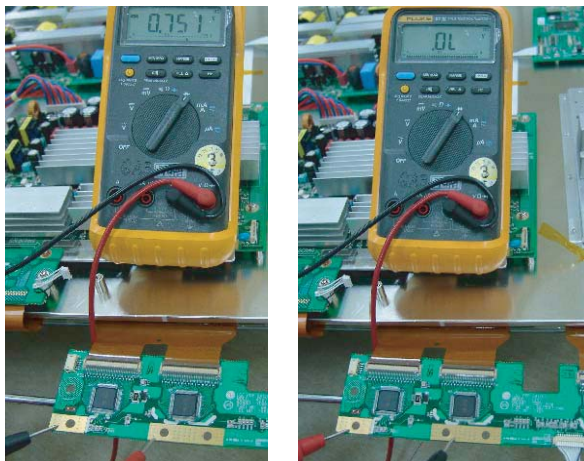


Figure 5-19 Open FPC electrode / Panel electrode breakdown

Scan IC Check

Check diode value of the right side part of the output pin.



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290605

Figure 5-20 Scan IC output diode check

5.1.6 Mis-discharge Defect

Most of mis-discharge appearance is a problem of the Y-DRV, Y-SUS, or Z board.

Check these boards when mis-discharge occurs.

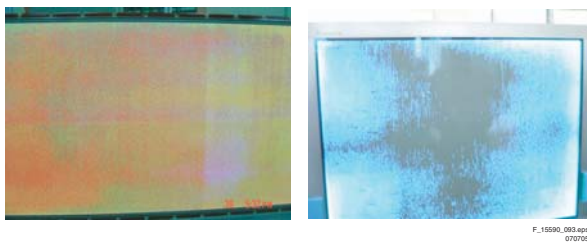


Figure 5-21 Mis-discharge

Checking Order

1. Check the Y-SUS and Z-SUS signal cables.
2. Check if the Y-DRV IC is defective.
3. Check the Y-SUS board voltages (-Vy, Vscw).
4. Check if the Y-SUS and/or Z-SUS IPMs are defective (see paragraph "How to Check an IPM" below).
5. Replace the Control board.

How to Check an IPM**Forward direction**

Measure between:

- GND (+) and Sus-out (-).
- Sus-out (+) and Vs (-).

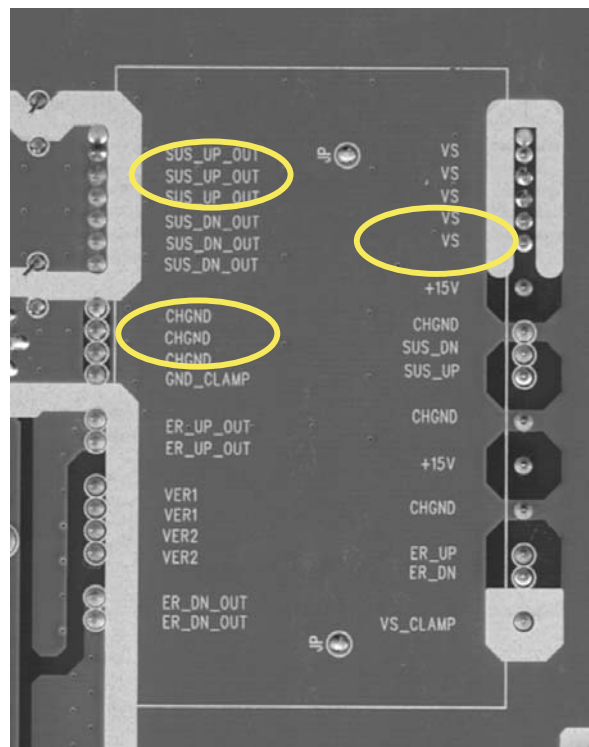
When both test diode values are over 0.4 => OK.

Reverse direction

Measure between:

- GND (-) and Sus-out (+).
- Sus-out (-) and Vs (+).

When all test diode values are infinite => OK



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010906

Figure 5-22 IPM check

5.2 Detailed Module Check**5.2.1 No Display****The Screen Does Not Display a Picture**

1. Check whether on the CTRL board LED (D12, D13, D14) is turned "ON" or not.
2. Check the power and signal cable of the CTRL board.
3. Check if the X, Y, and Z boards are plugged in correctly.
4. Check the connection of the X, Y, and Z boards to the CTRL board.
5. Measure the output wave of X, Y, and Z boards with an oscilloscope (> 200 MHz) and find the troubled board by comparing the output wave with the figures below.
 - Measuring point for the Y board: TP ("Waveform" on the Y-Driver board).
 - Measuring point for the Z board: TP (bead B28).
6. Check the SCAN (Y side) IC.
7. Check the DATA (X side) TCP IC.
8. Replace the CTRL board.



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300806

Figure 5-23 Output waveforms on X, Y, and Z-boards

5.2.2 Display Defects

Half of the Screen is Not Shown

- On the XR board:
 - Check if the power connector of the XR board is plugged in correctly.
 - Check if the 60-pin connection of the CTRL board to the XR board is plugged in correctly.
- On the XL board:
 - Check if the power connector of the XL board is plugged in correctly.
 - Check if the 60-pin connection of the CTRL board to the XL board is plugged in correctly.
- Replace relevant X board.

Notes:

Relationship between Screen and X board:

Screen	X-board
Left half of the screen	Right X-board
Right half of the screen	Left X-board

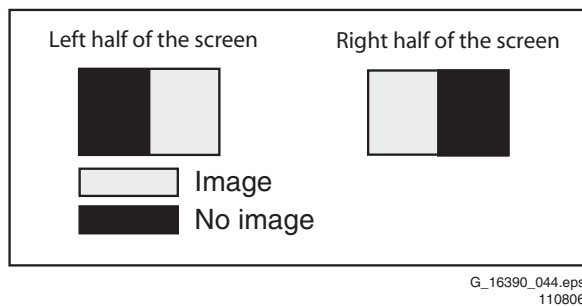


Figure 5-24 Screen display "1/2 display"

Vertical Parts of the Screen are Missing

- This can be related to a problem between the Data TCP and the X board.
- Verify that the connector of the Data TCP is well connected to the X board (it corresponds to the part of the screen that does not display the image).
- Confirm whether the Data TCP fails (examination with the naked eye of blown ICs or other parts included).
 - If an IC is damaged: replace the panel.
 - In case of an X board short circuit or an open PWB pattern: when the TCP IC is not defective, replace the X board.

Notes:

- Example of screen display (any of the Data TCPs can be shown).

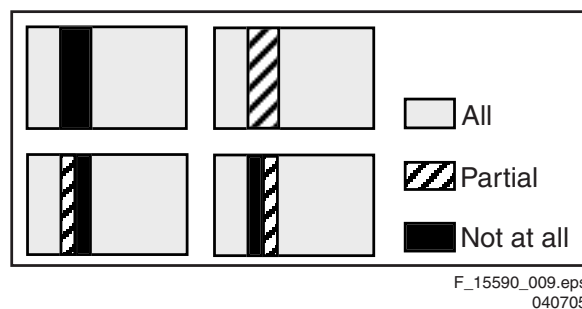


Figure 5-25 Screen display "Vertical parts missing"

- How to examine the Data TCP IC
 - Connect [1] "Va Power" to the minus and [2] "GND" to the plus of an ohmmeter, and then examine the diode in forward or reverse direction.

- Examine with the naked eye traces of blown ICs [3] or other parts.

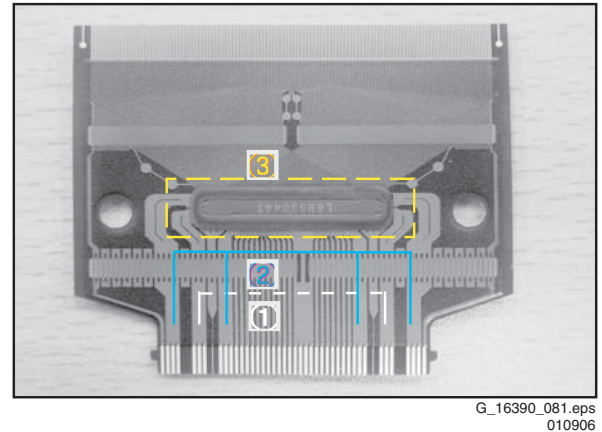


Figure 5-26 Data TCP IC examination

Unusual Pattern on Display

- In case of generation of an unusual pattern of the Data TCP IC unit as shown in the picture below, check the fixation of the relevant X board. If that doesn't help, replace the X board.
- In case of "Case 1":
 - Check the connection between the Data TCP connector and the IC.
 - Replace the relevant X board, or the Control board.
- In case of "Case 2" or "Case 3":
 - Check the connection between the CTRL board and the relevant X board.
 - Replace the relevant X board or the CTRL board.

Note:

- If the silicon tape between the X board and the heatsink feels (partially) hard, it has to be replaced.

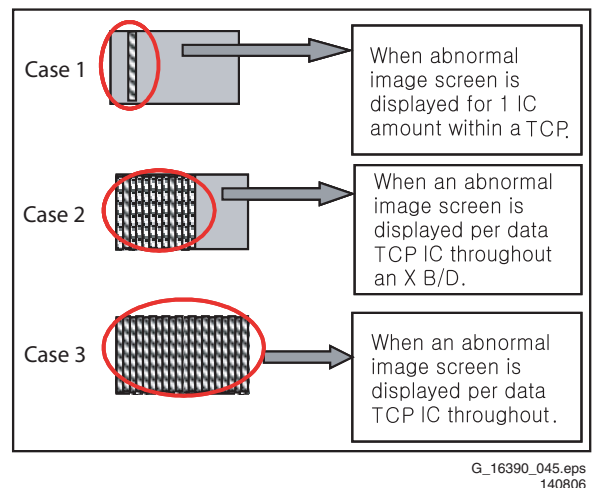


Figure 5-27 Possible cases

Scan FPC Problem

- Check the connection between Y DRV board and Scan FPC.
- If the Scan IC is defective, replace the Y DRV board.

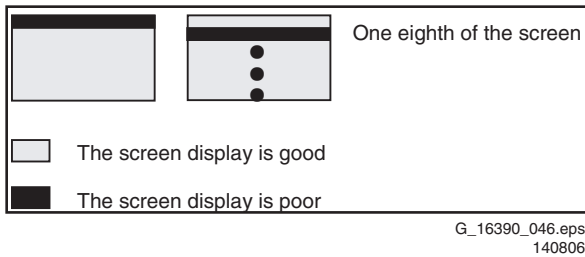


Figure 5-28 Screen display "Scan FPC problem"

- Check method of the SCAN IC
 - Connect the Vpp pin to the plus and "GND" to the minus of an ohmmeter, and then examine the diode in forward or reverse direction.

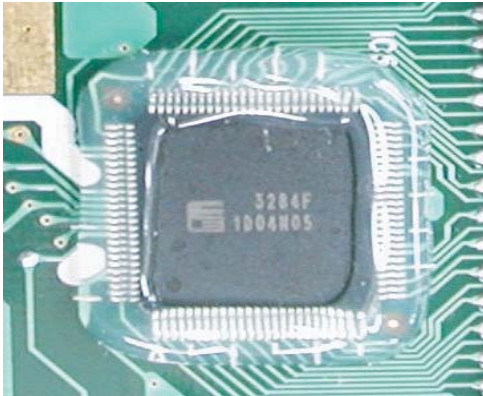


Figure 5-29 Scan IC

Vertical Lines with Regular Gap (Vertical Stripe Flash at Special Colour)

- Replace the CTRL board.

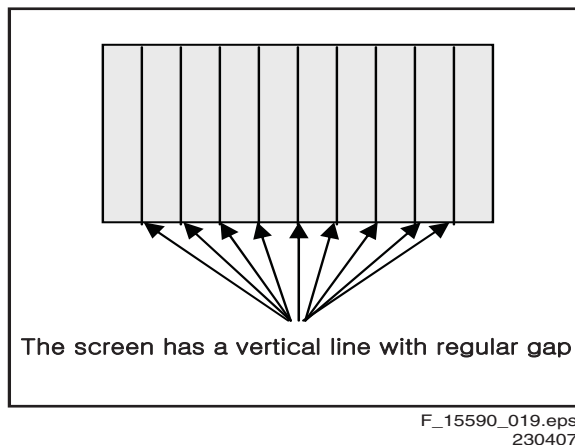


Figure 5-30 Screen display "Vertical lines with regular gap"

Data Copy in Vertical Direction

- Replace the Y-DRV board or the YSUS board.

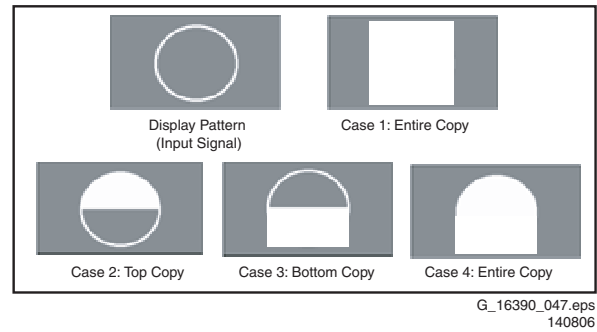


Figure 5-31 Screen display "Data copy in vertical direction"

One or Several Vertical Line(s) on the Screen

- It may be caused by:
 - Open or short circuit on DATA TCP FPC attached panel.
 - Defect on DATA TCP IC attached panel.
- Replace the panel.

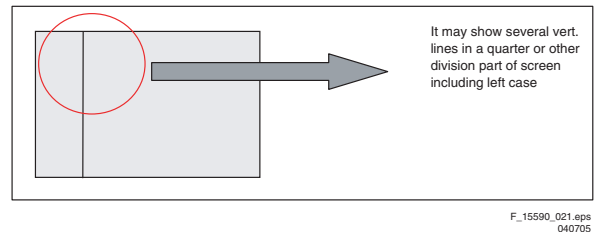


Figure 5-32 Screen display "Vertical lines"

One or Several Horizontal Lines on the Screen

- It may be caused by:
 - Open or short circuit on SCAN FPC attached panel.
 - Defect on SCAN IC attached panel.
- Replace the panel.

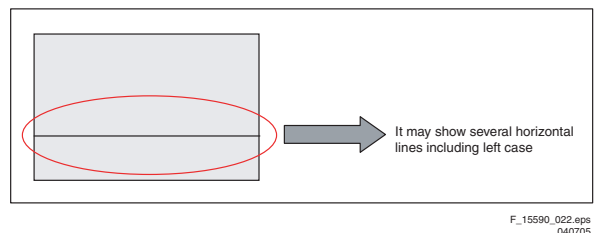


Figure 5-33 Screen display "Horizontal lines"

Low Brightness of Displayed Picture

- In this case, Z board operation is not complete.
- Check the power cord of Z board.
- Check the connector of Z board and CTRL board.
- Replace the CTRL board or Z board.

Partially Other Colour on Full White Screen or Partially Mis-Discharge on Full Black Screen.

- Check the Y board waveform, see below.
- Measure the output wave with an oscilloscope (> 200 MHz) and compare the waveform with the waveform in the figure below. Adjust the Y board Set-up voltage (Vsetup) and time-interval "A" by changing VR3 and VR2. Check if -Vy and Vscan have been set correctly with VRy and VRsc respectively, to the value indicated on the voltage label.
 - Measuring Point for "Vsetup" and time-interval "A": Test point "Waveform" on the Y-Driver board.
 - Measuring Points for "-Vy" and "Vscan": Test points "Vy" and "Vsc" on the Y-SUS board.

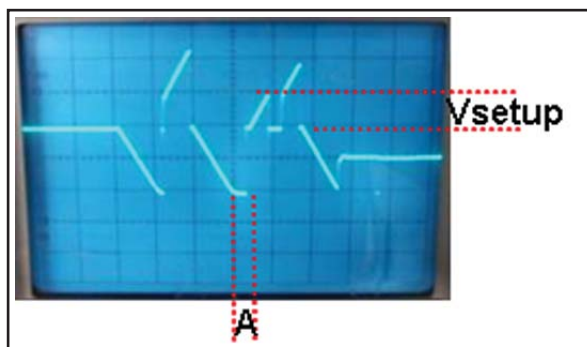
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020707

Figure 5-34 Y output voltage waveform

No Specified Brightness at Specified Colour

1. Check the connector of the CTRL board input signal (LVDS).
2. Replace the CTRL board.

5.2.3 Checking for Component Damage**Y IPM (IC 18) or Z IPM (IC 2)**

When the internal Sustain FET or ER FET of the Y IPM (IC18) or Z IPM (IC2) is damaged, there will be no picture, or the screen is partially mis-discharged.

- Test Points: Waveform-GND (Y-DRV board), B28-GND (Z board).
- Wave format: Waveform (Y-DRV board) or B28 (Z board) has no output wave.

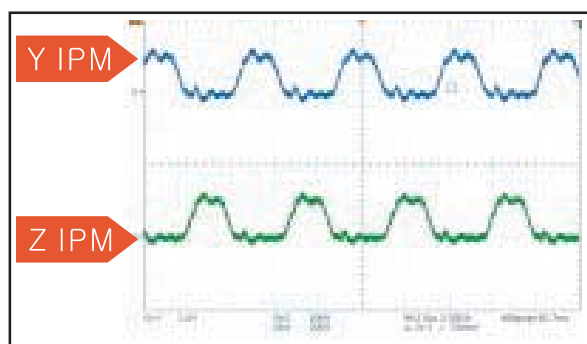
G_16390_049.eps
150806

Figure 5-35 IPM normal output

FET assay (Y board: HS2)

When the Set_up FET (2nd FFT of HS2) is damaged, there will be no picture.

- Test Point: GND-Waveform (Y-DRV board)
- Measuring condition: full white pattern.
- Wave format: as shown in the figure below.

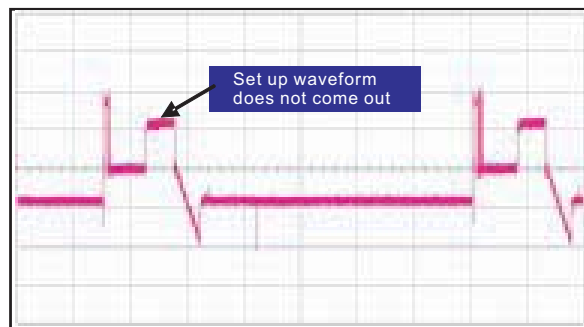
G_16390_050.eps
150806

Figure 5-36 Set up FET defective

When the Set_down FET/Pass_Top FET(1st, 3rd, 4th, 5th FFT of HS2) is damaged, mis-discharge of the entire screen is generated.

- Test Point: GND-Waveform (Y-DRV board)
- Wave format: as shown in the figure below.

G_16390_051.eps
150806

Figure 5-37 Set down FET defective

SCAN IC (Y-DRV board: IC1-10)

1. In case of the SCAN IC is damaged, one horizontal line may be open on the screen.
 - Test Point: ICT output - GND on the Y DRV board.
 - Wave format: As shown below figure.
2. When the SCAN IC is damaged (poor, external electricity, or spark), there might be no picture.
 - Test Point: ICT output - GND on the Y DRV board.
 - Wave format: Output wave format is not generated (you can see if which SCAN IC is damaged).
3. Overlap of two horizontal lines on the screen in case of shorted SCAN IC output.
 - Test Point: ICT output - GND on the Y DRV board.
 - Wave format: As shown in figures "SCAN IC shorted output" and "SCAN IC normal output".

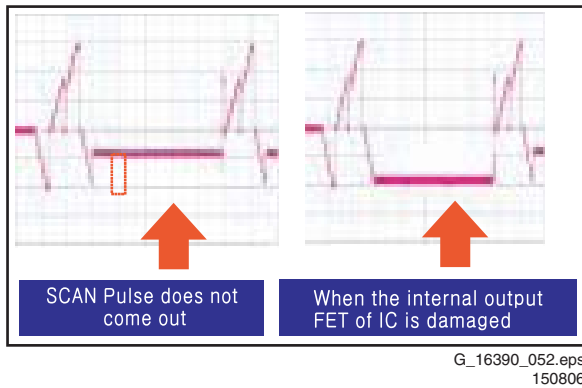


Figure 5-38 SCAN IC defective

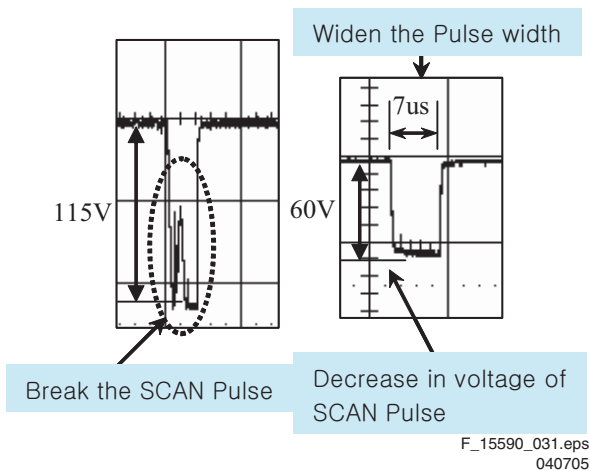


Figure 5-39 SCAN IC shorted output

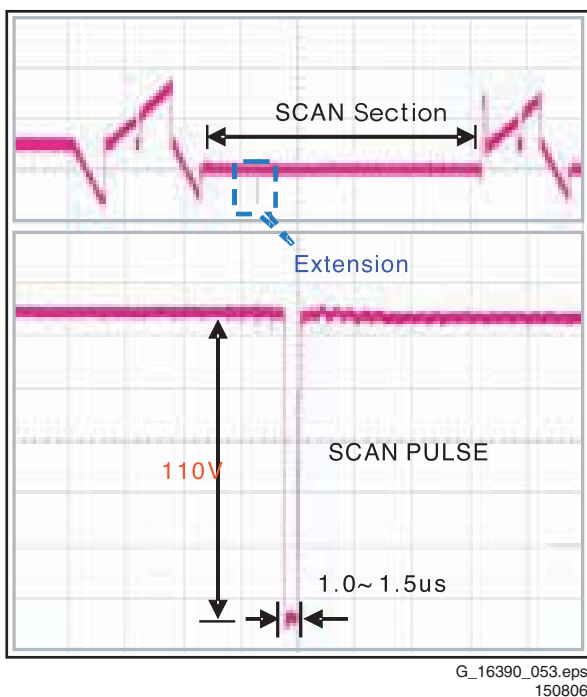


Figure 5-40 SCAN IC normal output wave

TCPs

1. In case of shorting or opening of TCP IC output, the screen may show one or several vertical lines.

- Test Point: Output TP of GND-TCP
 - Wave format: As shown in figure below. In case of normal wave output, when STB signal is generated, the output must maintain "HIGH". When STB signal is generated again, the output must fall to "LOW". But when the TCP IC is damaged, the STB signal is not generated, and the output falls to "LOW".
2. In case of IC damage, the screen may show no image on the corresponding part, or mis-discharge. In most cases you can see a burn mark on the IC.
 - Test Point: Output TP of GND-TCP
 - Wave format: No output wave.

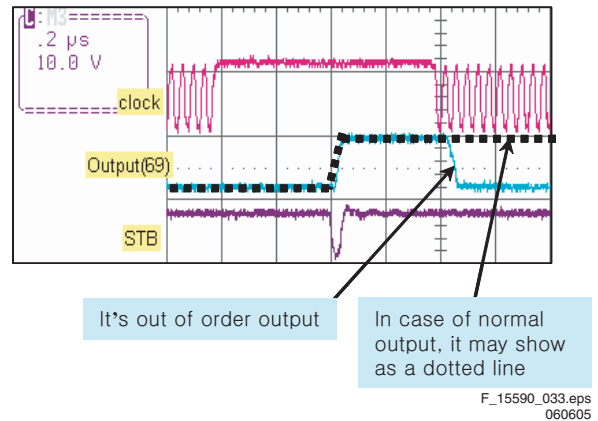


Figure 5-41 COF IC output defective

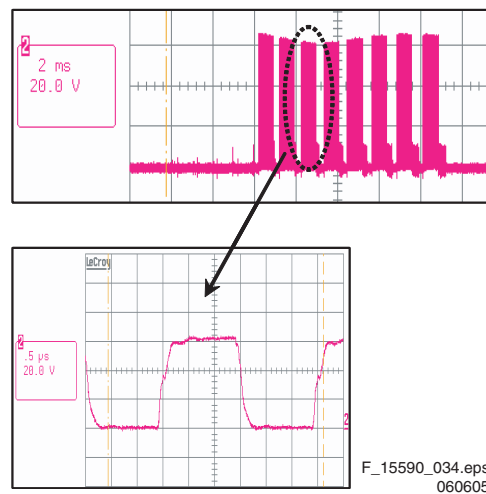
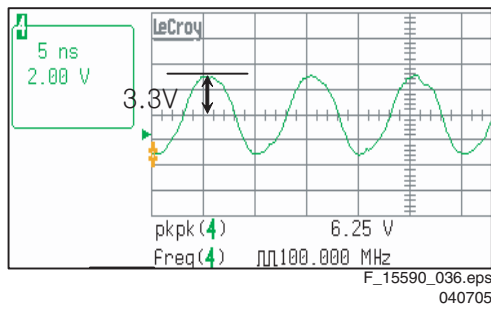
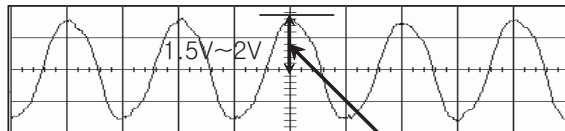


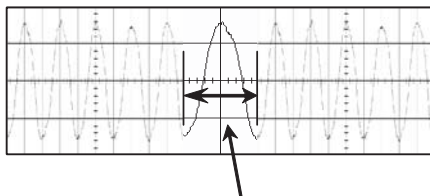
Figure 5-42 TCP normal output

Crystal (CTRL board: X1)

1. When a crystal is damaged, the screen is not shown.
 - Test Point: 3-pin of GND-Crystal (CTRL board: X1).
 - Wave format: Output wave is not generated.
2. In case of unusual start-up of the crystal, the screen may blink.
 - Wave format: As shown in figure below.
 - Measurement position: Measuring output 3-pin of crystal (CTRL board: X1).

**Figure 5-43 Crystal normal output**

Output voltage of the signal is low



It may change the frequency, suddenly

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060605

Figure 5-44 Crystal defective output

5.3 Defect Description Form

This form must be used by the workshops for warranty claims:

Defect Description Form LCD PLASMA v4.0 final					Date last modified: 28/03/2006	
To be filled in by <u>WORKSHOP / WORK CENTER</u>						
Country:		PHILIPS LCD & Plasma <u>DEFECT DESCRIPTION</u> <u>FORM</u>		Type nr./Model nr. set		
Customer Account nr.:				Serial nr. set		
Job sheet nr.:				Type nr. display		
				Serial nr. display		
				Part nr display (12nc)		
				Return number		
GENERAL REPAIR DATA	Condition	<input type="checkbox"/> Constantly <input type="checkbox"/> Intermittently <input type="checkbox"/> After a while			<input type="checkbox"/> In hot environment <input type="checkbox"/> In cold environment Other: <div></div>	
	Symptom(s)	<input type="checkbox"/> No backlight <input type="checkbox"/> No picture <input type="checkbox"/> Picture too bright <input type="checkbox"/> Scratches (LCD only acc. Pixel criteria sheet V4.0) <input type="checkbox"/> Only partial picture <input type="checkbox"/> Unstable picture			<input type="checkbox"/> Flickering / flashing picture <input type="checkbox"/> Lines across/down image <input type="checkbox"/> Inactive row(s) <input type="checkbox"/> Inactive column(s) <input type="checkbox"/> Missing colour(s) <input type="checkbox"/> Light leakage Other: <div></div>	
PANEL REPAIR	Pixel Defect(s):	Dark dots Bright dots	Qty of dots:	Mark Defect(s):		
	Symptoms	Following defect symptoms are out of warranty: <div> - Broken glass / Broken polarizer - Scratch(es) on display / polarizer </div> <div> - Number of dark/bright pixels within spec. - Burn in (Plasma TV) / Sticking image (LCD TV) - MURA </div>				These symptoms are not claimable.
BOARD REPAIR	Defect Board			New Board		
	Spare Part Nr.	Serial Nr.		Spare Part Nr.	Serial Nr.	
	1.					
	2.					
	3.					
4.						
Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected.						
Owner: PHILIPS CE EUROSERVICE						DE10WEG

Figure 5-45 Defect Description Form (DDF)

6. Block Diagrams, Test Point Overviews, and Waveforms

6.1 Block Diagram PDP Module

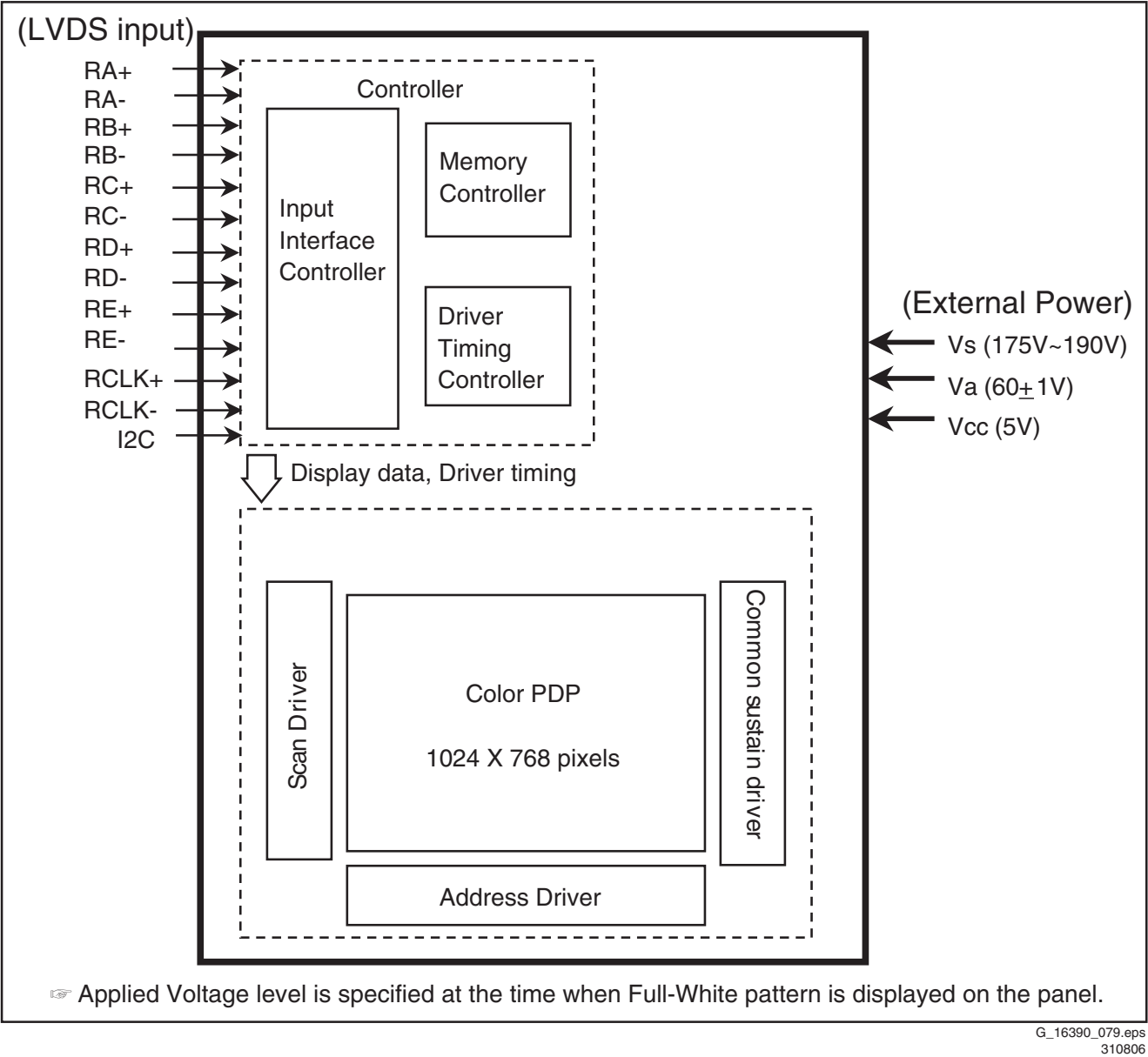


Figure 6-1 Block Diagram

7. Circuit Diagrams and PWB Layouts

Not applicable

8. Alignments

Index of this chapter:

- 8.1 General
- 8.2 Alignments
 - 8.2.1 Tools
 - 8.2.2 Connection Diagram and Set-Up
 - 8.2.4 Y-SUS Alignment

8.1 General

Notes:

- **Important:** if the PSU board, the Y-SUS board or the Z-SUS board is replaced, the technician should check if the voltages delivered by these boards are correct. If not, the boards should be realigned in order to avoid bad performance of the PDP.
- Allow the set to warm up according conditions below for at least 10 minutes before adjusting.
 - Service signal: 100% Full White.
 - Service DC voltage: $V_{cc}=5\text{ V}$, $V_a=60\text{ V}$, $V_s=180\text{ V}$.
 - DC/DC Pack voltage: $V_{sc}=120\text{ V}$, $V_{zb}=100\text{ V}$, $-V_y=-200\text{ V}$
 - Preliminaries environment: Temp ($25 \pm 5\text{ deg. C}$), Relative Humidity ($65 \pm 10\%$).
- Module adjustment should follow below sequence.
 1. First, set up the V_{sc} / $-V_y$ voltage ($V_{sc}=120\text{ V}$, $-V_y=-200\text{ V}$).
 2. Then, adjust the voltage waveform (refer to adjustment).

Caution: Do not leave a still image for more than 10 minutes (especially The Digital pattern or Cross Hatch Pattern which has clear gradation) on the display, because this will cause burn-in effects.

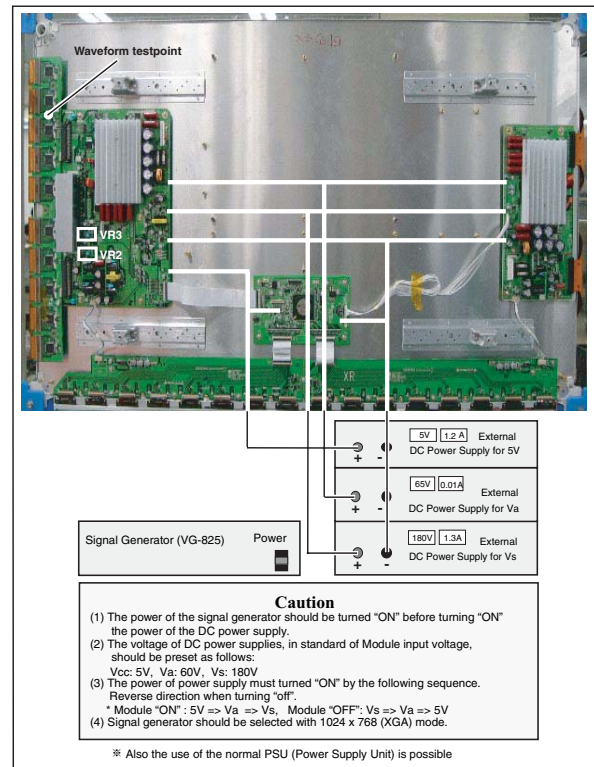


Figure 8-1 Measuring equipment connection diagram

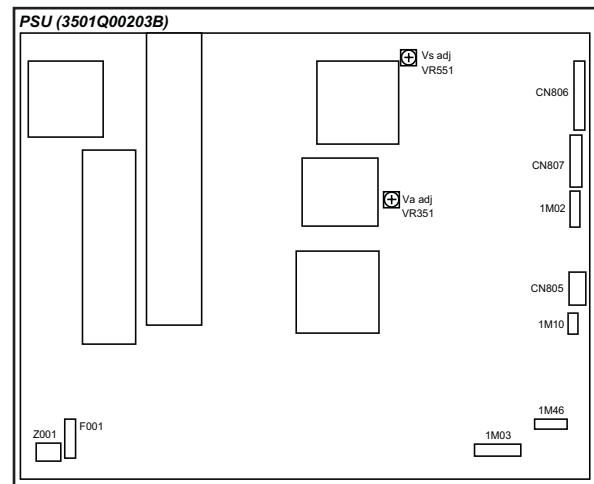
8.2 Alignments

8.2.1 Tools

- Digital oscilloscope: > 200 MHz.
- DVM (Digital Multimeter): Fluke 187 or similar.
- Signal generator: VG-828 or similar.
- DC power supply or PSU:
 - 1 DC power supply for V_s : 0 - 200 V, > 10 A.
 - 1 DC power supply for V_a : 0 - 100 V, > 5 A.
 - 1 DC power supply for 5V: 0 - 10 V, > 10 A.
 - A set of wires and appropriate connectors to hook up the power supplies to the display.
 - Required voltage stability of the power supplies: within $\pm 1\%$ for V_s and V_a , within $\pm 3\%$ for 5V.

8.2.2 Connection Diagram and Set-Up

1. For the connection diagram of the measuring instrument, refer to Fig. "Measuring equipment connection diagram".
2. Set-up the initial voltage $V_{cc}=5\text{ V}$, $V_a=60\text{ V}$, $V_s=180\text{ V}$. Note that the initial set-up voltage can be changed according to the module's characteristics (= the values on the voltage label).
3. Environmental conditions: temperature $25 \pm 5\text{ }^\circ\text{C}$, relative humidity $65 \pm 10\%$.



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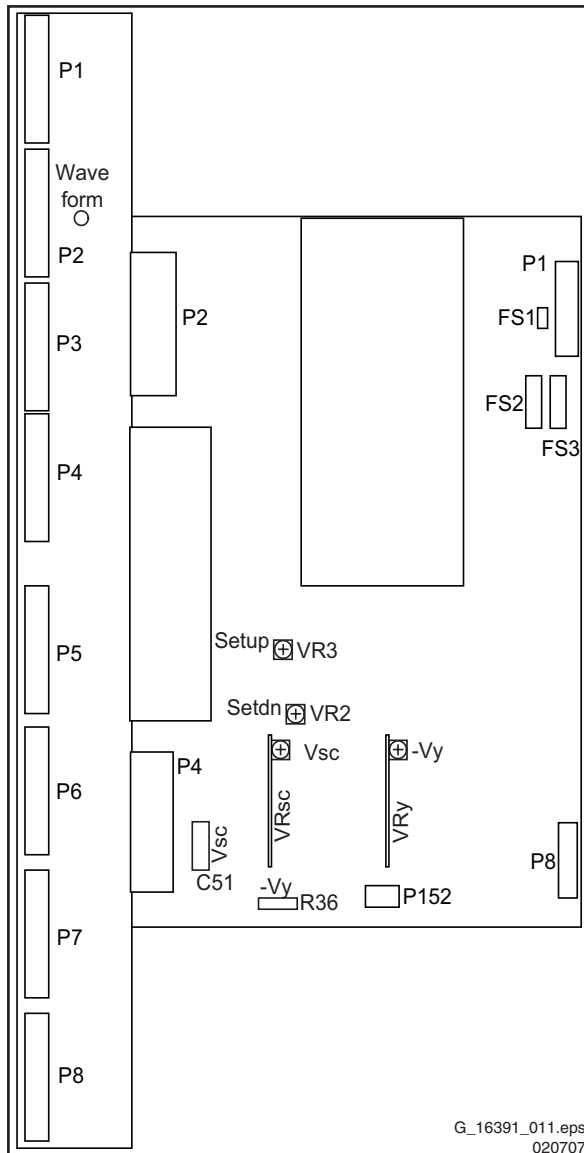
Figure 8-2 PSU Alignment

Vs Voltage Adjustment

1. Measure the V_s voltage (180...195 VDC) on pin 10 of CN806 on the PSU board (see Figure "PSU Alignment"). The voltage should have the same value as indicated on the label on the PSU.
2. If necessary, adjust V_s to its correct value with potentiometer VR551 on the PSU board.

Va Voltage Adjustment

1. Measure the Va voltage (55...65 VDC) on pin 1 of CN806 on the PSU board (see Figure "PSU Alignment"). The voltage should have the same value as indicated on the label on the PSU.
2. If necessary, adjust Va to its correct value with potentiometer VR351 on the PSU board.

8.2.4 Y-SUS Alignment**Figure 8-3 Y-SUS alignment****Condition**

- Set up a situation as shown in "Measuring equipment connection diagram".
- Check if the voltages Vs and Va of the PSU are correct (see PSU label and PSU Alignment 8.2.3).

Vscan Voltage Adjustment

1. Measure the Vscan voltage across C51 (or on the "Vsc" test point on the right of connector P4) on the Y-SUS board (see Figure "Y-SUS Alignment").
2. Adjust Vsc to the value indicated on the voltage sticker with potentiometer VRsc on the Y-SUS board.

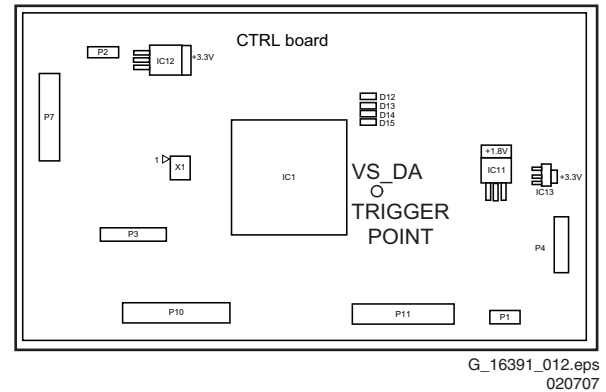
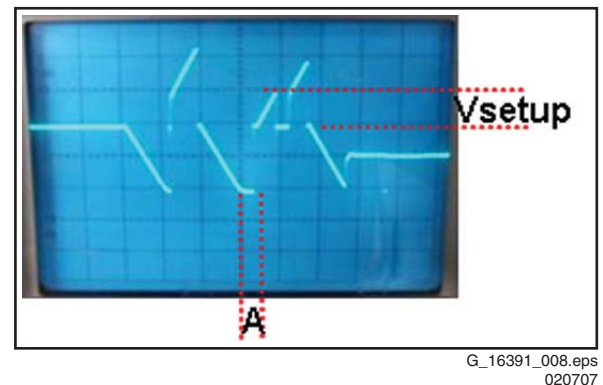
-Vy Voltage Adjustment

1. Measure the Vy voltage across R36 (or on the "Vy" test point on the DC converter) on the Y-SUS board (see Figure "Y-SUS Alignment").

2. Adjust -Vy to the value indicated on the voltage sticker with potentiometer VRy on the Y-SUS board.

Y-SUS Set-up Voltage Waveform Adjustment

Now connect the oscilloscope between the Waveform test point on the Y-Driver board and GND (see Figure "Y-SUS Alignment"). Trigger with Vs-DA on the Control board (see Figure "Trigger point Vs-DA").

**Figure 8-4 Trigger point Vs-DA****Figure 8-5 V set-up waveform**

1. Refer to Figure "V set-up waveform".
2. Adjust Vsetup to 150 ± 1 V with potentiometer VR3/Setup on the Y-SUS board (see Figure "Y-SUS Alignment").
3. Adjust the duration of time-interval "A" to 10 ± 5 μ sec with potentiometer VR2/Setdown on the Y-SUS board.

8.2.5 Z-SUS Alignment

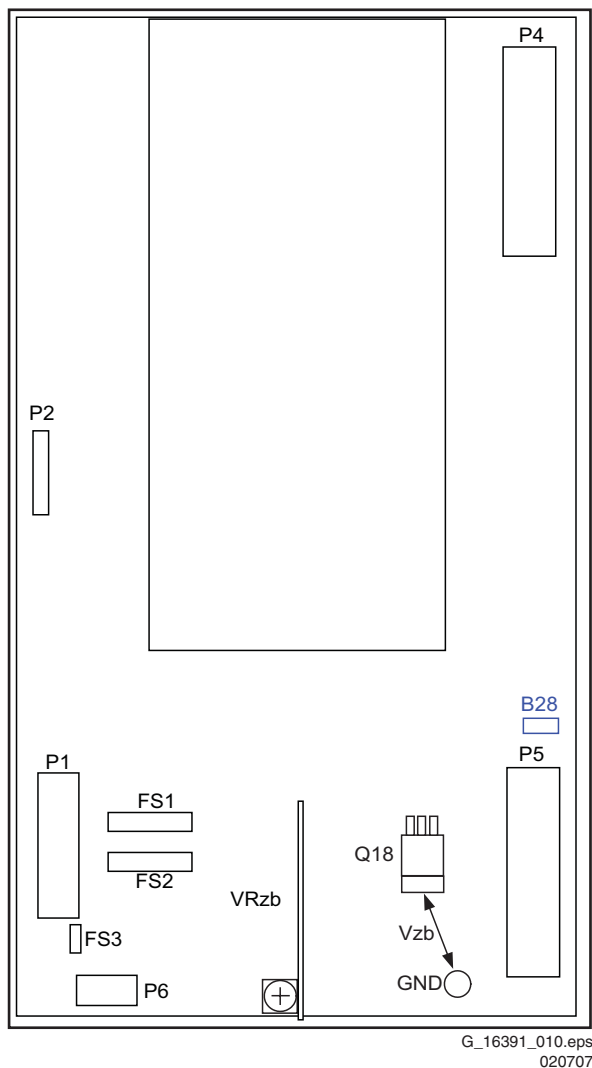


Figure 8-6 Z-SUS alignment

Condition

- Set up a situation as shown in "Measuring equipment connection diagram".
- Check if the voltages V_s and V_a of the PSU are correct (see PSU label and PSU Alignment 8.2.3).

Vzb (Z bias) Voltage Adjustment

1. Measure the voltage between the Vzb test point (the drain of Q18) and GND on the Z-SUS board (see Figure "Z-SUS Alignment").
2. Adjust Vzb to 100 ± 0.5 V with potentiometer VRzb on the Z-SUS board.

8.2.6 Internal Test Patterns

The CTRL board is capable of generating its own video test patterns. To generate the test patterns, do as follows:

- Disconnect the mains cord.
- Disconnect the SSB of the TV set, by removing the cables of connectors 1M03 and 1M46 on the PSU.
- Reconnect the mains cord.
- Connect pins 1 & 2 or pins 3 & 4 of Connector P1 on the Control Board (see Figure below) to each other.
- Now the internal test patterns are automatically shown in a loop.

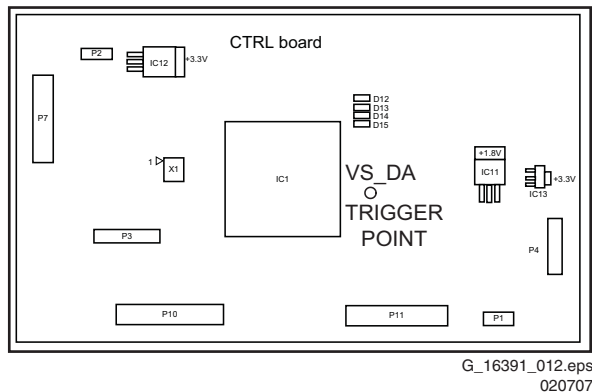


Figure 8-7 P1: Connector for Internal Test Patterns

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

- 9.1 Introduction
- 9.2 Power Supply Unit (PSU)
- 9.3 Control Board
- 9.4 X Board
- 9.5 Y Sustain Board
- 9.6 Y Drive Board
- 9.7 Z Sustain Board
- 9.8 DC/DC Converter Part
- 9.9 FPC (Flexible Printed Circuit)
- 9.10 FFC (Flat Flexible Cable)
- 9.11 TCP (Tape Carrier Package)
- 9.12 IPM (Intelligent Power Modules)
- 9.13 Abbreviation List
- 9.14 IC Data Sheets

9.1 Introduction

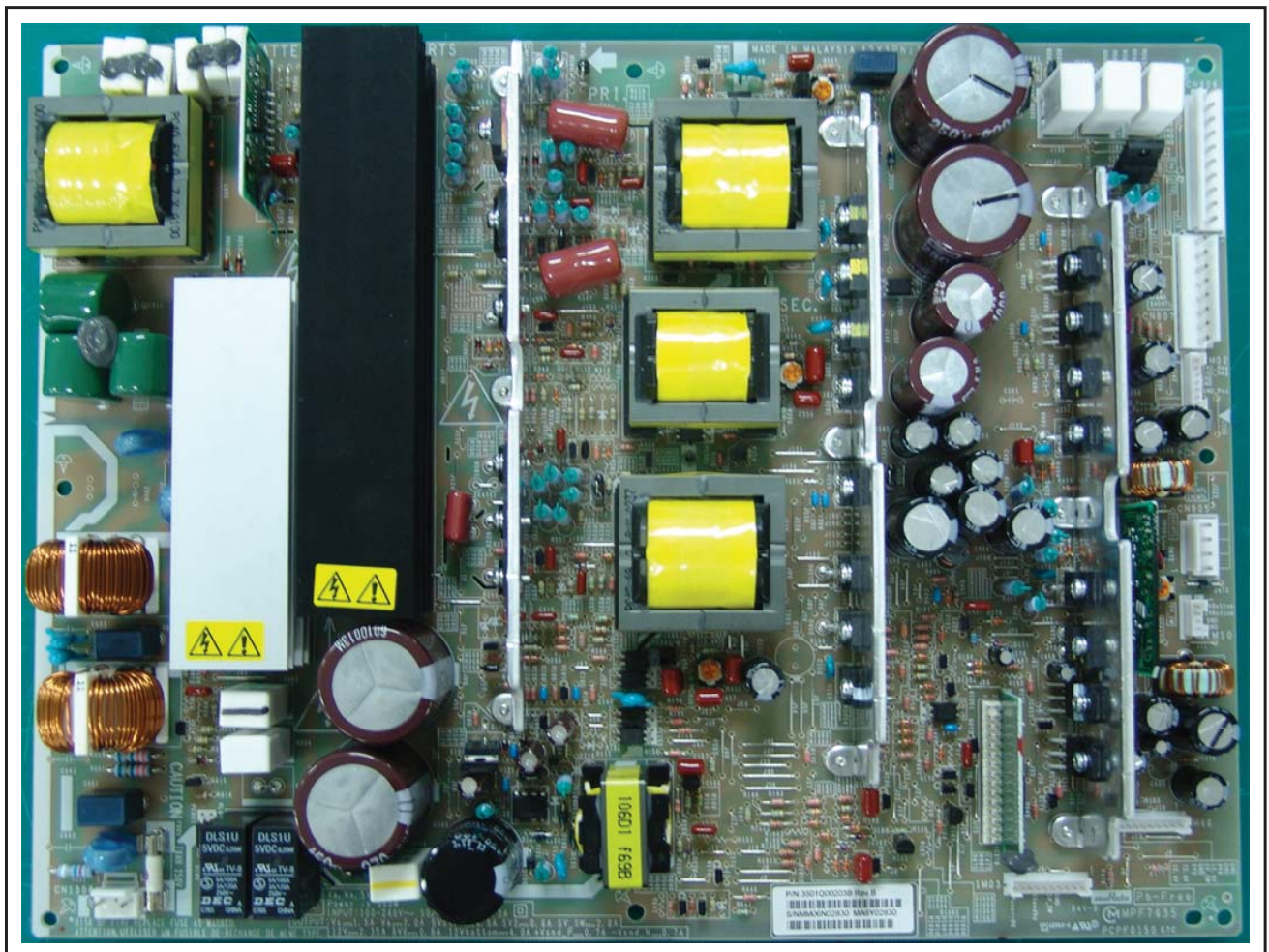
The 42X3* panel is LGE's HD successor for the year 2007 of the 42V7* panel.

9.2 Power Supply Unit (PSU)

9.2.1 Purpose

- To convert an input voltage of 100 ~ 240 Volt AC to voltages that the different boards and the panel need.
- Output voltages: Vcc (5 V), Vs (180 ~ 200 V), and Va (60 ~ 65 V), all DC.
- The PSU switches "OFF" automatically, when it detects errors like short circuits.

Warning: Voltages on the PSU reach 390 Volt maximum, so be very careful when handling it!



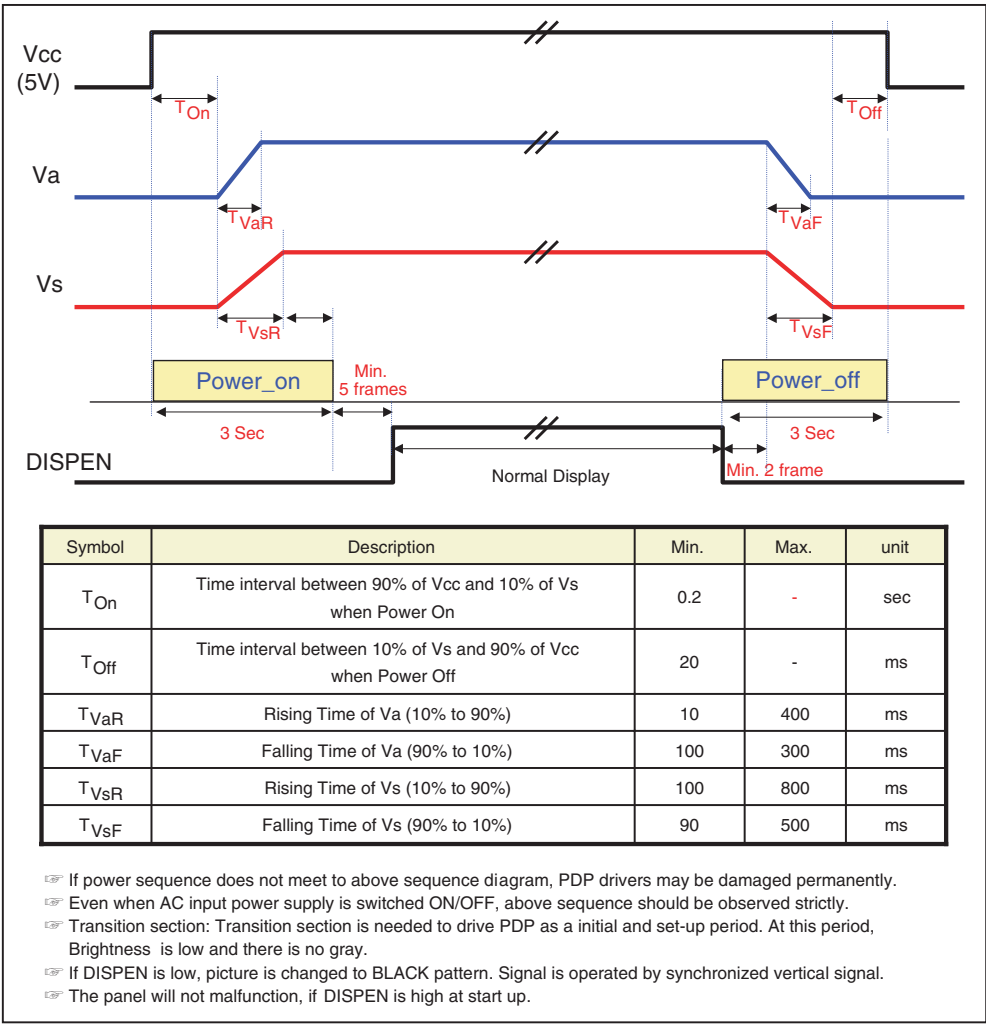
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020707

Figure 9-1 Power supply

9.2.2 Power ON and Power OFF Sequence

- For a correct functioning of the display, the different supply voltages have to be powered up and down according to a

certain sequence. This sequence is shown in the following figure.



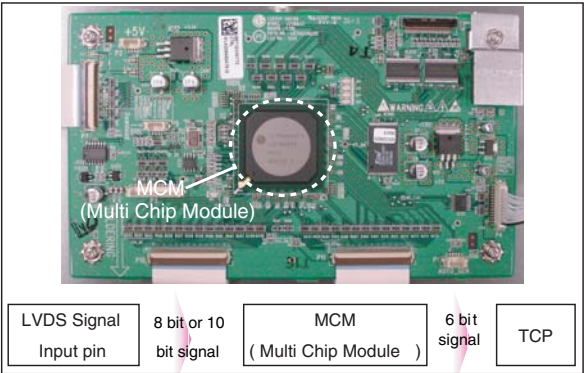
G_16390_080.eps
310806

Figure 9-2 Power supply sequence

9.3 Control Board

9.3.1 Purpose

Creates signal processing, and controls many FETs on each DRIVER board with R, G, and B signals.



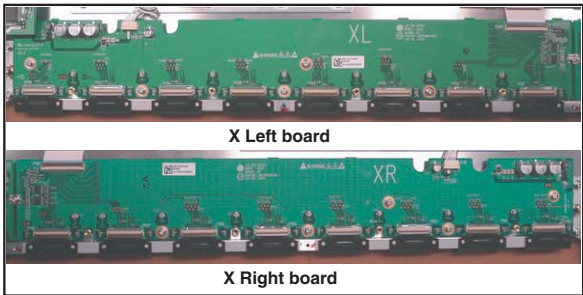
G_16390_035.eps
100806

Figure 9-3 Control board

9.4 X Board

9.4.1 Purpose

Receives LOGIC signal from the CONTROL board and makes the ADDRESS PULSE (generates Address discharge) by ON/OFF operation, and then supplies this waveform to TCP (data).



G_16390_083.eps
010906

Figure 9-4 X boards

9.5 Y Sustain Board

9.5.1 Purpose

Generates Sustain waveform, Reset, Vsc (Scan) and -Vy voltages, and supplies them to the Y DRIVE board.

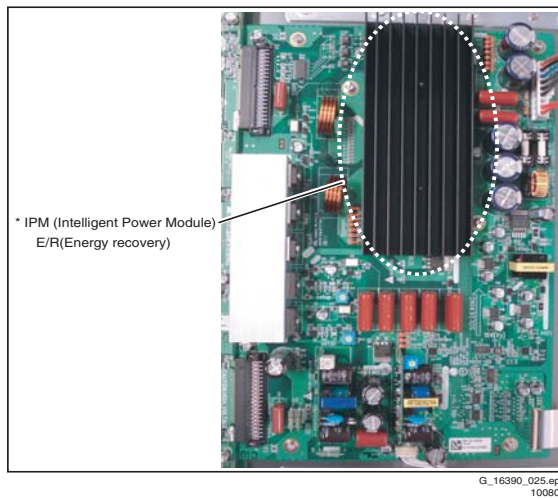


Figure 9-5 Y Sustain board

9.5.2 Main Components

IPM, diodes, electrolytic capacitors, and FETs.

9.6 Y Drive Board

9.6.1 Purpose

- To supply Sustain, Reset waveform, made by the Y-SUS board, to the PDP through the SCAN DRIVER IC.
- To supply a waveform that selects the horizontal electrodes (Y SUSTAIN electrodes) sequentially.
 - Potential difference is 0 V between GND and Vpp of the DRIVER IC during the SUSTAIN period.
 - Generates a potential difference between GND and Vpp only during the SCAN period.

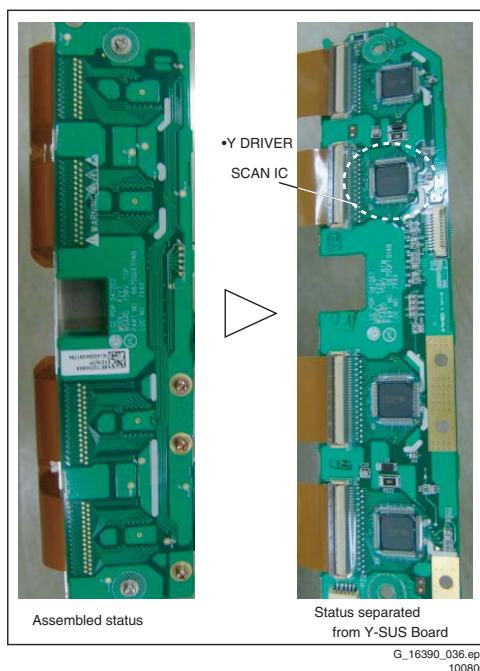


Figure 9-6 Y Drive board

9.7 Z Sustain Board

9.7.1 Purpose

To make the SUSTAIN and ERASE pulses that generate SUSTAIN discharge in the panel by receiving LOGIC signal from CONTROL board. This waveform is then supplied to the panel through FPC (Z).

9.7.2 Main Components

IPM, FET, DIODE, electrolytic capacitor, and E/R coil.

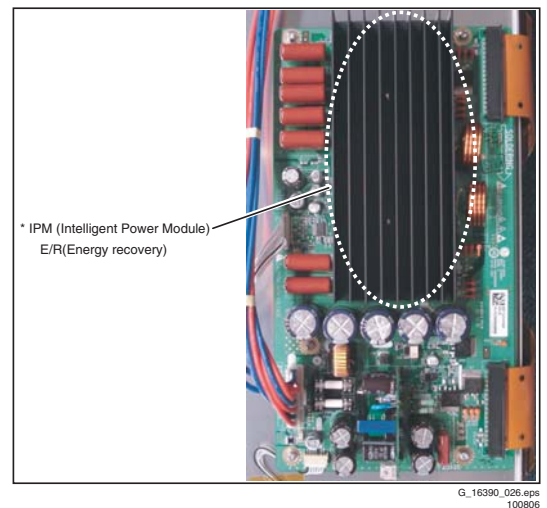


Figure 9-7 Z Sustain Board

9.8 DC/DC Converter Part

9.8.1 Purpose

From 5V, Vs, and Va (from the PSU), the DC/DC converter makes 5V, 15V, Vy, Vsc, 5Vf, and Va, which are essential for each board.

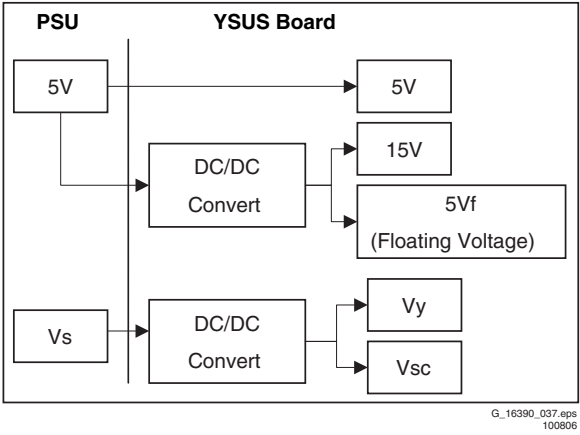


Figure 9-8 DC/DC Converter block diagram

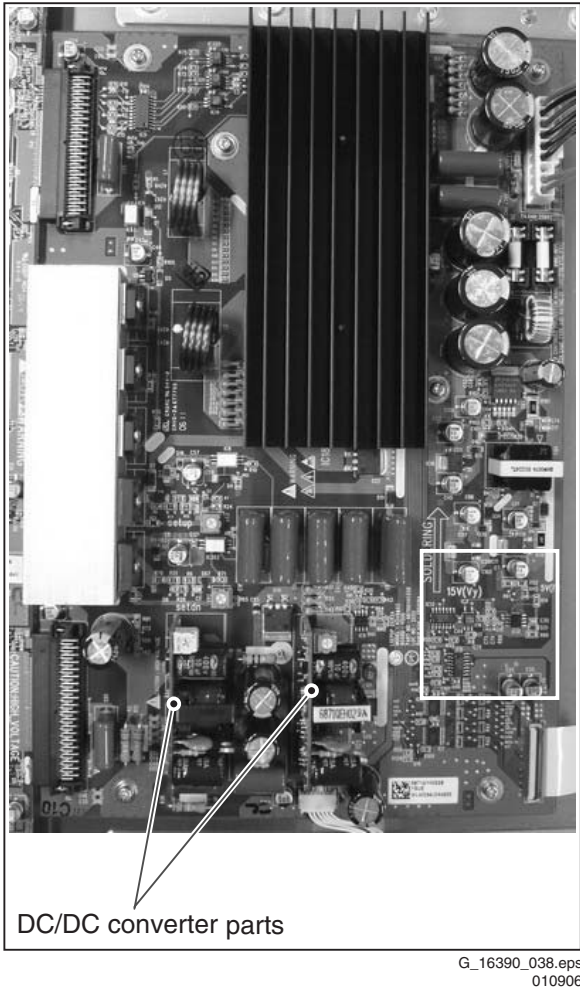


Figure 9-9 DC/DC Converter part

9.9 FPC (Flexible Printed Circuit)

9.9.1 Purpose

To supply a driving waveform to the PDP by connecting a PAD electrode of the PDP with a PWB (Y and Z boards).

- There are two types of this for the Y board: One is single-sided, the other double-sided (these have a pattern on it).
- For Z board there is no pattern, single-sided, and Beta type (all of copper surface).

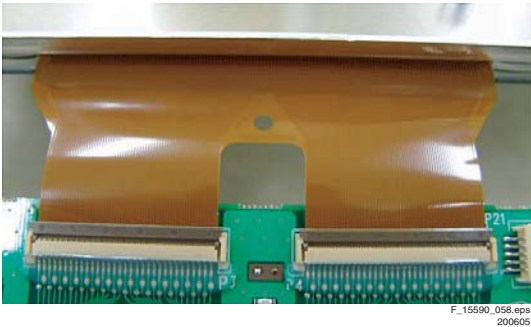


Figure 9-10 Flexible Printed Circuit

9.10 FFC (Flat Flexible Cable)

9.10.1 Purpose

For connecting LOGIC signals between boards. There are two types

- 0.5 mm pitch, 50-pin type.
- 1.0 mm pitch, 30-pin type.

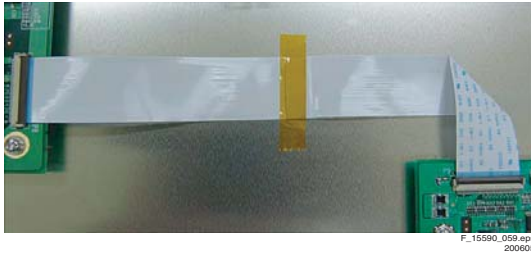


Figure 9-11 Flat Flexible Cable

9.11 TCP (Tape Carrier Package)

9.11.1 Purpose

To supply a 6-bit RGB signal to the panel, by connecting a PAD electrode of the panel with the X board.



Figure 9-12 Tape Carrier Package

9.12 IPM (Intelligent Power Modules)

9.12.1 Purpose

- Attached to Y board (SUS IPM) and Z board (ER IPM):
- SUS IPM generates the Sustain waveform
 - ER IPM performs an Energy Recovery function

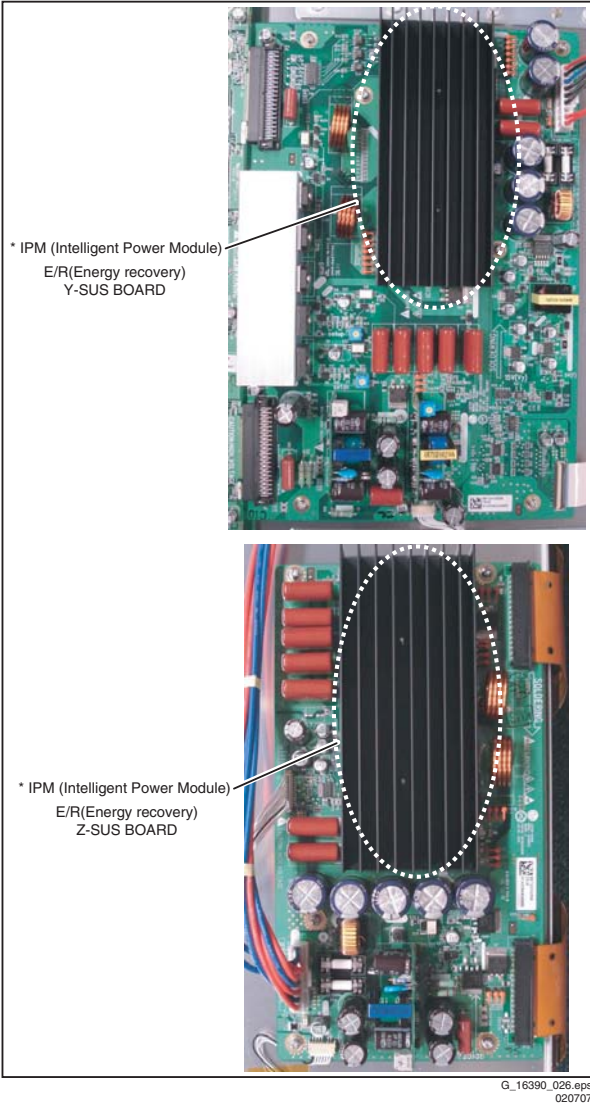


Figure 9-13 Intelligent Power Modules

9.12.2 Main Components

Heatsink, capacitor, diode, IC, resistor, transistor, and FET.

9.13 Abbreviation List

AC	Alternating Current
B/D	Board
CLK	Clock signal
COF	Chip On Flex / Foil / Film
CTRL	Control (board)
DC	Direct Current
FET	Field Effect Transistor
FPC	Flexible Printed Circuit
I/O	Input/Output
IC	Integrated Circuit
IPM	Intelligent Power Module
LED	Light Emitting Diode
LGE	Lucky Goldstar Electronics (supplier)
MCM	Multi Chip Module
PCB	Printed Circuit Board (same as PWB)
PDP	Plasma Display Panel
PFC	Power Factor Corrector circuit
PSU	Power Supply Unit
PWB	Printed Wiring Board (same as PCB)
RGB	Red, Green, Blue colour space
STB	Stand-by signal
TCP	Tape Carrier Package

9.14 IC Data Sheets

Not applicable

10. Spare Parts List

Please refer to the Philips Service website, for an actual overview (monthly updated).

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- References in text and graphics to PSU model 3501Q00201A (not used in this PDP model) changed to references to PSU model 3501Q00203B.
- Corrections in texts referring to the PSU, Y-SUS and Z-SUS boards.

Manual xxxx xxx xxxx.2

- Text on how to generate Internal Test Patterns added to Chapter 8, Alignments.
- Minor text corrections added.

Service Service Service

SDI PDP Repair Manual

S37SD-YD02 (37-inch SD v4)

S42SD-YD05, YD06, YD07 (42-inch SD v2, v3, v4)

S42AX-XD02, YD01 (42-inch HD v3, v4)

S50HW-XD03, XD04 (50-inch HD v3, v4)

Service Manual

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1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

- 1.1 PDP Overview
- 1.2 Serial Numbers
- 1.3 Chassis Overview

Notes:

- Figures can deviate due to the different model executions.
- Specifications are indicative (subject to change).

1.1 PDP Overview

Table 1-1 PDP overview

	PDP Type/Version	Model Name	H x V Pixel
1	37" SD v4	S37SD-YD02	852 x 480
2	42" SD v2	S42SD-YD06	852 x 480
3	42" SD v3	S42SD-YD05	852 x 480
4	42" SD v4	S42SD-YD07	852 x 480
5	42" HD v3	S42AX-XD02	1024 x 768
6	42" HD v4	S42AX-YD01	1024 x 768
7	50" HD v3	S50HW-XD03	1366 x 768
8	50" HD v4	S50HW-XD04	1366 x 768

Table 1-2 PDP vs Chassis overview

Display type	Model #	Chassis	Chassis Manual #
37" SD v4	37PF9936/37	LC4.7U	3122 785 14742
37" SD v4	37PF9946/12	LC4.7E	3122 785 14722
37" SD v4	37PF9946/69	LC4.7A	3122 785 14761
42" SD v2	420P20/00	FM242	3122 785 14130
42" SD v2	42FD9925/01	FM242	3122 785 14130
42" SD v2	42FD9935/17	FM242	3122 785 14130
42" SD v2	42FD9935/93S	FM242	3122 785 14130
42" SD v2	42FD9945/01	FM242	3122 785 14130
42" SD v2	42FD9953/17, /69, /93	FM242	3122 785 14130
42" SD v2	42HF9953/12Z	FM24_AB	3122 785 13890
42" SD v2	42PF9936/37	FTP1.1U	3122 785 14381
42" SD v2	42PF9945/12	FTP1.1E	3122 785 14370
42" SD v2	42PF9945/69, /79, /98	FTP1.1U	3122 785 14381
42" SD v2	42PF9955/12	F21RE	3122 785 13890
42" SD v3	42PF9936D/37	LC4.7U	3122 785 14742
42" SD v3	42PF9946/12	LC4.7E	3122 785 14722
42" SD v3	42PF9946/79, /93, /98	LC4.7A	3122 785 14761
42" SD v3	42PF9956/12	FTP2.2E	3122 785 14651
42" SD v3	42PF9956/93	FTP2.2A	3122 785 14680
42" SD v4	42PF7320/10	LC4.9E	3122 785 15431
42" SD v4	42PF7320/79, /98	LC4.9A	3122 785 15450
42" HD v3	42PF9966/37	FTP2.2U	3122 785 14662
42" HD v3	42PF9966/79, /93, /98	FTP2.2A	3122 785 14680
42" HD v3	42PF9976/37	FTP2.2U	3122 785 14662
42" HD v4	42HF7543/37	BP2.3HU	3122 785 15900
42" HD v4	42PF7320A/37	BP2.3U	3122 785 15541
42" HD v4	42PF7520D/10	LC4.9E_AB	3122 785 15670
42" HD v4	42PF9630/78	FTP2.4L	3122 785 15470
42" HD v4	42PF9630A/37	BP2.2U	3122 785 15541
42" HD v4	42PF9630A/96	BP2.2U	3122 785 15541
42" HD v4	42PF9966/79, /98	FTP2.4A	3122 785 15470
50" HD v3	50PF9956/37	FTP2.2U	3122 785 14662
50" HD v3	50PF9966/12	FTP2.2E	3122 785 14651
50" HD v3	50PF9966/37	FTP2.2U	3122 785 14662
50" HD v3	50PF9966/69, /93	FTP2.2A	3122 785 14680
50" HD v4	50HF7543/37	BP2.3HU	3122 785 15900
50" HD v4	50PF7320/10	LC4.9E	3122 785 15431
50" HD v4	50PF7320/79, /93, /98	LC4.9A	3122 785 15450
50" HD v4	50PF9630/78	LC4.9L	3122 785 15450
50" HD v4	50PF9630A/96	BP2.2U	3122 785 15541
50" HD v4	50PF9830A/37	BP2.1U	3122 785 15541
50" HD v4	50PF9966/79	FTP2.4A	3122 785 15470
50" HD v4	50PF9967D/10	FTP2.4E_AB	3122 785 15740

In above table the link is given between the SDI Plasma Display Panel and the Philips TV chassis (incl. chassis manual no.).

1.1.1 37" SD v4

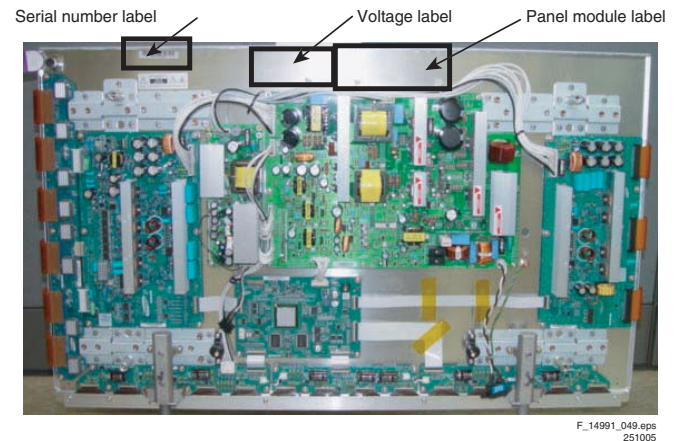


Figure 1-1 External view (37" SD v4)

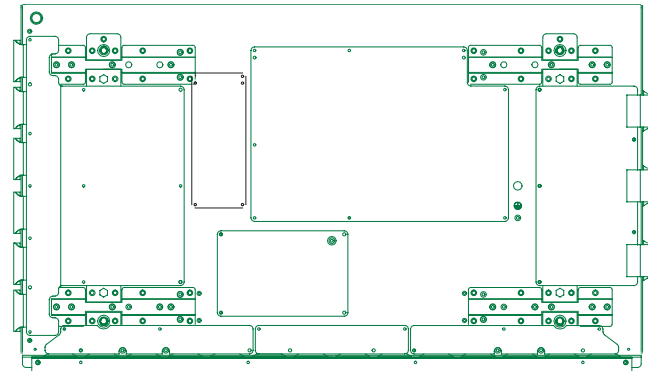


Figure 1-2 Points of screw mount (37" SD v4)

No	Item	Specification 37" SD v4	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	0.960 mm (H) x 0.960 mm (V)	
4	Cell Pitch	R	0.320 (H) mm 0.960 (V) mm
		G	0.320 (H) mm 0.960 (V) mm
		B	0.320 (H) mm 0.960 (V) mm
5	Display size	817.92 (H) x 460.80 mm (V)	
6	Screen size	Diagonal 37" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 15.5 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.2 42" SD v2

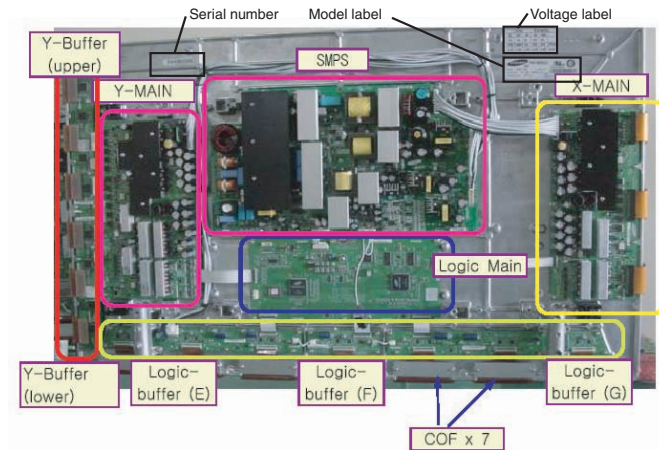


Figure 1-3 External view (42" SD v2)

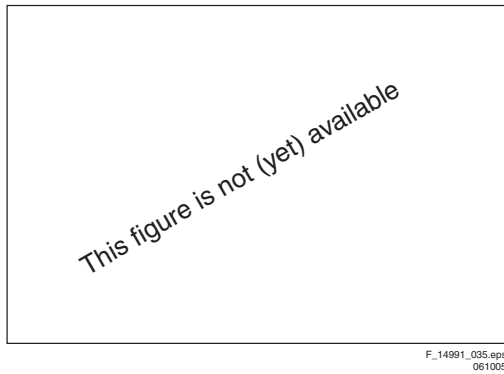


Figure 1-4 Points of screw mount (42" SD v2)

No	Item	Specification 42" SD v2	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 mm (H) x 1.110 mm (V)	
4	Cell Pitch	R	0.324 (H) mm 1.110 (V) mm
		G	0.365 (H) mm 1.110 (V) mm
		B	0.406 (H) mm 1.110 (V) mm
5	Display size	932.940 (H) x 532.800(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 16.6 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.3 42" SD v3

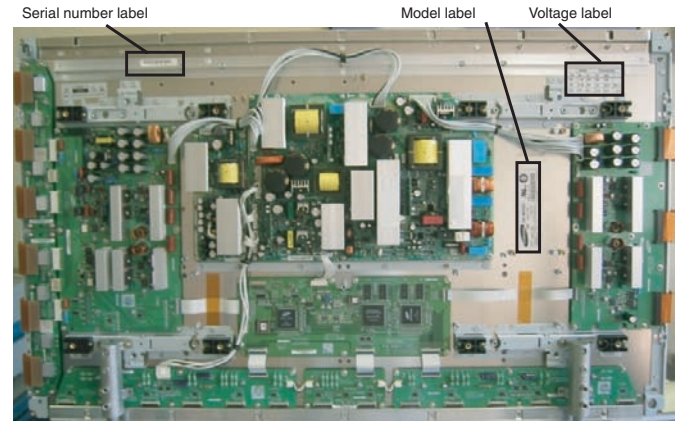


Figure 1-5 External view (42" SD v3)

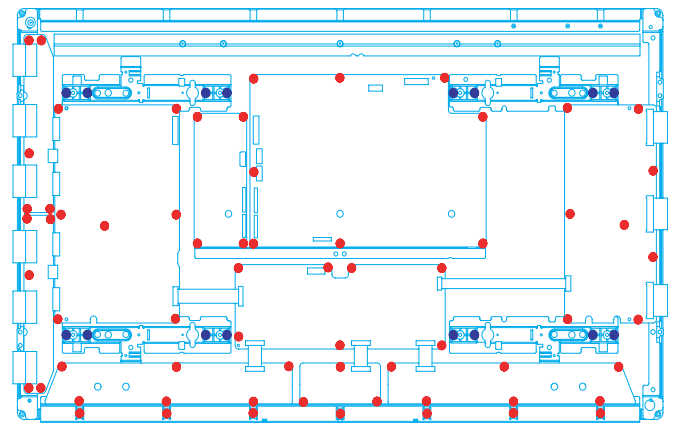


Figure 1-6 Points of screw mount (42" SD v3)

No	Item	Specification 42" SD v3	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 mm (H) x 1.110 mm (V)	
4	Cell Pitch	R	0.365 (H) mm 1.110 (V) mm
		G	0.365 (H) mm 1.110 (V) mm
		B	0.365 (H) mm 1.110 (V) mm
5	Display size	932.940 (H) x 532.800(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 16.6 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.4 42" SD v4

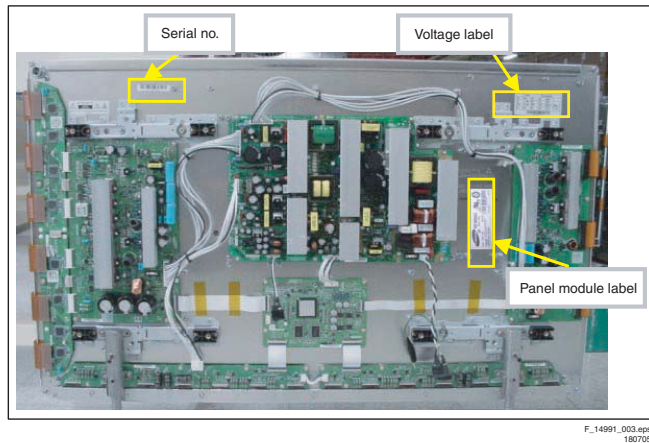


Figure 1-7 External view (42" SD v4)

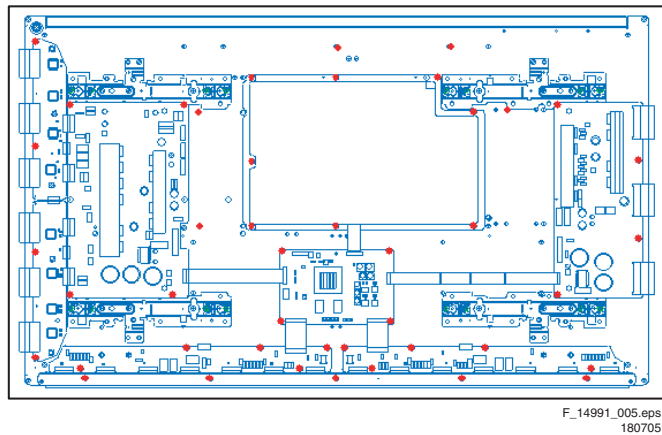


Figure 1-8 Points of screw mount (42" SD v4)

No	Item	Specification 42" SD v4
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	2556 (H) x 480 (V)
3	Pixel Pitch	1.095 (H) mm x 1.110 (V) mm
4	Cell Pitch	R 0.365 (H) mm x 1.110 (V) mm G 0.365 (H) mm x 1.110 (V) mm B 0.365 (H) mm x 1.110 (V) mm
5	Display size	932.940 (H) x 532.800(V) mm
6	Screen size	Diagonal 42" Colour Plasma Display Module
7	Screen aspect	16:9
8	Display colour	16.77 million colours
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)
10	Dimensions	982 (W) x 582 (H) x 54 (D) mm
11	Weight	Module 1 About 15.4 kg
14	Broadc. reception Vertical frequency Video/Logic Interface	60 Hz/ 50 Hz, LVDS

1.1.5 42" HD v3

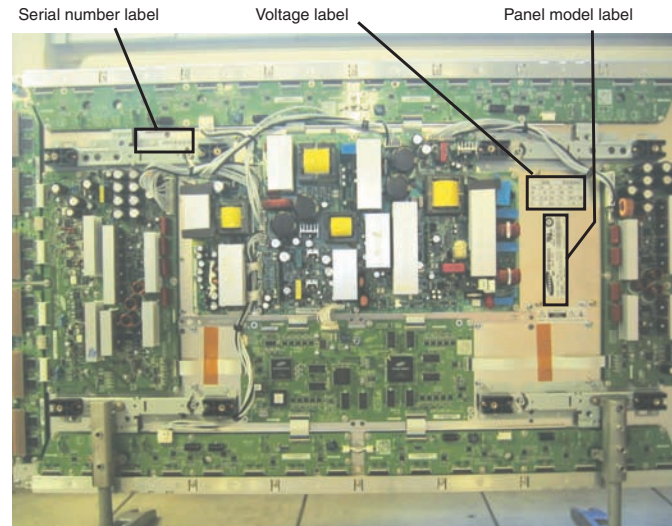


Figure 1-9 External view (42" HD v3)

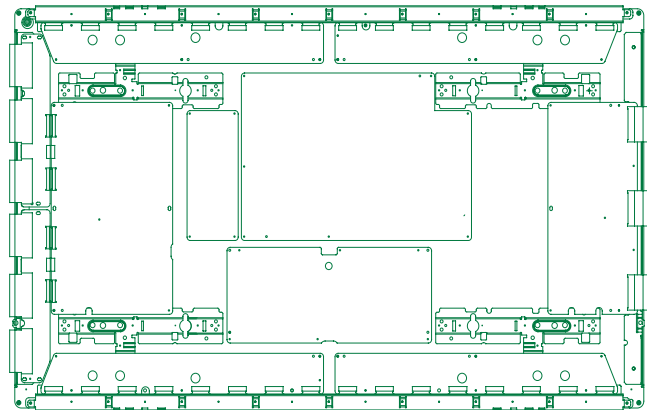


Figure 1-10 Points of screw mount (42" HD v3)

No	Item	Specification 42" HD v3
1	Pixel	1.024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)
2	Number of Cells	3072 (H) x 768 (V)
3	Pixel Pitch	0.912mm (H) x 0.693mm (V)
4	Cell Pitch	R Horizontal 0.304 mm Vertical 0.693 mm G Horizontal 0.304 mm Vertical 0.693 mm B Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	932.940 (H) x 532.800(V) mm
6	Screen size	Diagonal 42" Colour Plasma Display Module
7	Screen aspect	16:9
8	Display colour	16.77 million colours
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm
11	Weight	Module 1 About 18.0 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS

1.1.6 42" HD v4

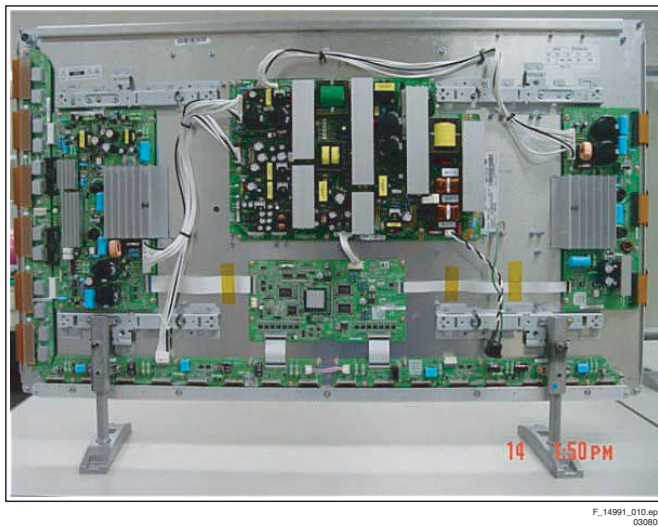


Figure 1-11 External view (42" HD v4)

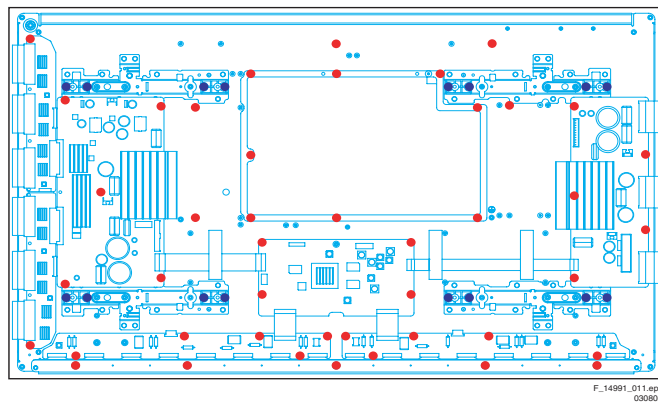


Figure 1-12 Points of screw mount (42" HD v4)

No	Item	Specification 42" HD v4	
1	Pixel	1.024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)	
3	Pixel Pitch	0.912mm (H) x 1.110mm (V)	
4	Cell Pitch	R	Horizontal 0.304 mm Vertical 0.693 mm
		G	Horizontal 0.304 mm Vertical 0.693 mm
		B	Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	933.98 (H) x 532.220(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours (8-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1000 (W) x 598 (H) x 64.4 (D) mm	
11	Weight	Module 1	About 20.0 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.7 50" HD v3

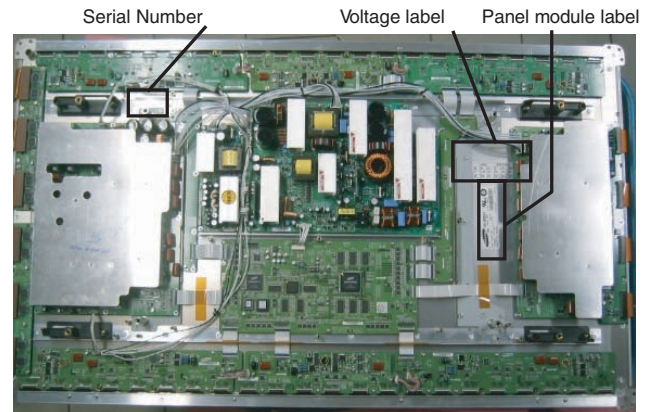


Figure 1-13 External view (50" HD v3)

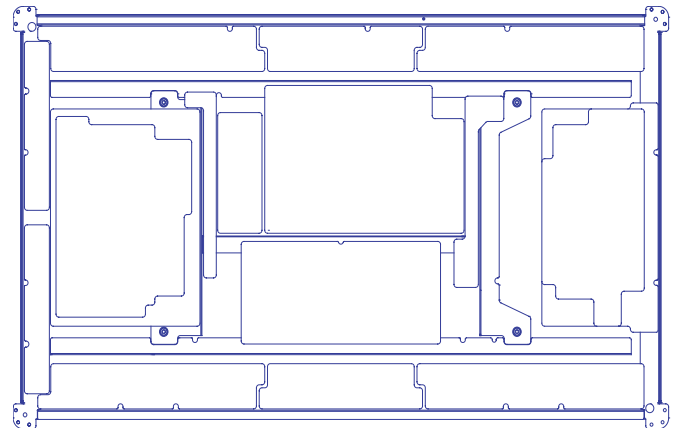


Figure 1-14 Points of screw mount (50" HD v3)

No	Item	Specification 50" HD v3	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	0.810mm (H) mm x 0.810 mm (V)	
4	Cell Pitch	R	Horizontal 0.270mm Vertical 0.810mm
		G	Horizontal 0.270mm Vertical 0.810mm
		B	Horizontal 0.270mm Vertical 0.810mm
5	Display size	1106.46 mm (H) x 622.08 mm (H)	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1184 (W) x 700 (H) x 60.1 (D) mm	
11	Weight	Module 1	About 18.0 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.8 50" HD v4

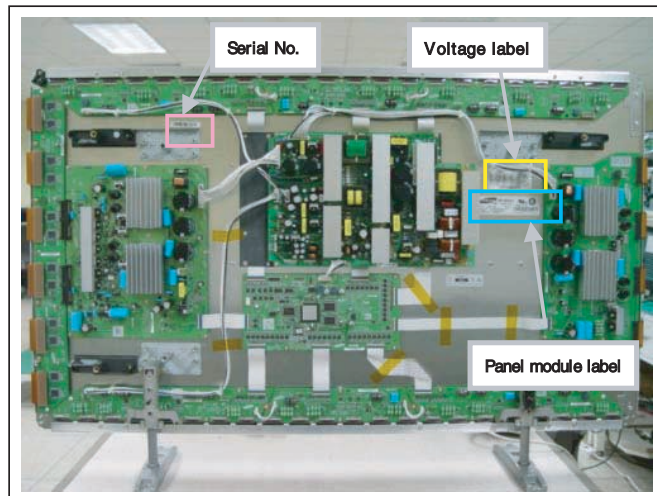
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Figure 1-15 External view (50" HD v4)

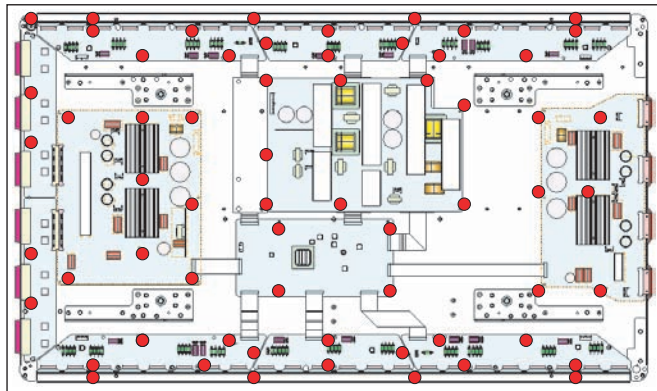
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Figure 1-16 Points of screw mount (50" HD v4)

No	Item	Specification 50" HD v4	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	0.810mm (H) mm x 0.810 mm (V)	
4	Cell Pitch	R	Horizontal 0.270mm Vertical 0.810mm
		G	Horizontal 0.270mm Vertical 0.810mm
		B	Horizontal 0.270mm Vertical 0.810mm
5	Display size	1106.46 mm (H) x 622.08 mm (H)	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1175 (W) x 682 (H) x 65.5 (D) mm	
11	Weight	Module 1	About 25.4 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.2 Serial Numbers

Class	14 digits							
ID Type	C	001	A	4	9	03	A	0001
	Area	Model	Module Line	Year	Month	Date	Worker Group	S/N
ID Meaning	① Area (C: Cheonan, S : Shenzhen) ② Model : 3 digit ③ Module Line : A ~ Z ④ Year : 1 Digit ⇒ Rotate every decades ⑤ Month (Hex: 1 Digit ⇒ Oct - A, Nov - B, Dec - C) ⑥ Date : 1 ~ 31 ⑦ Worker Goup : A Part(Day), B Part(Afternoon), C Part(Night)							

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Figure 1-17 Module serial number

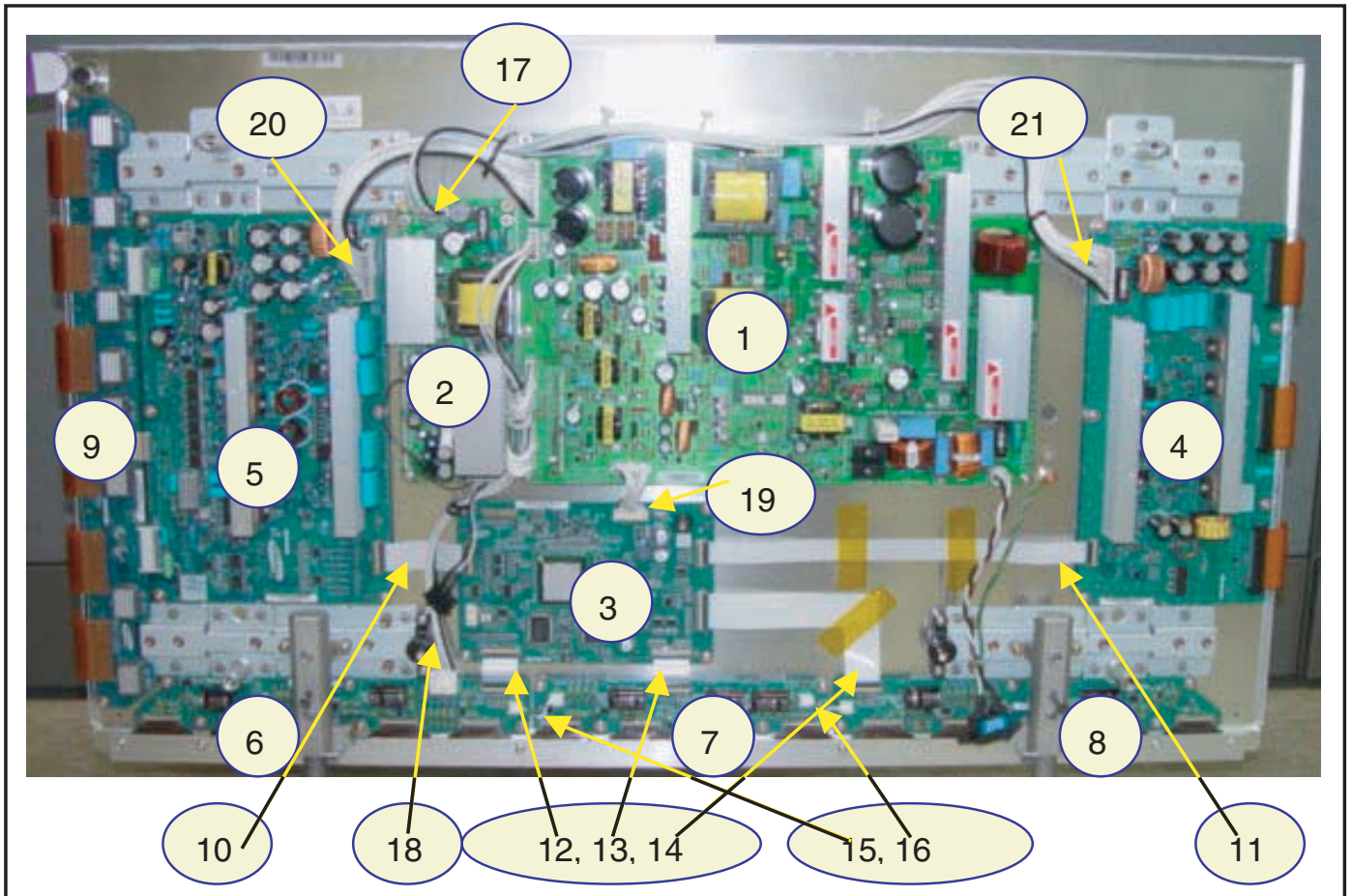
2 6 1 4 0 8 07 0 8 6 5

Serial No : 0001~9999
Date : 01~31
Month : 01~12
Year : 00(2000) ~99(2099)
Line No : 1 ~ 9 (0:Pilot Line)
Type : 02~48 (ex.50HDv3:26) (Step of even)

Figure 1-18 Panel serial number

1.3 Chassis Overview

1.3.1 37" SD v4



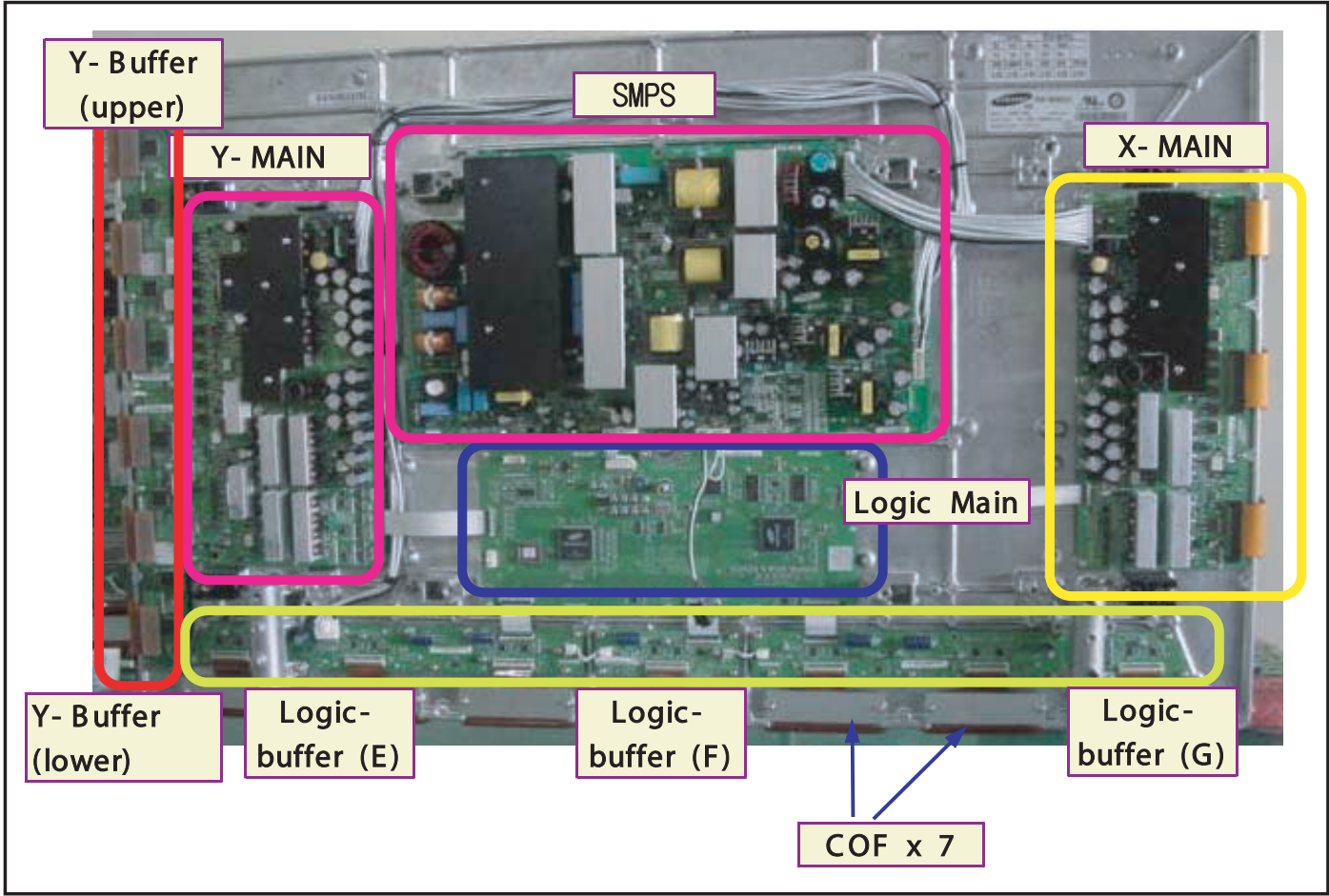
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Figure 1-19 PWB location (37" SD v4)

Table 1-3 PWB overview (37" SD v4)

No.	Location	Name
1	Main PSU	Assy PWB PSU
2	SUB-PSU	Assy PWB SUB-PSU
3	LOGIC-MAIN Board	Assy PWB LOGIC Main
4	X-MAIN Driving Board	Assy PWB X Main
5	Y-MAIN Driving Board	Assy PWB Y Main
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	LOGIC G BUFFER Board	Assy PWB Buffer
9	Y-BUFFER Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOGIC BUF(E)	FFC Cable-flat
13	LOGIC + LOGIC BUF(F)	FFC Cable-flat
14	LOGIC + LOGIC BUF(G)	FFC Cable-flat
15	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
16	LOGIC BUF(F) + LOG. BUF(G)	Lead connector
17	PSU + SUB PSU	Lead connector
18	PSU + LOGIC BUF(E)	Lead connector
19	PSU + LOGIC MAIN	Lead connector
20	PSU + Y-MAIN	Lead connector

1.3.2 42" SD v2



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Figure 1-20 PWB location (42" SD v2)

Table 1-4 PWB overview (42" SD v2)

No.	Location	Name
1	info not available	
2		
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1.3.3 42" SD v3

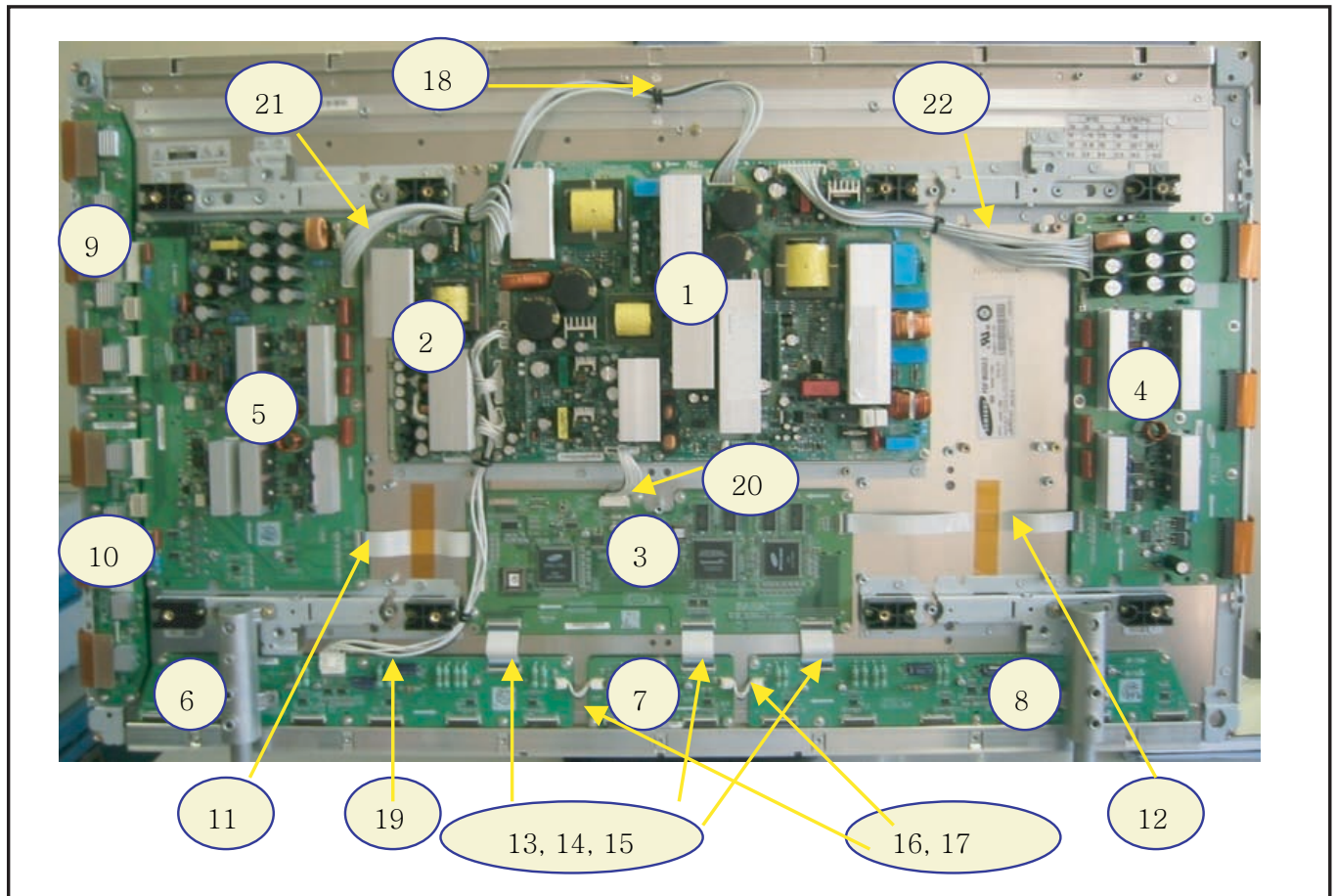
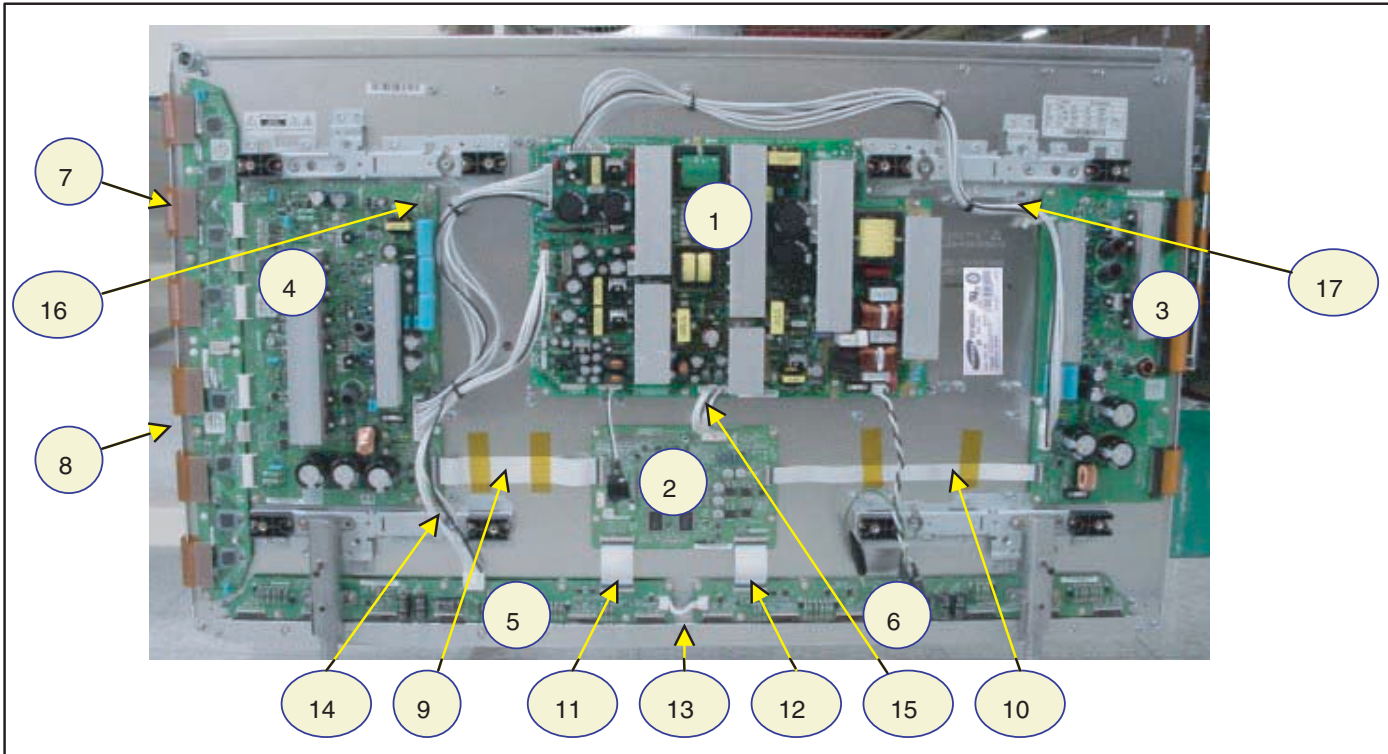
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061005

Figure 1-21 PWB location (42" SD v3)

Table 1-5 PWB overview (42" SD v3)

No.	Location	Name
1	Main PSU	Assy PWB PSU
2	SUB-PSU	Assy PWB SUB-PSU
3	LOGIC-MAIN Board	Assy PWB LOGIC Main
4	X-MAIN Driving Board	Assy PWB X Main
5	Y-MAIN Driving Board	Assy PWB Y Main
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	LOGIC G BUFFER Board	Assy PWB Buffer
9	Y-BUFFER (UPPER) Board	Assy PWB Buffer
10	Y-BUFFER (DOWN) Board	Assy PWB Buffer
11	LOGIC + Y-MAIN	FFC Cable-flat
12	LOGIC + X-MAIN	FFC Cable-flat
13	LOGIC + LOGIC BUF(E)	FFC Cable-flat
14	LOGIC + LOGIC BUF(F)	FFC Cable-flat
15	LOGIC + LOGIC BUF(G)	FFC Cable-flat
16	LOGIC BUF(E) +LOG. BUF(F)	Lead connector
17	LOGIC BUF(F) +LOG. BUF(G)	Lead connector
18	PSU + SUB PSU	Lead connector
19	PSU + LOGIC BUF(E)	Lead connector
20	PSU + LOGIC MAIN	Lead connector
21	PSU + Y-MAIN	Lead connector
22	PSU + X-MAIN	Lead connector

1.3.4 42" SD v4



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Figure 1-22 PWB location (42" SD v4)

Table 1-6 PWB overview (42" SD v4)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB Logic Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB buffer
6	LOGIC F BUFFER Board	Assy PWB buffer
7	Y-BUFFER (UPPER) Board	Assy PWB buffer
8	Y-BUFFER (DOWN) Board	Assy PWB buffer
9	LOGIC + Y-MAIN	FFC cable-flat
10	LOGIC + X-MAIN	FFC cable-flat
11	LOGIC + LOGIC BUF (E)	FFC cable-flat
12	LOGIC + LOGIC BUF (F)	FFC cable-flat
13	LOGIC BUF (E) + (F)	Lead connector
14	SMPS + LOGIC BUF (E)	Lead connector
15	SMPS + LOGIC MAIN	Lead connector
16	SMPS + Y-MAIN	Lead connector
17	SMPS + X-MAIN	Lead connector

1.3.5 42" HD v3

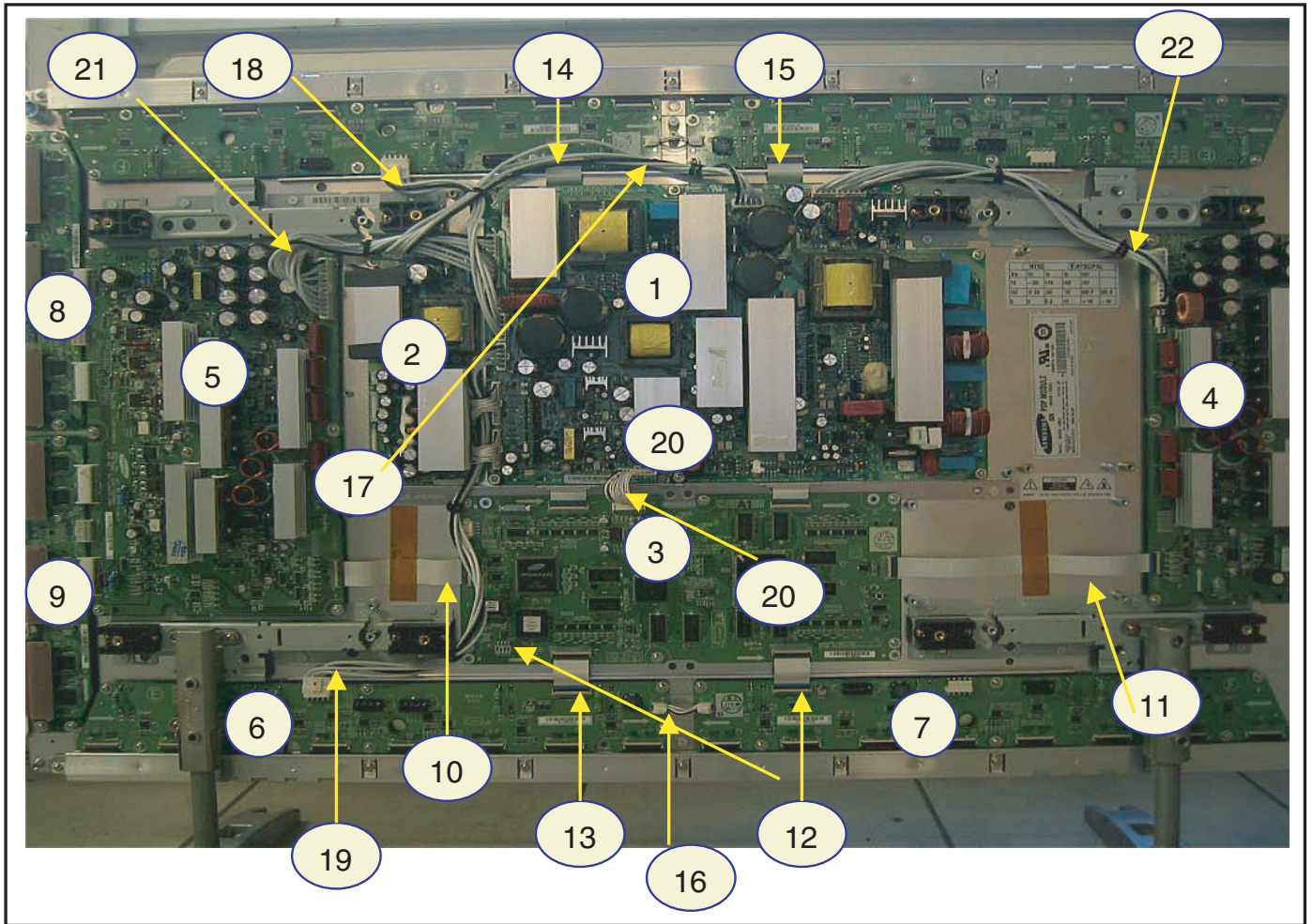
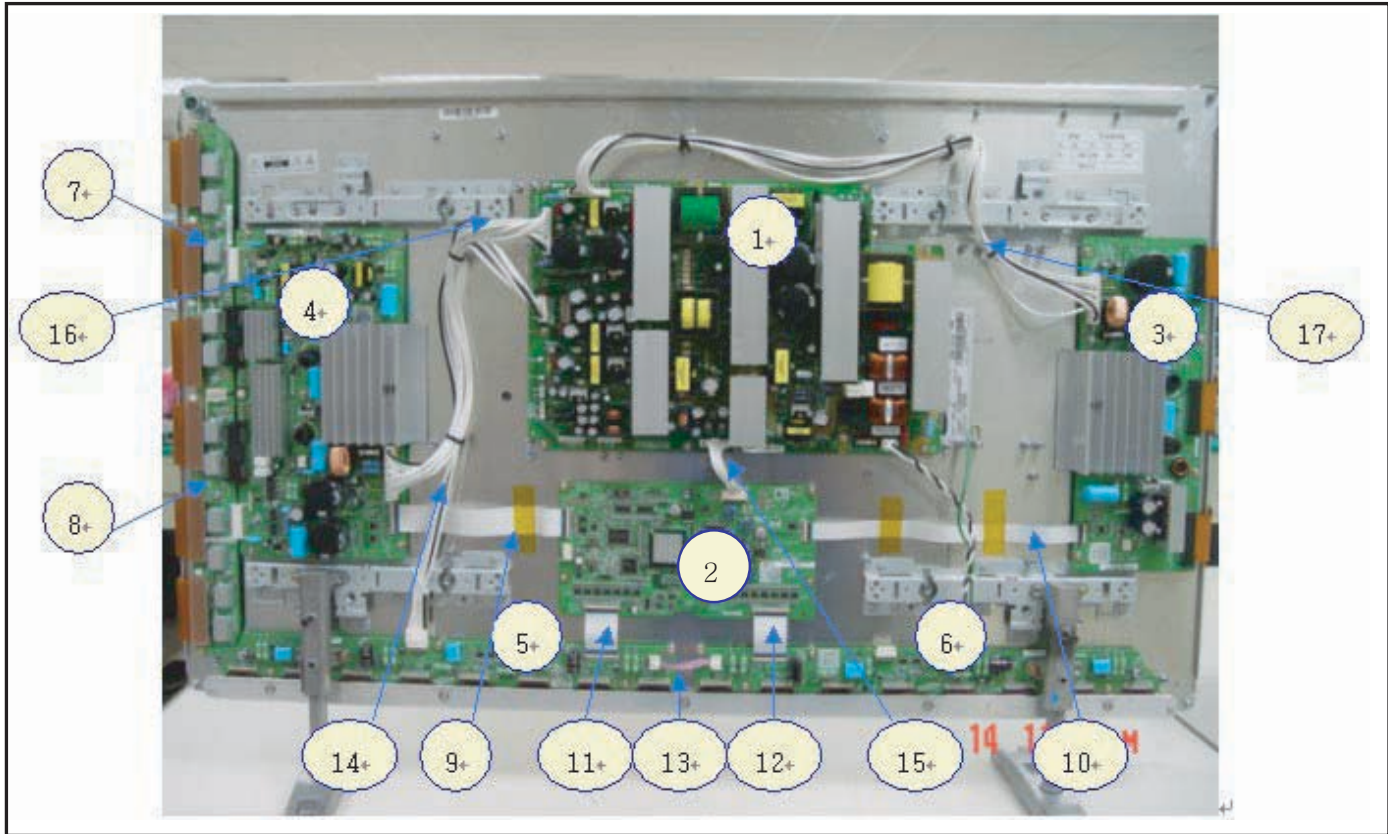
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Figure 1-23 PWB location (42" HD v3)

Table 1-7 PWB overview (42" HD v3)

No.	Location	Name
1	Main PSU	Assy PWB PSU
2	SUB-PSU	Assy PWB SUB-PSU
3	LOGIC-MAIN Board	Assy PWB LOGIC Main
4	X-MAIN Driving Board	Assy PWB X Main
5	Y-MAIN Driving Board	Assy PWB Y Main
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	Y-BUFFER (UPPER) Board	Assy PWB Buffer
9	Y-BUFFER (DOWN) Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOG. BUF(E) (Down)	FFC Cable-flat
13	LOGIC + LOG. BUF(F) (Down)	FFC Cable-flat
14	LOGIC + LOGIC BUF(E) (Up)	FFC Cable-flat
15	LOGIC + LOGIC BUF(E) (Up)	FFC Cable-flat
16	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
17	PSU + SUB PSU	Lead connector
18	PSU + LOGIC BUF(E) (UP)	Lead connector
19	PSU + LOGIC BUF(E) (Down)	Lead connector
20	PSU + LOGIC MAIN	Lead connector
21	PSU + Y-MAIN	Lead connector
22	PSU + X-MAIN	Lead connector

1.3.6 42" HD v4



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Figure 1-24 PWB location (42" HD v4)

Table 1-8 PWB overview (42" HD v4)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWBLOGIC Main
3	X-MAIN Driving Board	Assy PWBX Main
4	Y-MAIN Driving Board	Assy PCBY Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER (UPPER) Board	Assy PWB Buffer
8	Y-BUFFER (DOWN) Board	Assy PWB Buffer
9	LOGIC + Y-MAIN	FFC Cable-flat
10	LOGIC + X-MAIN	FFC Cable-flat
11	LOGIC + LOGIC BUF(E)	FFC Cable-flat
12	LOGIC + LOGIC BUF(F)	FFC Cable-flat
13	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
14	SMPS + LOGIC BUF(E)	Lead connector
15	SMPS + LOGIC MAIN	Lead connector
16	SMPS + Y-MAIN	Lead connector
17	SMPS + X-MAIN	Lead connector

1.3.7 50" HD v3

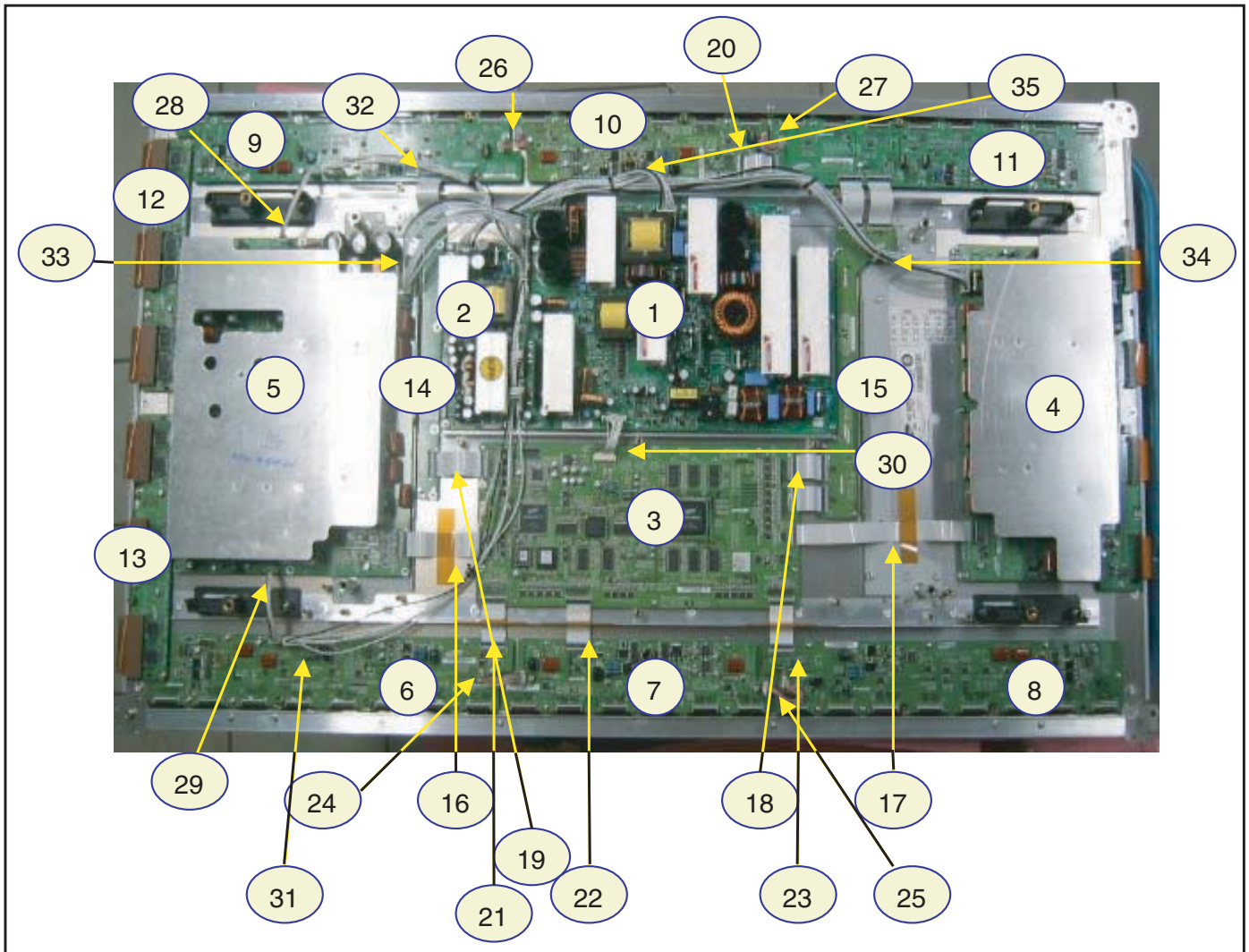
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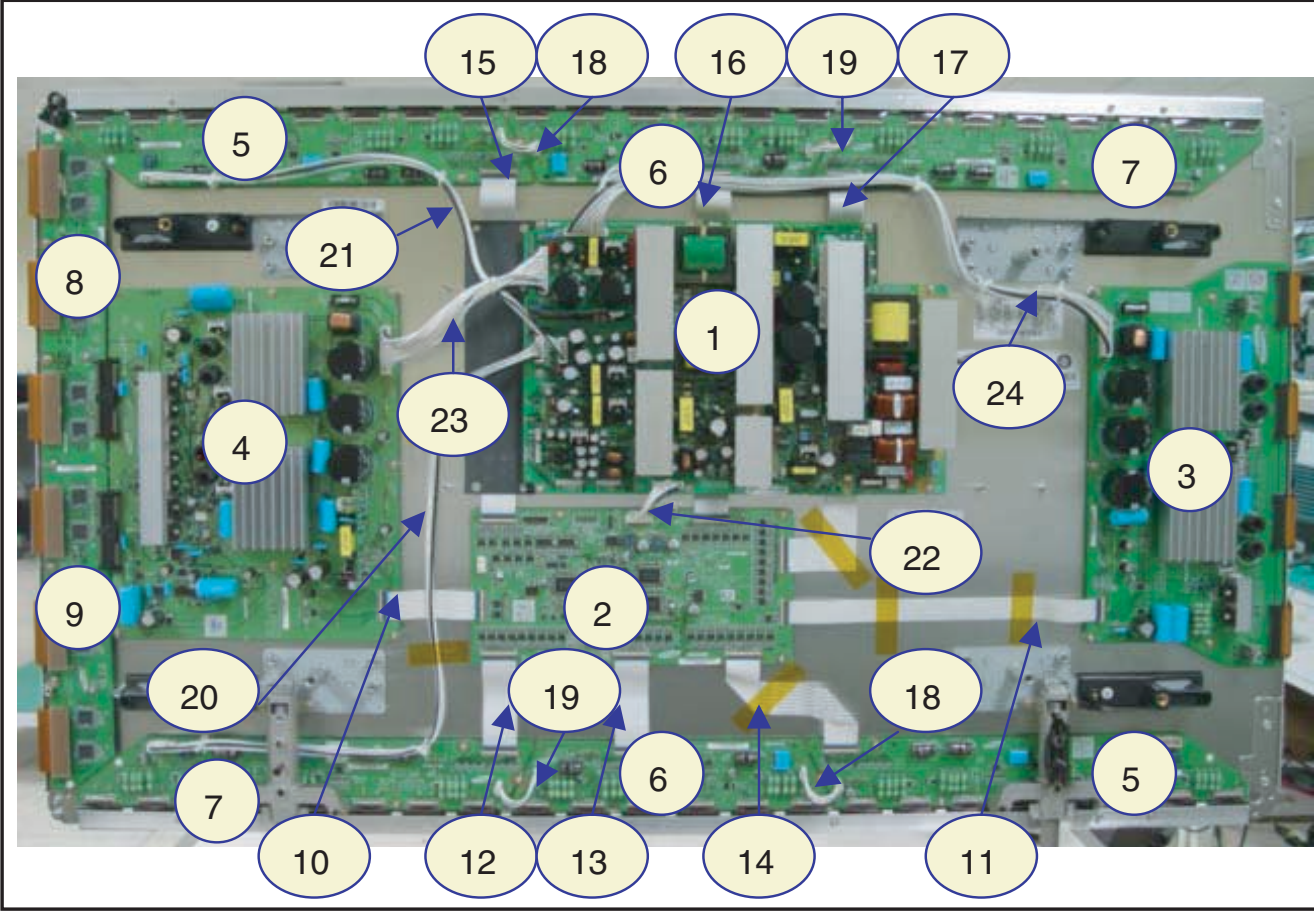
Figure 1-25 PWB location (50" HD v3)

Table 1-9 PWB overview (50" HD v3)

No.	Location	Name
1	Main PUS	Assy PWBPSU
2	SUB-PSU	Assy PWB SUB-PSU
3	LOGIC-MAIN Board	Assy PWB LOGIC Main
4	X-MAIN Driving Board	Assy PWB X MAIN
5	Y-MAIN Driving Board	Assy PWB Y MAIN
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	LOGIC G BUFFER Board	Assy PWB Buffer
9	LOGIC H BUFFER Board	Assy PWB Buffer
10	LOGIC I BUFFER Board	Assy PWB Buffer
11	LOGIC J BUFFER Board	Assy PWB Buffer
12	Y-BUFFER (UPPER) Board	Assy PWB Buffer
13	Y-BUFFER (DOWN) Board	Assy PWB Buffer
14	SUB-R	Assy PWB Buffer
15	SUB-L	Assy PWB Buffer
16	LOGIC + Y-MAIN	FFC Cable-flat
17	LOGIC + X-MAIN	FFC Cable-flat
18	SUB R + LOGIC	FFC Cable-flat
19	SUB L + LOGIC	FFC Cable-flat
20	LOG.BUF(I) + LOG.BUF(J) (Up)	FFC Cable-flat
21	LOGIC + LOG. BUF(E) (Down)	FFC Cable-flat

No.	Location	Name
22	LOGIC + LOG. BUF(F) (Down)	FFC Cable-flat
23	LOGIC + LOG. BUF(G) (Down)	FFC Cable-flat
24	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
25	LOGIC BUF(F) + LOG. BUF(G)	Lead connector
26	LOGIC BUF(H) + LOG. BUF(I)	Lead connector
27	LOGIC BUF(I) + LOG. BUF(J)	Lead connector
28	Y-MAIN + LOGIC BUF(H)	Lead connector
29	Y-MAIN + LOGIC BUF(E)	Lead connector
30	PSU + LOGIC MAIN	Lead connector
31	PSU + LOGIC BUF(E)	Lead connector
32	PSU + LOGIC BUF(H)	Lead connector
33	PSU + Y-MAIN	Lead connector
34	PSU + X-MAIN	Lead connector
35	PSU + SUB PSU	Lead connector

1.3.8 50" HD v4



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Figure 1-26 PWB location (50" HD v4)

Table 1-10 PWB overview (50" HD v4)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWBLOGIC Main
3	X-MAIN Driving Board	Assy PWBX Main
4	Y-MAIN Driving Board	Assy PCBY Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	LOGIC G BUFFER Board	Assy PWB Buffer
8	Y-BUFFER (Upper) Board	Assy PWB Buffer
9	Y-BUFFER (Down) Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOG. BUF(G: Down)	FFC Cable-flat
13	LOGIC + LOG. BUF(F: Down)	FFC Cable-flat
14	LOGIC + LOG. BUF(E: Down)	FFC Cable-flat
15	LOGIC + LOG. BUF(E: Upper)	FFC Cable-flat
16	LOGIC + LOG. BUF(F: Upper)	FFC Cable-flat
17	LOGIC + LOG. BUF(G: Upper)	FFC Cable-flat
18	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
19	LOGIC BUF(F) + LOG. BUF(G)	Lead connector
20	SMPS + LOGIC BUF(G: Down)	Lead connector
21	SMPS + LOGIC BUF(E: Upper)	Lead connector
22	SMPS + LOGIC MAIN	Lead connector
23	SMPS + Y-MAIN	Lead connector
24	SMPS + X-MAIN	Lead connector

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

- 2.1 Handling Precautions
- 2.2 Safety Precautions
- 2.3 Notes

Notes:

- Only authorised persons should perform servicing of this module.
- When using/handling this unit, pay special attention to the PDP Module: it should not be enforced into any other way than next rules, warnings, and/or cautions.
- **"Warning"** indicates a hazard that may lead to death or injury if the warning is ignored and the product is handled incorrectly.
- **"Caution"** indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

2.1 Handling Precautions

- The PDP module use high voltage that is dangerous to humans. Before operating the PDP, always check for dust to prevent short circuits. Be careful touching the circuit device when power is "on".
- The PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- The PDP module has a lot of electric devices. The service engineer must wear equipment (for example, earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- The PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. The operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is "off". Operator must wait for discharging of remaining voltage during at least 1 minute.

2.2 Safety Precautions

2.2.1 Safety Precautions

- Before replacing a board, discharge forcibly.
- The remaining electricity from board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.
- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuff including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change: Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, it cause danger on safety. And, if you change the design or insert, manufacturer guarantee will be not effect.
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between

parts and circuit board. Check the cord of AC power preparing damage.

- Product Safety Mark: Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned "off", before next repair.
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

2.2.2 ESD Precautions

There are parts, which are easily damaged by electrostatics (for example Integrated Circuits, FETs, etc.) Electrostatic damage rate of product will be reduced by the following technics:

- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring (it must be operated after removing dust on it. It comes under precaution of electric shock).
- After removing the assembly, lay it with the tracks on a conductive surface to prevent charging.
- Do not use chemical stuff containing Freon. It generates positive electric that can damage ESD sensitive devices.
- You must use a soldering device for ground-tip when soldering or de-soldering these devices.
- You must use anti-static solder removal device. Most removal devices do not have antistatic which can charge a enough positive electric enough for damaging these devices.
- Before removing the protective material from the lead of a new device, bring the protective material into contact with the chassis or assembly.
- When handing an unpacked device for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the device.
- Do not take a new device from the protective case until the it is ready to be installed. Most devices have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminium)

2.3 Notes

A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel, it is recommended to do some maintenance by a qualified service employee only.

2.3.1 Safe PDP Handling

- The work procedures shown with the "Note" indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times, other than when adjusting and checking the product, be sure to turn "off" the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of PWBs, start the servicing work at least 30 seconds after the main power has been turned "off". Especially when installing and removing the Power Supply PWB and the SUS PWB in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned "off".

- While the main power is “on”, do not touch any parts or circuits other than the ones specified. The high voltage Power Supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit PWB, be sure to remove static electricity from your body before handling the circuit PWB.
- Be sure to handle the circuit PWB by holding the large parts as the heat sink or transformer. Failure to observe this

precaution may result in the occurrence of an abnormality in the soldered areas.

- Do not stack the circuit PWB. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original

3. Directions For Use

Not applicable.

4. Mechanical Instructions

Index of this chapter:

- 4.1 Dis-assembling / Re-assembling
 - 4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)
 - 4.1.2 Flat Cable Connector of X-main Board
 - 4.1.3 FFC and TCP from Connector
 - 4.1.4 Exchange of LBE, LBF, LBG board
 - 4.1.5 Exchange YBU, YBL and YM board

4.1 Dis-assembling / Re-assembling

4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)

- Dis-assembly: Pull out the FPC from the connector by holding the lead of the FPC with both hands.
- Re-assembly: Push the lead of FPC with same force on both sides into the connector.

Note: Be careful do not to damage the connector pin during connecting.

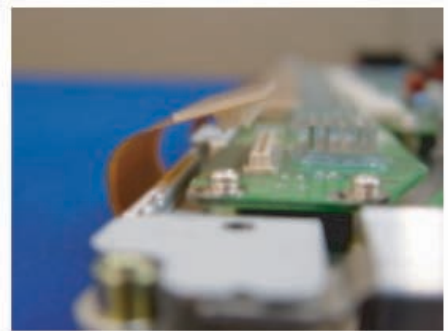
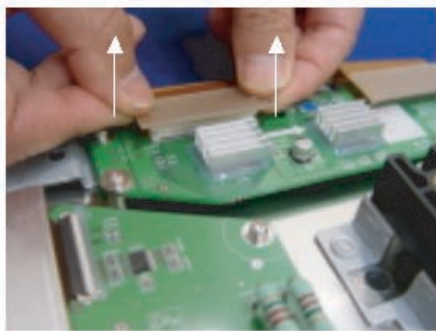


Figure 4-1 Dis-assembly FPC of Y-buffer

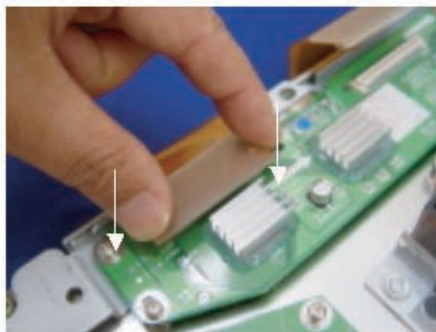


Figure 4-2 Re-assembly FPC of Y-buffer

4.1.2 Flat Cable Connector of X-main Board

- Dis-assembly:
 1. Pull out the clamp of connector.
 2. Pull Flat cable out press down lightly.
 3. Turn the Flat Cable reversely.
- Re-assembly: Put the Flat Cable into the connector press down lightly until locking sound ("Click") comes out.

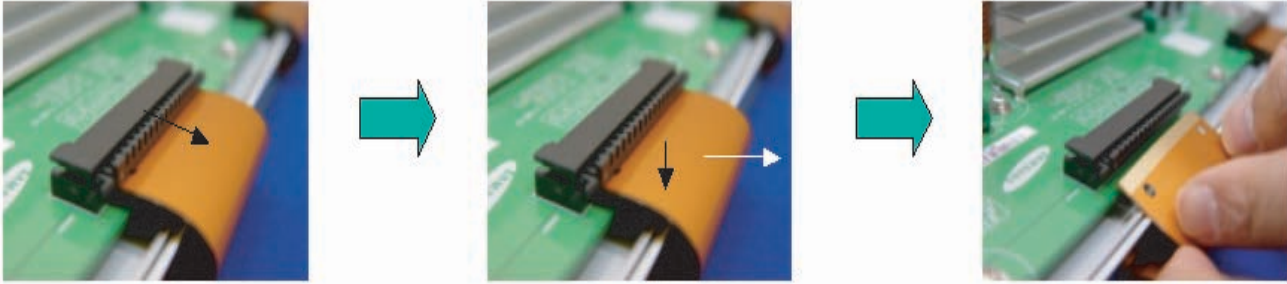


Figure 4-3 Dis-assembly FCC of X-main board

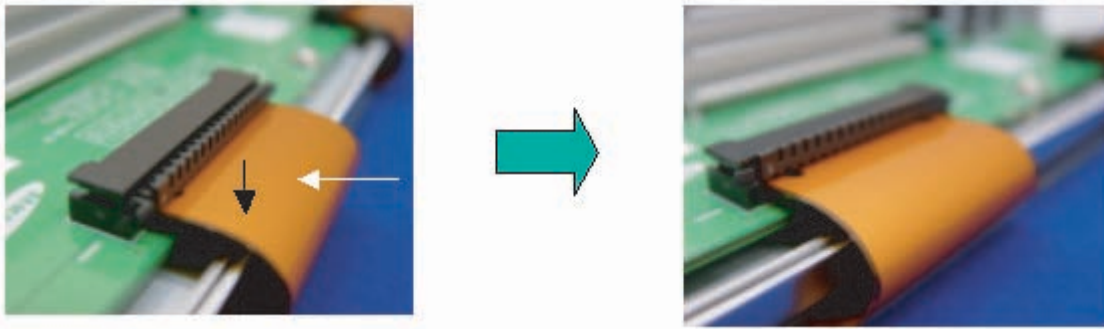


Figure 4-4 Re-assembly FCC of X-main board

4.1.3 FFC and TCP from Connector

- Dis-assembling of TCP:
 1. Open the clamp carefully.
 2. Pull the TCP out from its connector.
- Re-assembling of TCP:
 1. Put the TCP into the connector carefully
 2. Close the clamp completely (until "Click" comes out.).

Notes:

- Checking whether the foreign material is on the connector inside before assembling of TCP.
- Be careful, do not damage the board by ESD during handling of TCP.

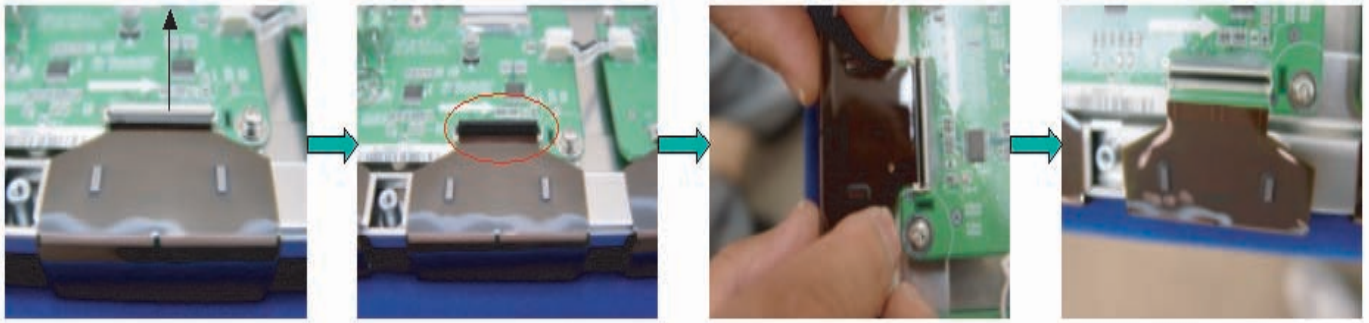


Figure 4-5 Dis-assembly of TCP

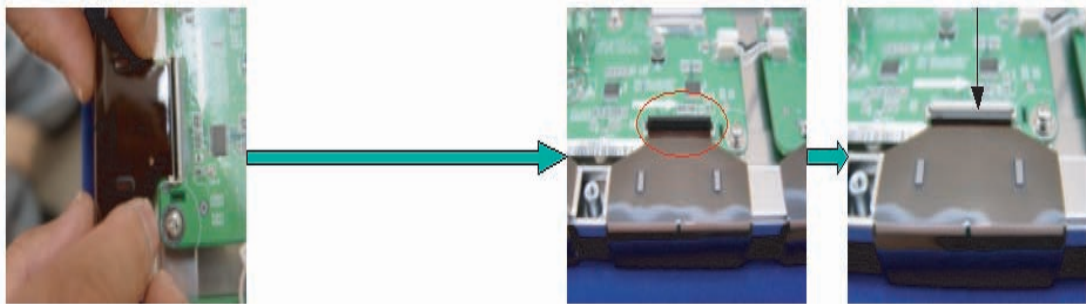


Figure 4-6 Re-assembly of TCP

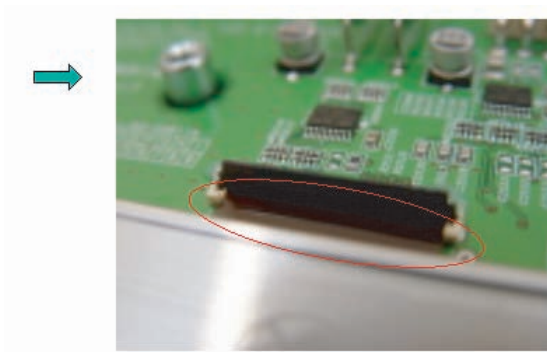


Figure 4-7 Mis-assembly of TCP

The procedure of assembling and disassembling of FFC is same as TCP

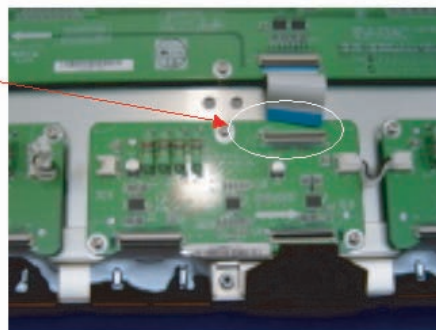


Figure 4-8 Dis- and re-assembly of FFC

4.1.4 Exchange of LBE, LBF, LBG board

1. Depending on the model (see "Photo 2" per model.):
 - **42" SD v3** - Remove the screws in order of 2-3-5-7-1-4-6 (and 10-11-13-16-9-12-14 for HD) from heat sink and then remove heat sink (Photo 1).
 - **42" SD v4** - Remove the screws in order of 2-4-1-5-3 from heat sink and then remove heat sink (Photo 1).
 - **42" HD v3, 37" SD v4, 50" HD v3** - Remove the screws in order of "Centre - Left Side - Right Side" from heat sink and then get rid of heat sink (Photo 1).
 - **50" HD v4** - Remove the screws in order of 2-3-1-4 from heat sink and then remove heat sink (Photo 1).
2. Remove the TPC, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defected board.
Note: When replacing the Logic board or Y-main board for a lead-free (Pb-free) board, always replace them together. (this is **only** valid for the 37" SD v4 displays!)
5. Replace the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connector.
8. Re-assemble the TCP heat sink. Use the same screw mounting order as described above

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.



Figure 4-9 Photo 1 - Heatsink removal

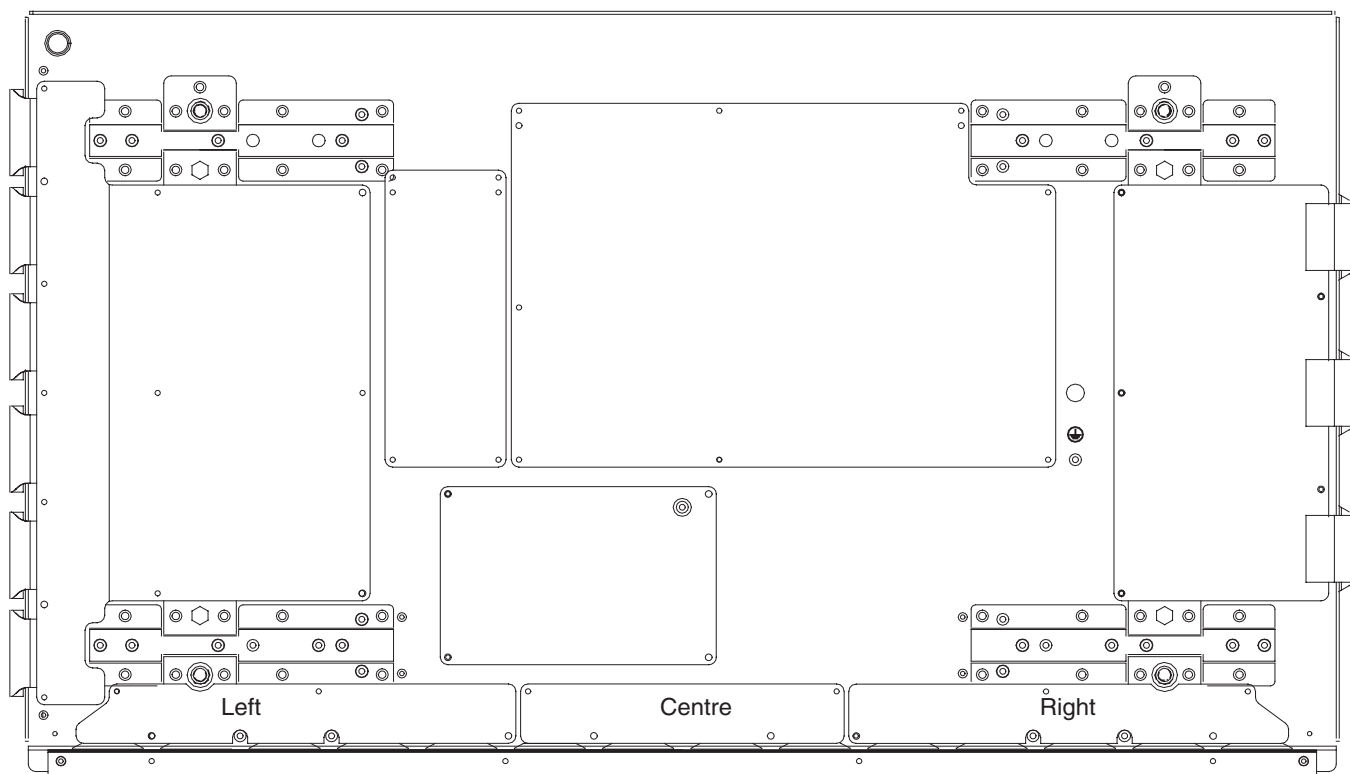


Figure 4-10 Photo 2 - 37" SD v4

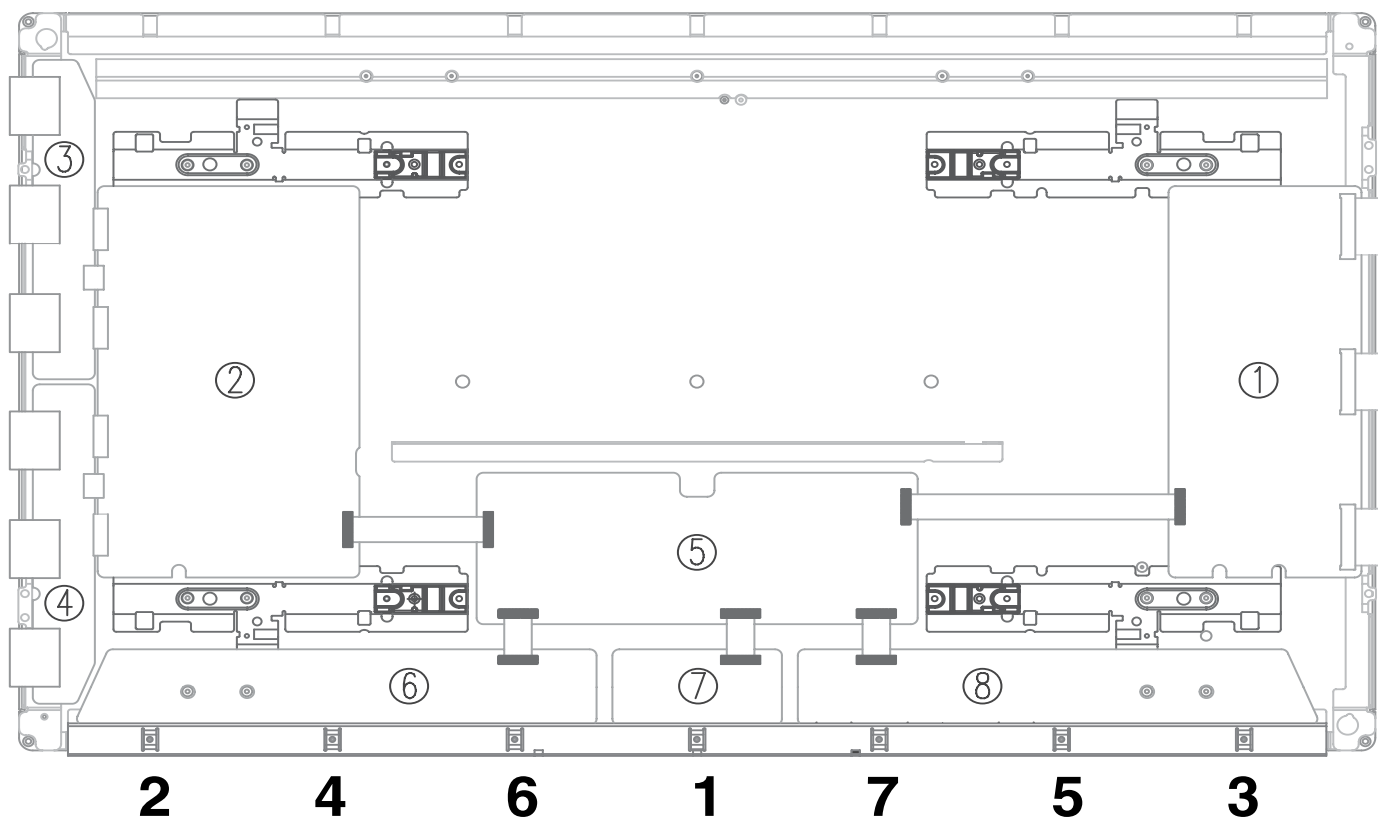
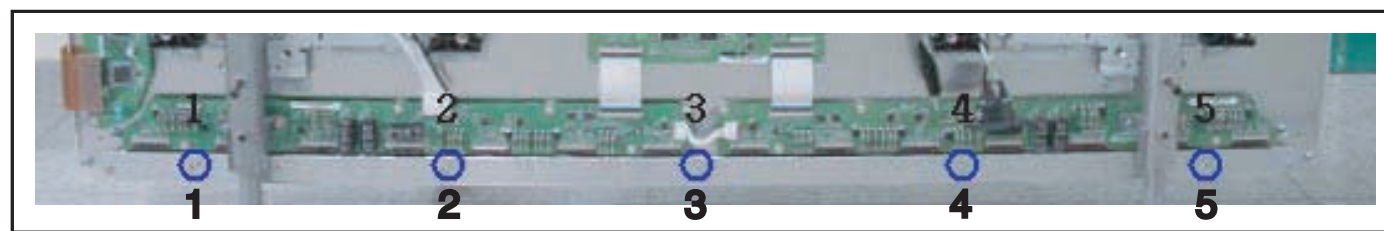


Figure 4-11 Photo 2 - 42" SD v2 and v3



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Figure 4-12 Photo 2 - 42" SD v4

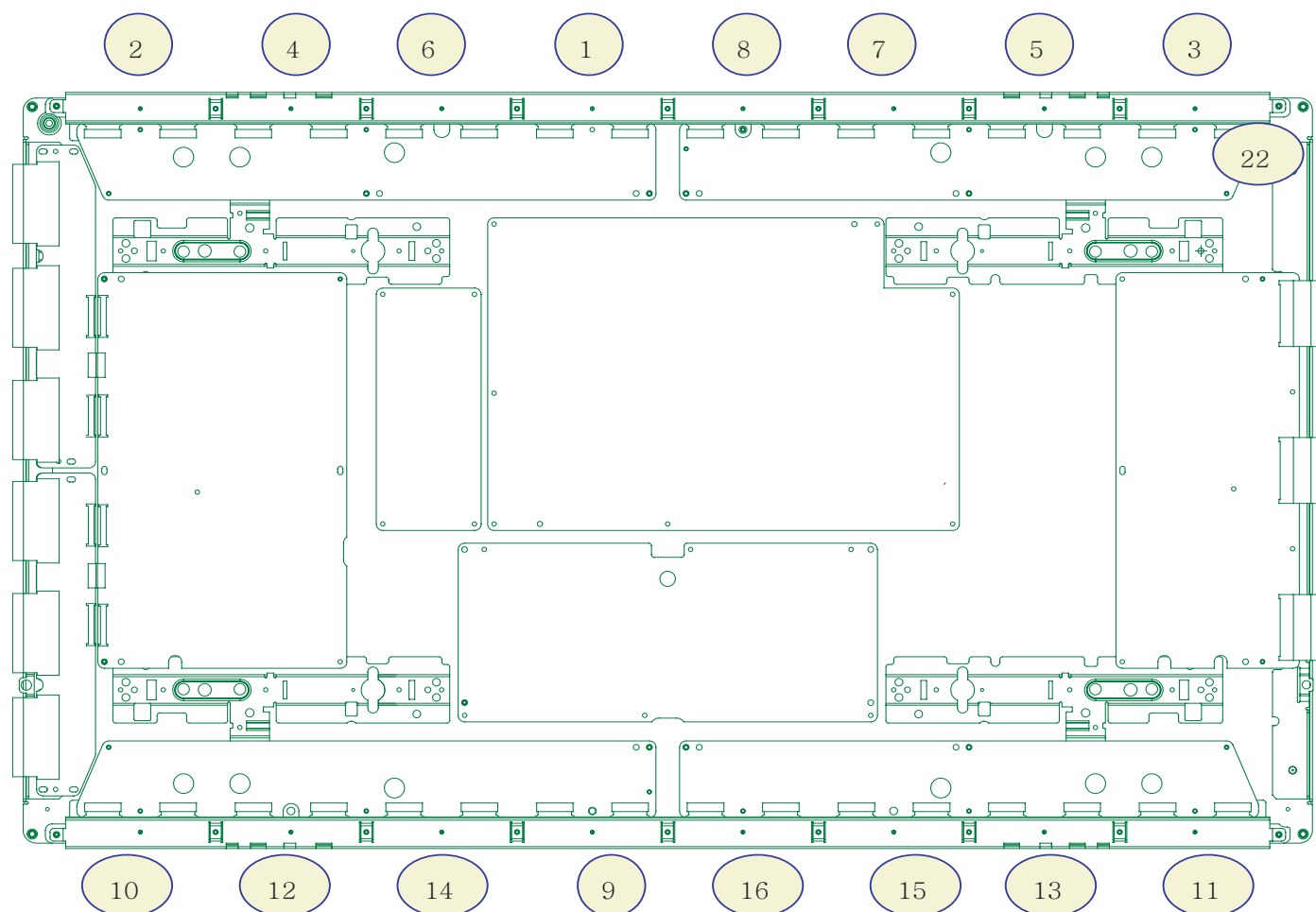
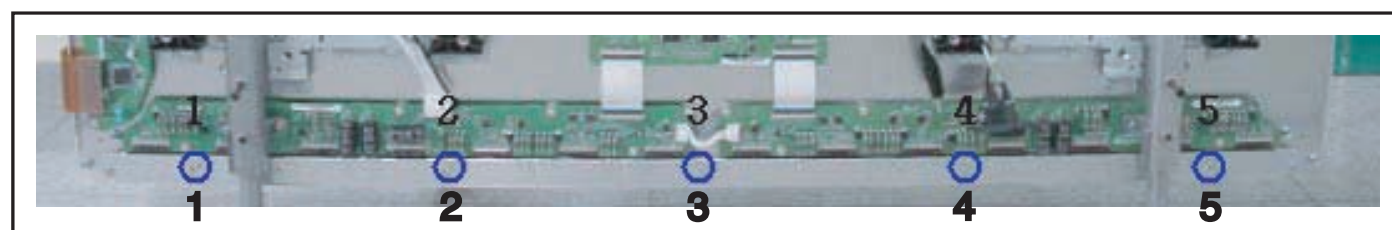


Figure 4-13 Photo 2 - 42" HD v3



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Figure 4-14 Photo 2 - 42" HD v4

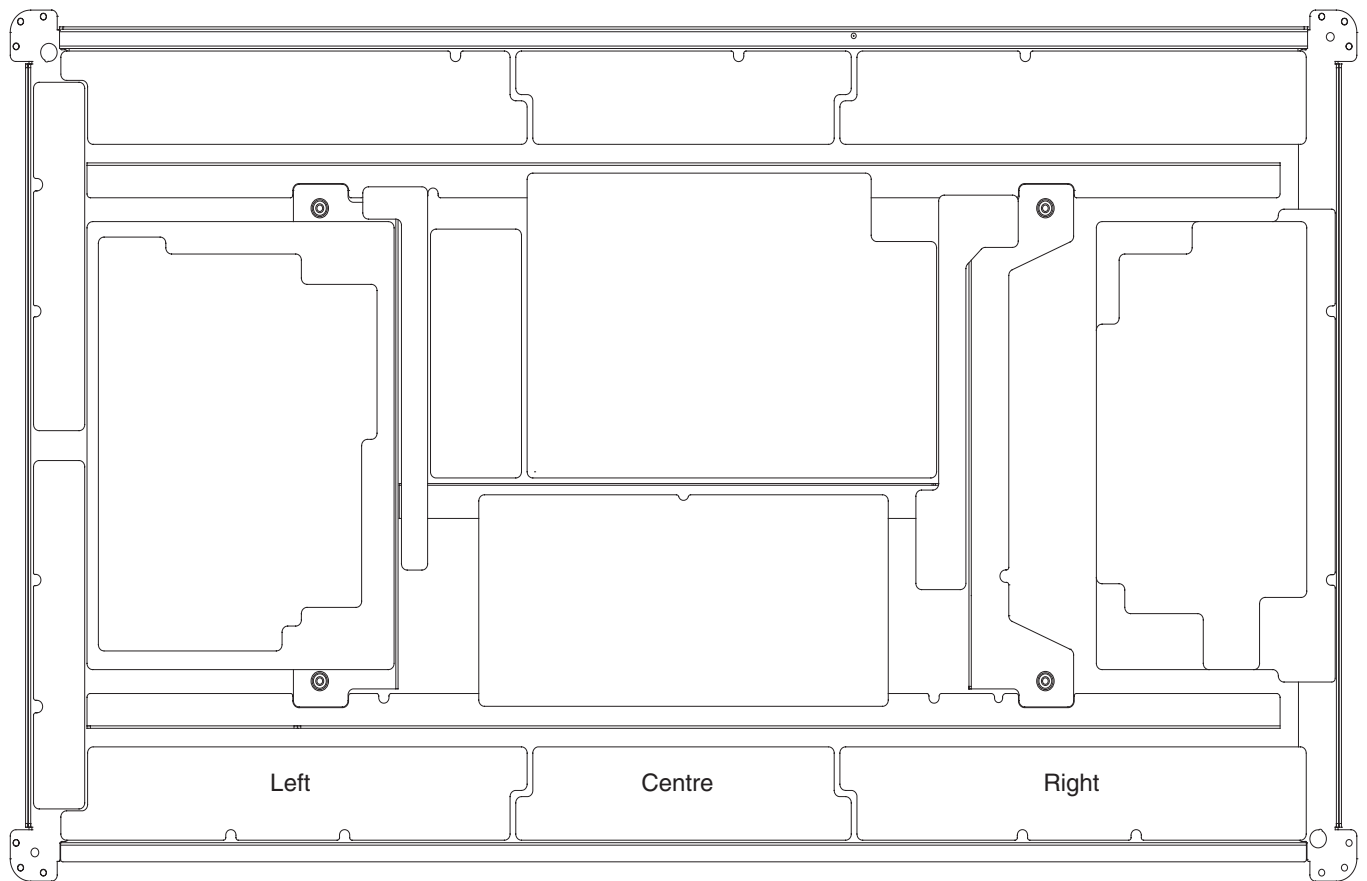


Figure 4-15 Photo 2 - 50" HD v3

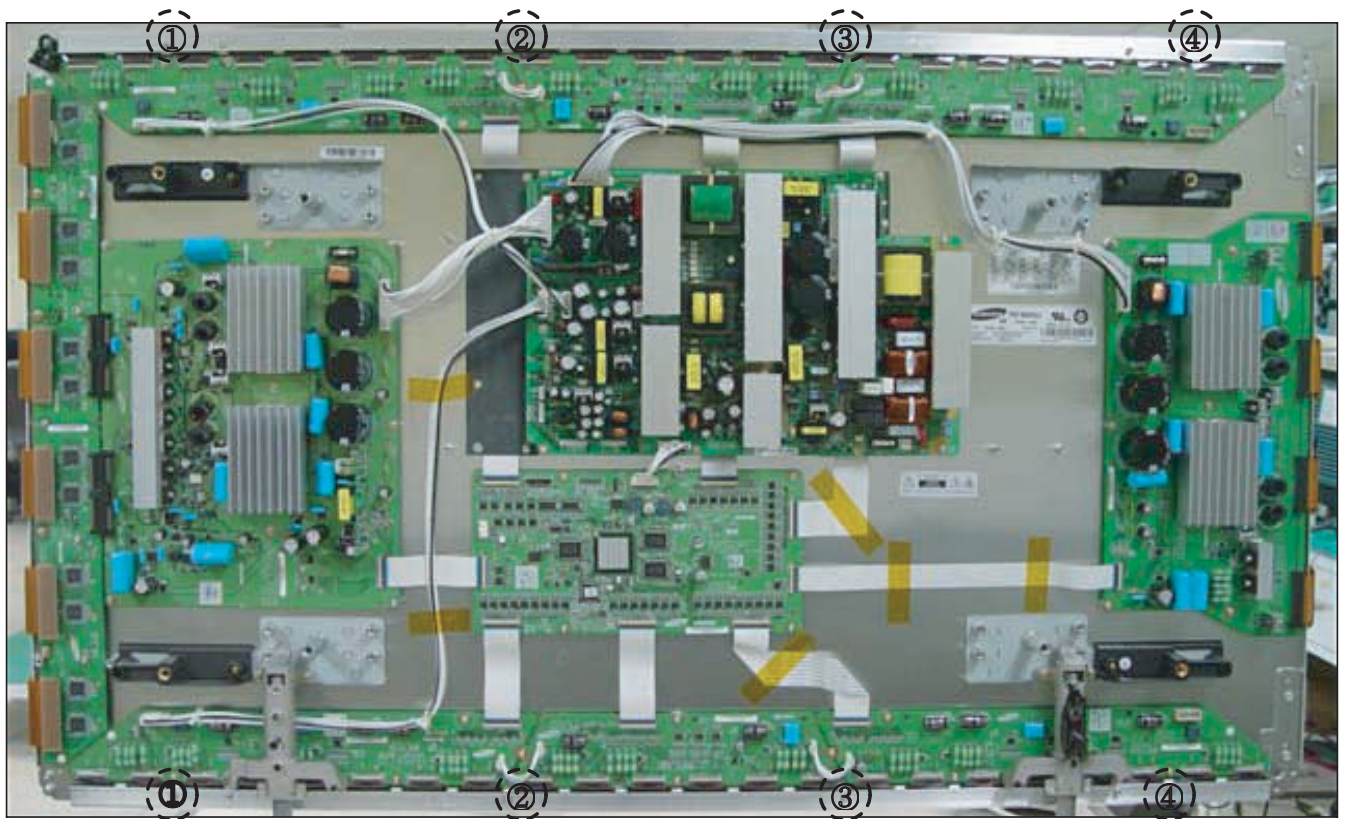
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Figure 4-16 Photo 2 - 50" HD v4

4.1.5 Exchange YBU, YBL and YM board

1. Separate all the FPC connector s of YBU (Y-Buffer upper) and YBL (Y-Buffer lower). See "Photo 1".
 2. Separate all the connector of CN5001 and CN5008 from Y-Main. See "Photo 2".
 3. Loosen all the screws of YBU, YBL, and YM. See "Photo 3".
 4. Remove the board from chassis.
 5. Remove the connector of CN5006 and CN5007 among YBU, YBL and YM.
 6. Remove the YBL and YBU from Y-main.
 7. Remove the defected board.
- Note:** When replacing the Logic board or Y-main board for a lead-free (Pb-free) board, always replace them together. (this is **only** valid for the 37" SD v4 displays!)
8. Re-assemble the YBU and YBL to the Y-Main.
 9. Connect the connector of CN5006 and CN5007 among YBU, YBL and YM. See "Photo 4".
 10. Arrange the board on the chassis and then screw to fix.
 11. Connect the FPC and YM of panel to the connector. See "Photo 5".
 12. Supply the electric power to the module and then check the waveform of the board.
 13. Turn "off" the power after the waveform is adjusted.

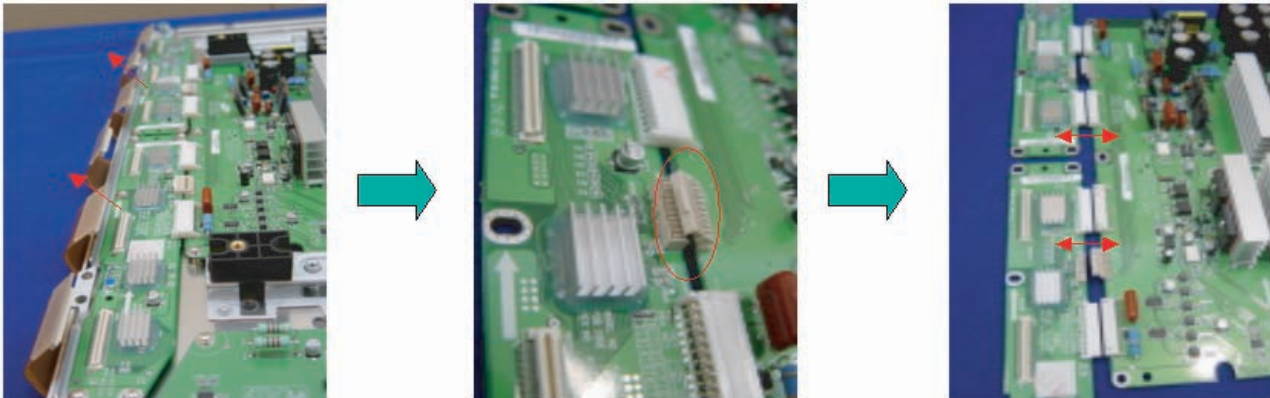


Figure 4-17 Photo 1, 2, and 3: Dis-assembly of YBU, YBL, and YM

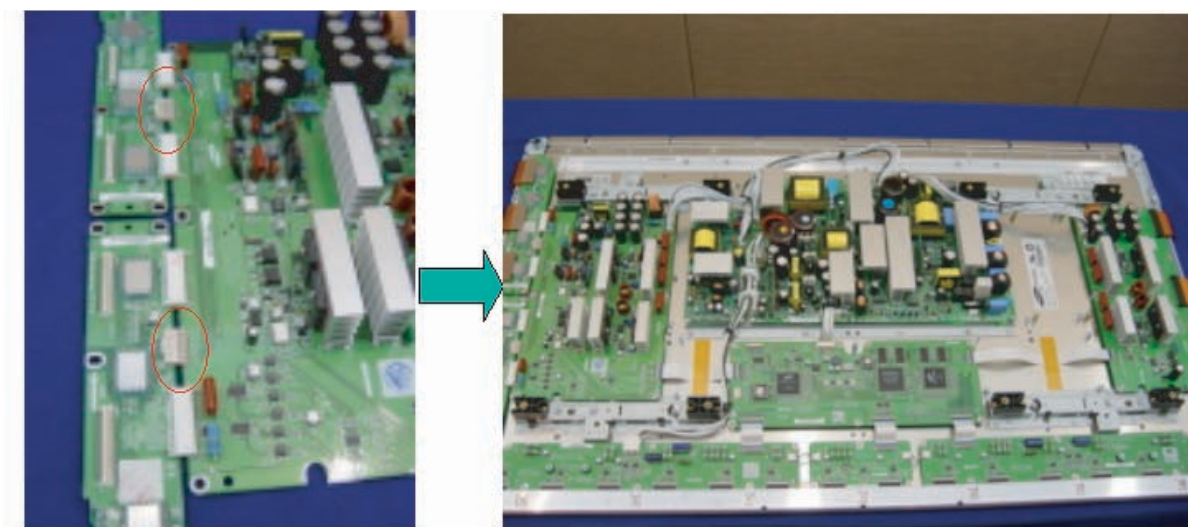


Figure 4-18 Photo 4 and 5: Re-assembly of YBU, YBL, and YM

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

- 5.1 Repair Tools
- 5.2 Fault Finding
- 5.3 Defect Description Form

5.1 Repair Tools

5.1.1 ComPair

For the v3 and v4 models, it will be possible to generate test patterns with ComPair. The ComPair interface must be connected to the Logic Board with the special interconnection cable (see table below for the order code).

5.1.2 Other Service Tools

Table 5-1 Overview Service tools

Service Tools	Order Code
Jumper J8002 + V2 JIG connector kit	3122 785 90760
V3 JIG connector + for SDI panel repair	3122 785 90770
Jumper J8002 to be used in connector kit	3122 785 90780
V2 JIG connector to be used in conn. kit	3122 785 90790
ComPair / SDI interconnection cable	3122 785 90800
Foam buffers (2 pcs.)	3122 785 90581

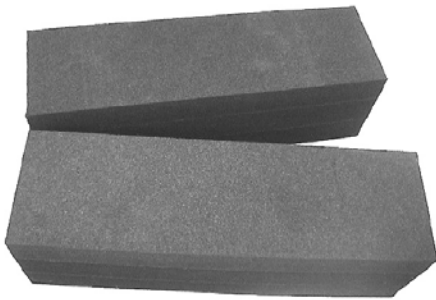


Figure 5-1 Foam buffers



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Figure 5-2 V2 jig



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Figure 5-3 V3 jig

5.2 Fault Finding

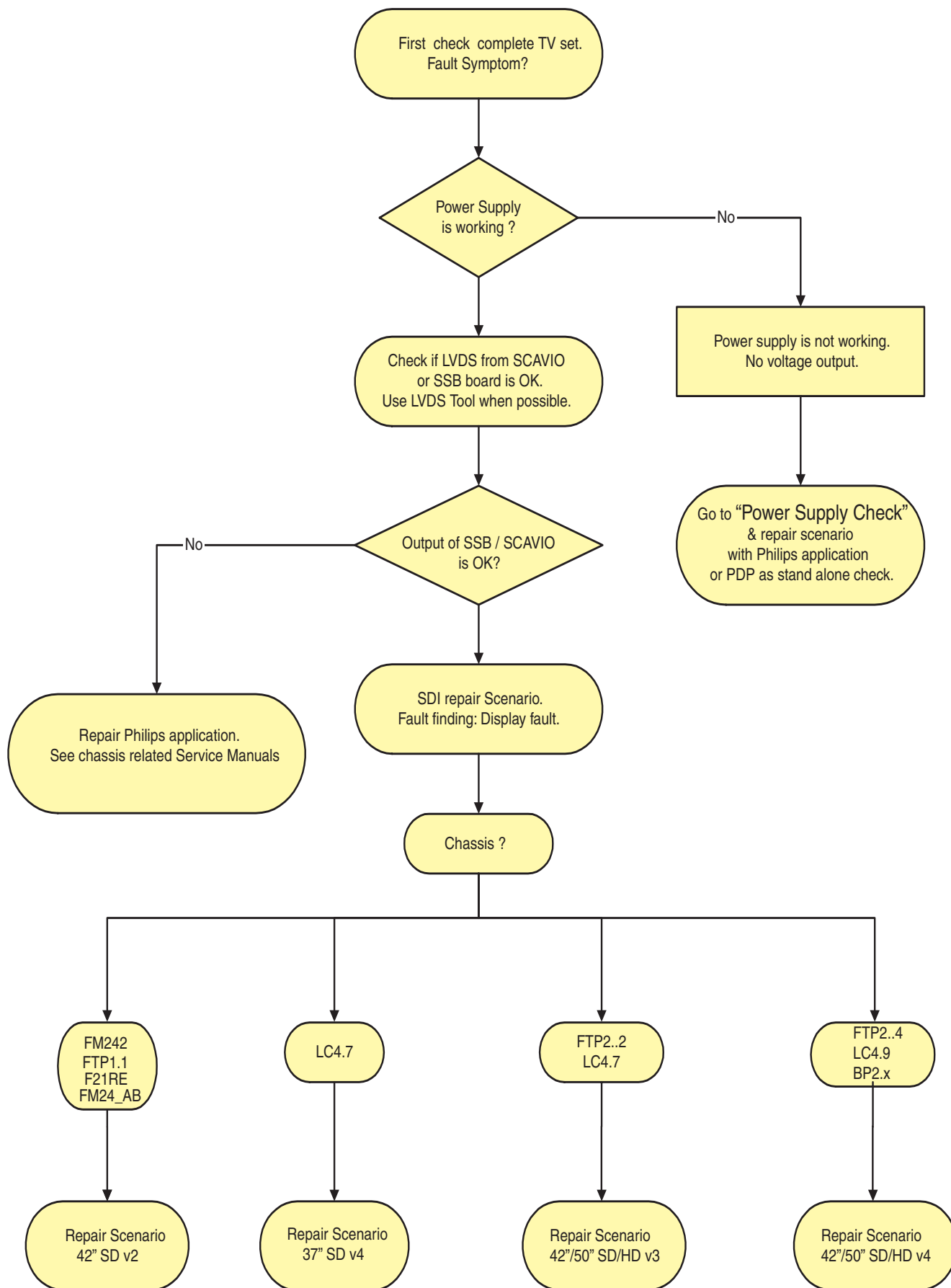


Figure 5-4 Which repair scenario?

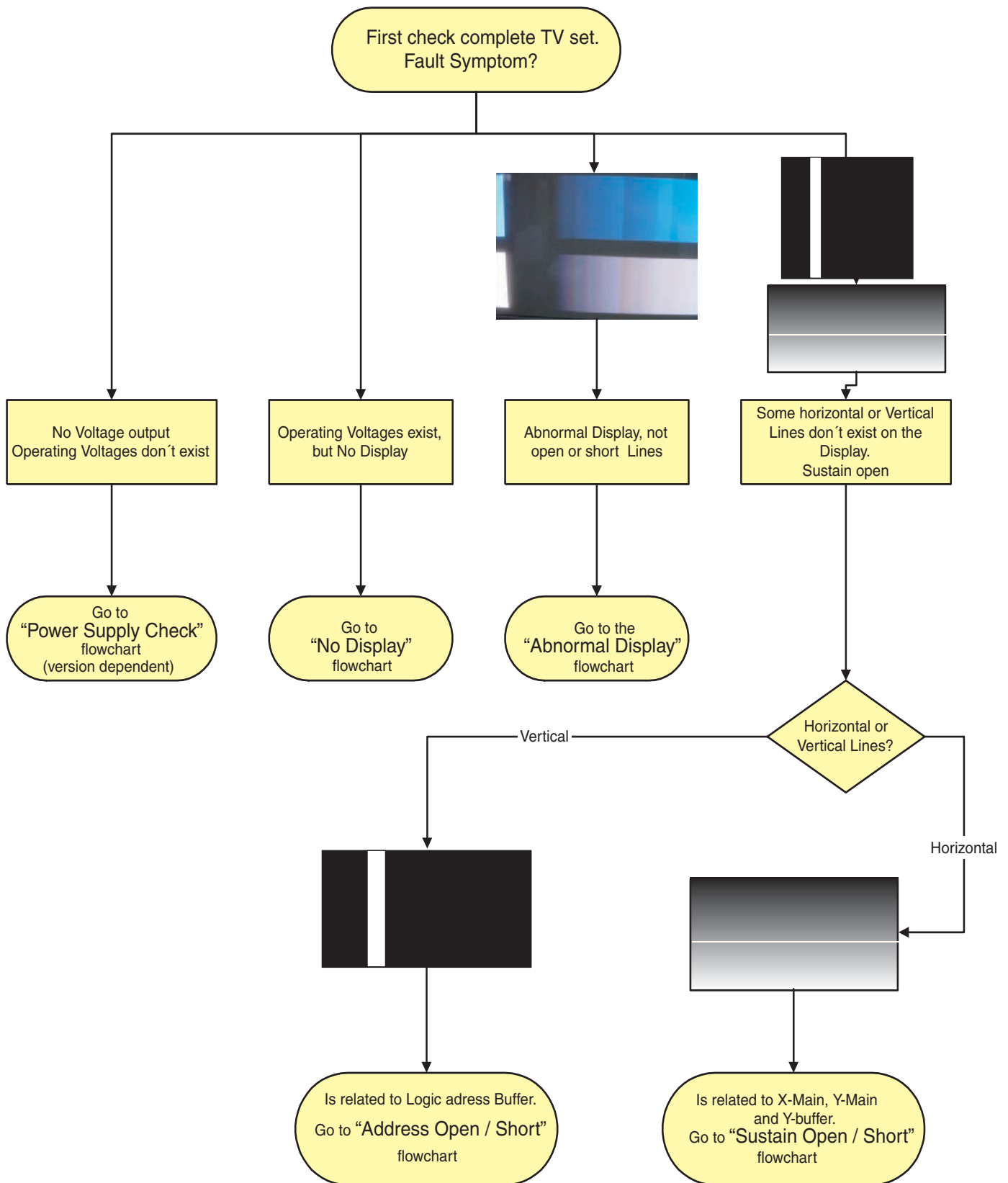


Figure 5-5 Fault symptom overview (complete TV set)

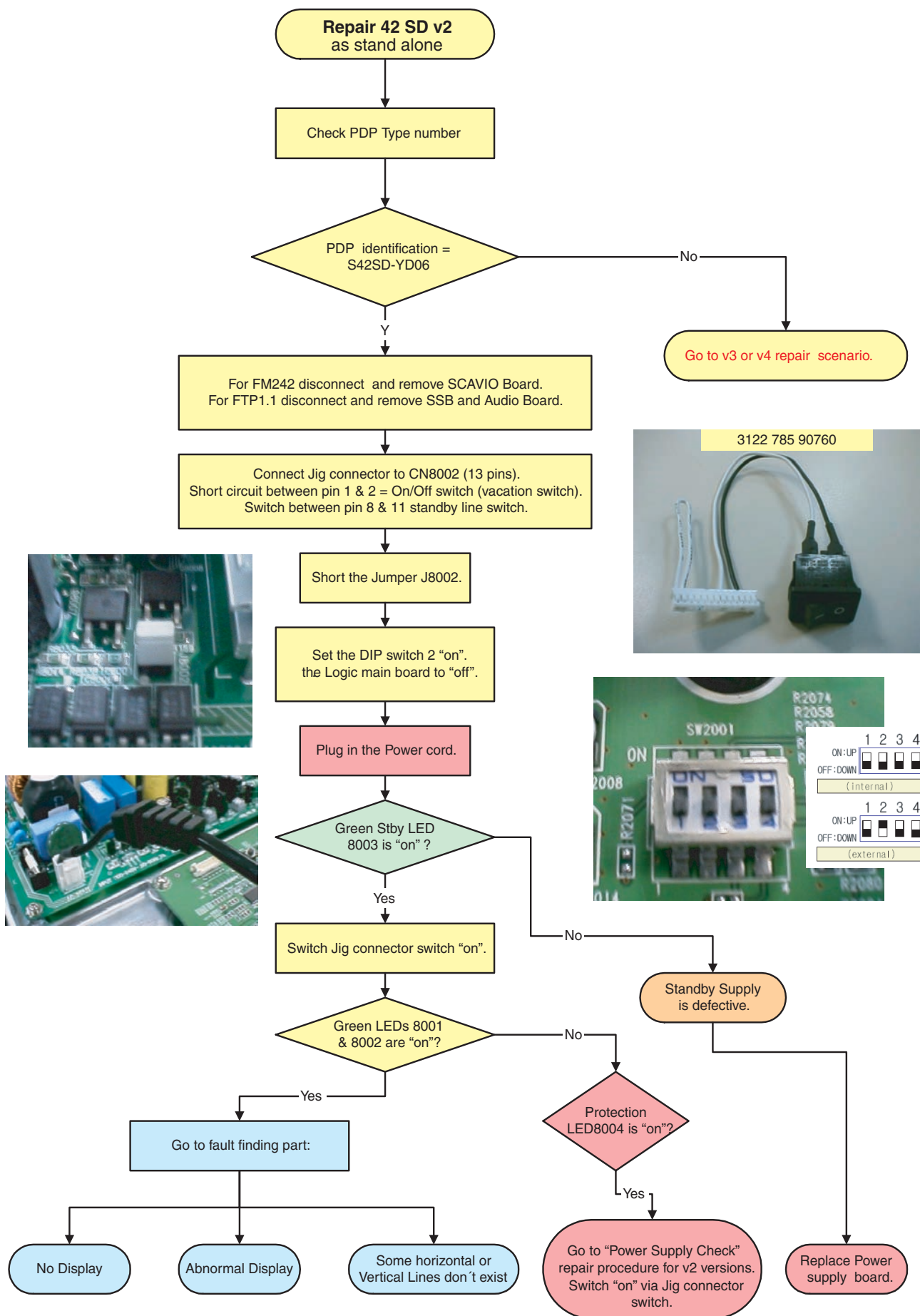


Figure 5-6 Repair scenario v2 stand alone panels

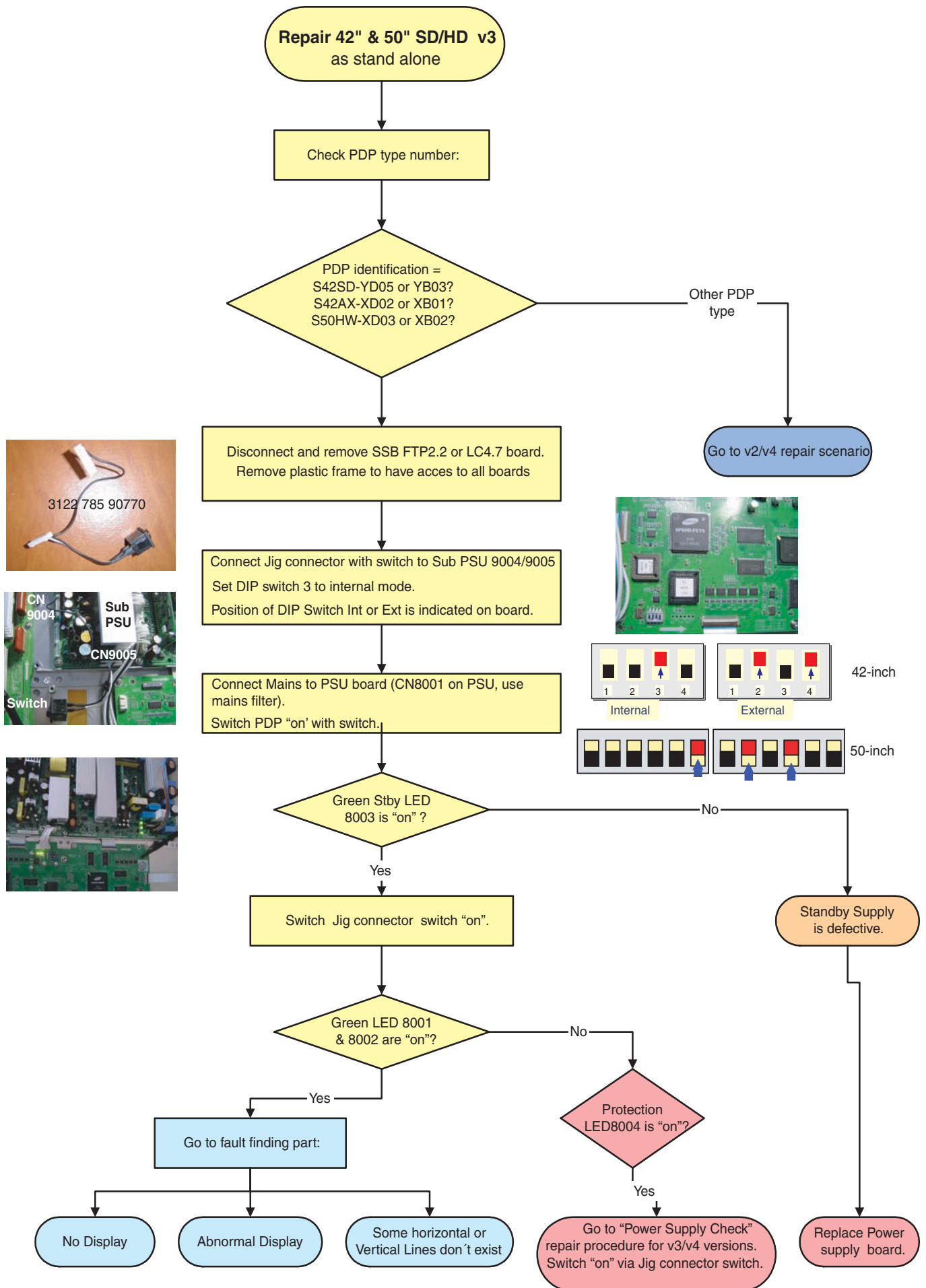


Figure 5-7 Repair scenario 42"/50" SD/HD v3 stand alone panels

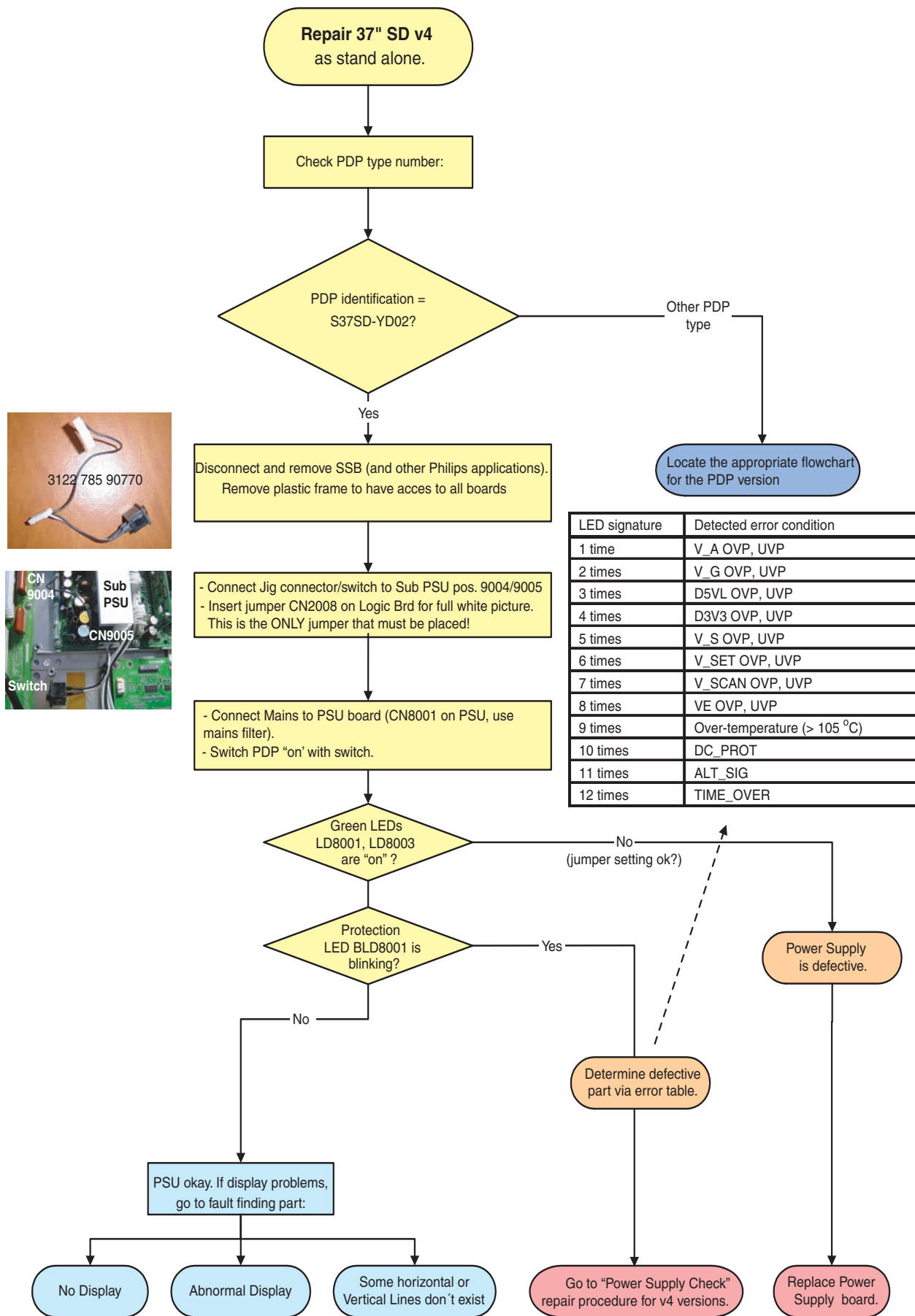


Figure 5-8 Repair scenario 37" SD v4 stand alone panels

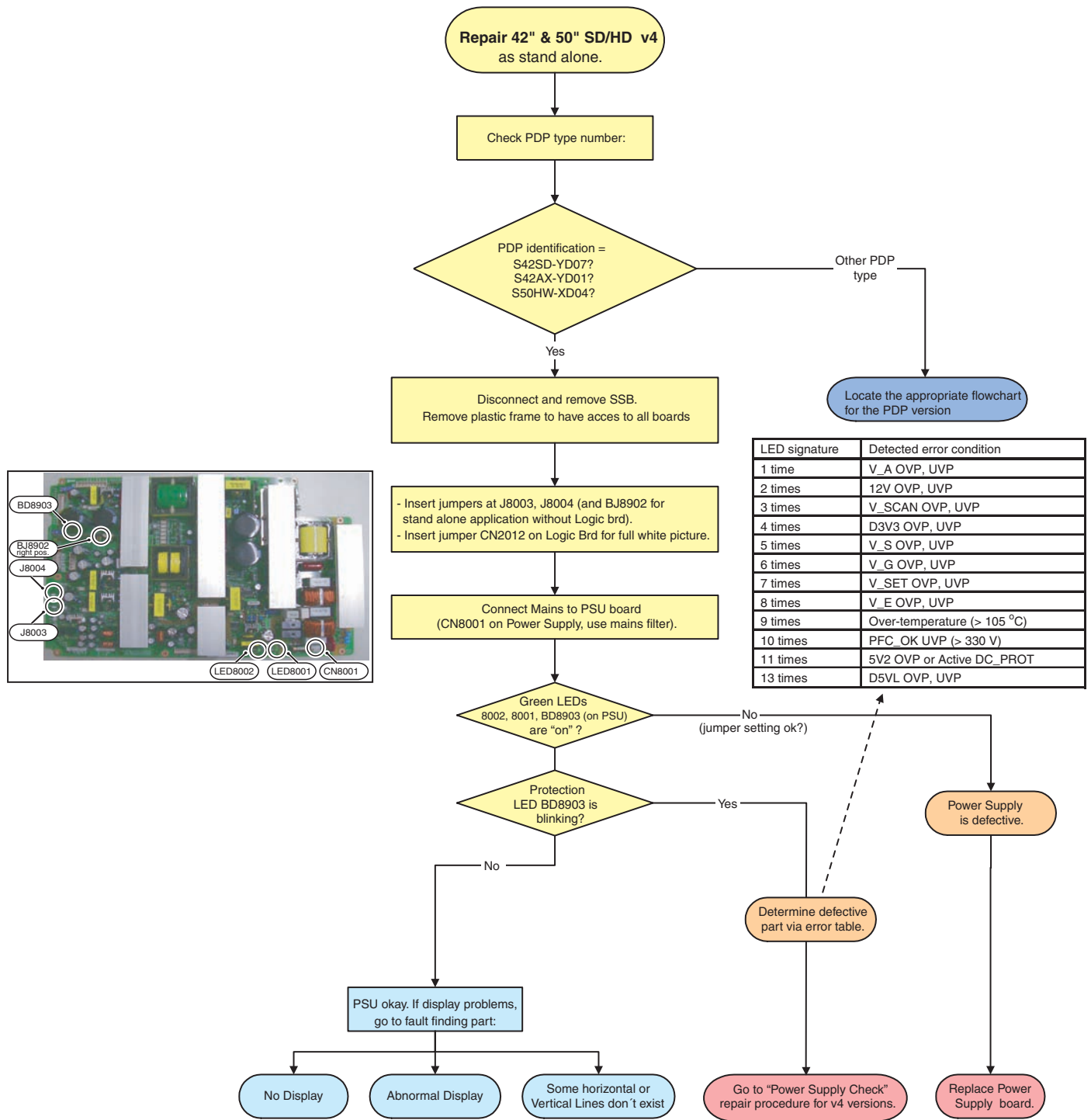


Figure 5-9 Repair scenario 42"/50" SD/HD v4 stand alone panels

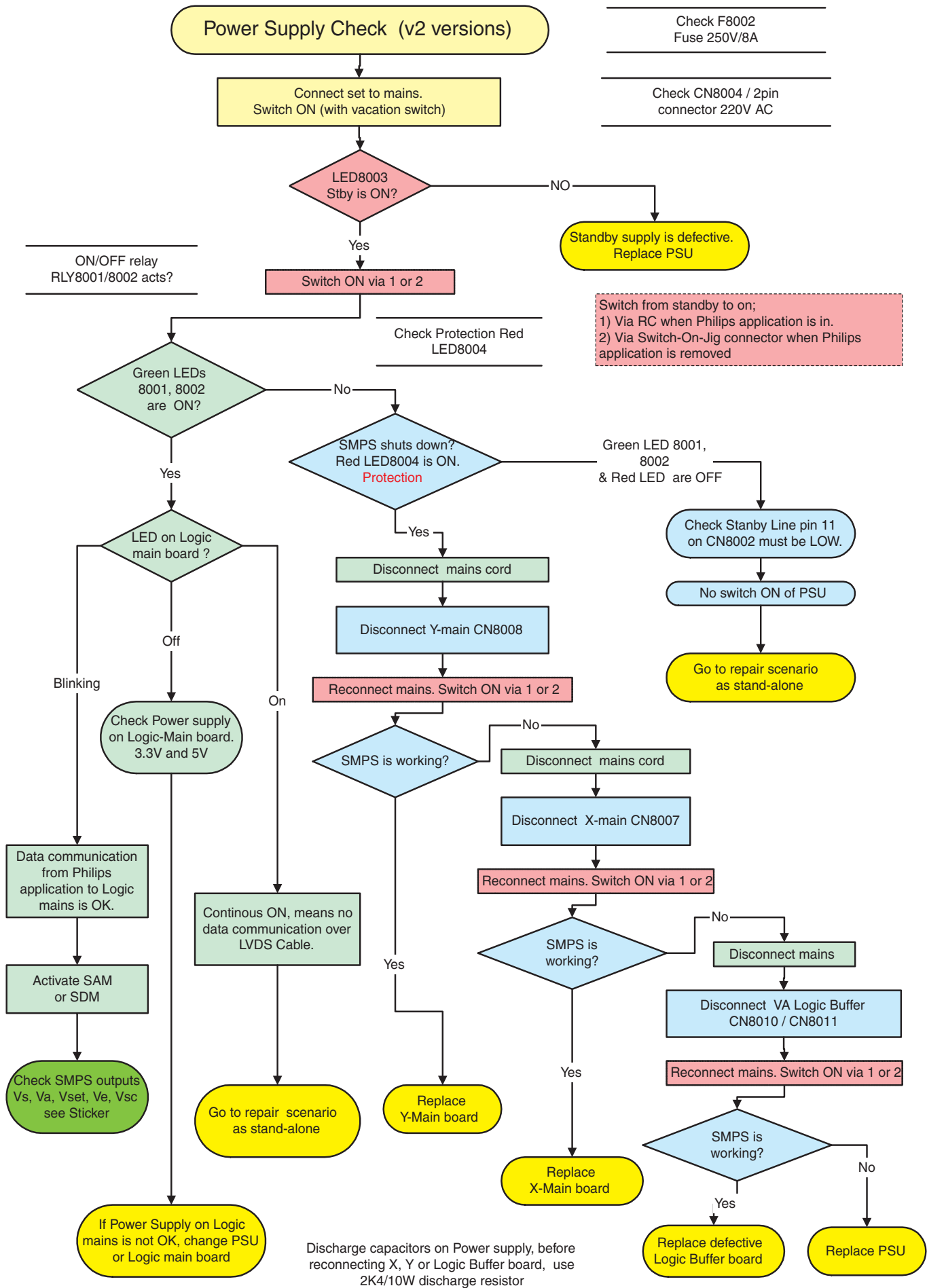


Figure 5-10 Power Supply Check for v2 models

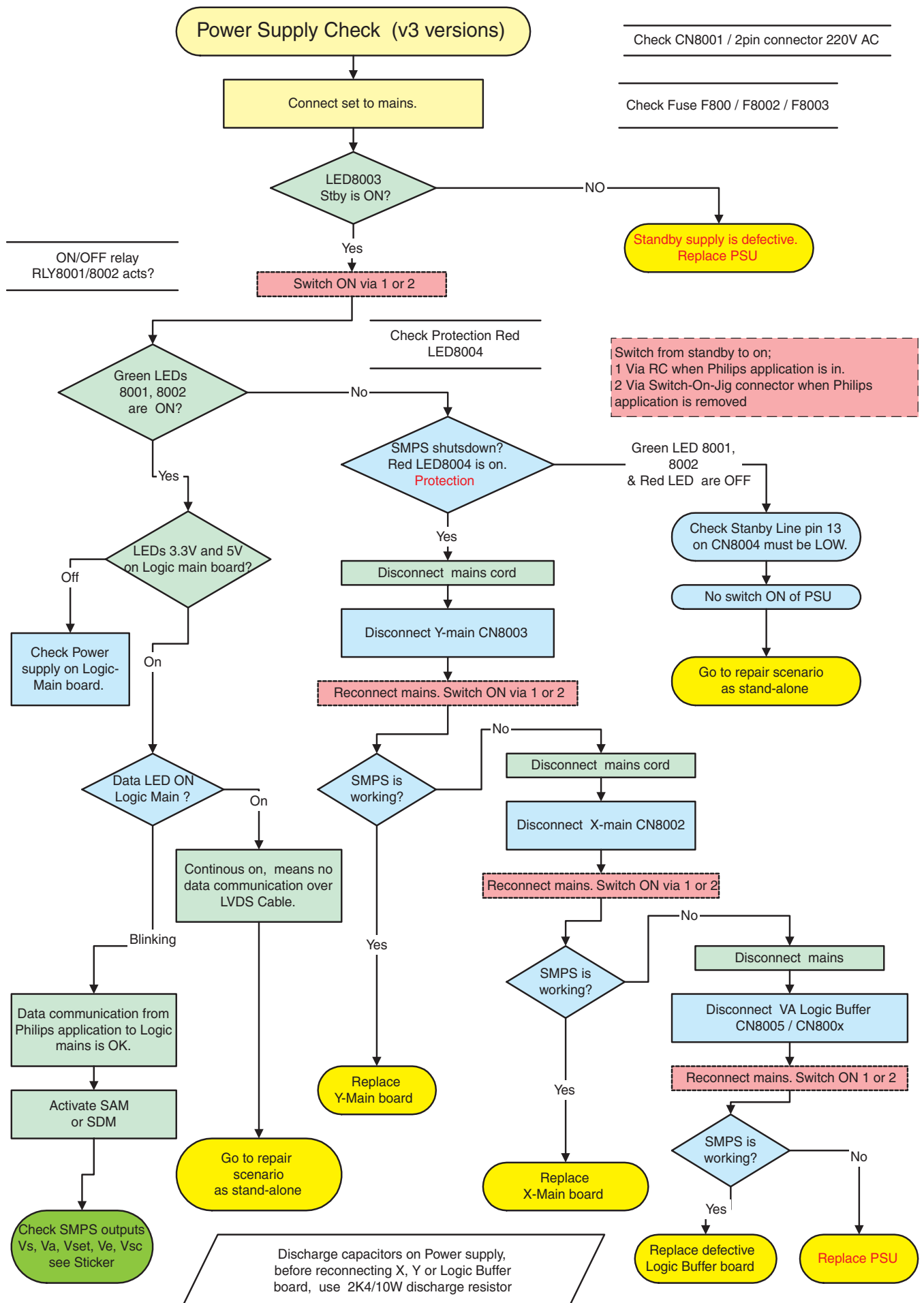


Figure 5-11 Power Supply Check for v3 models

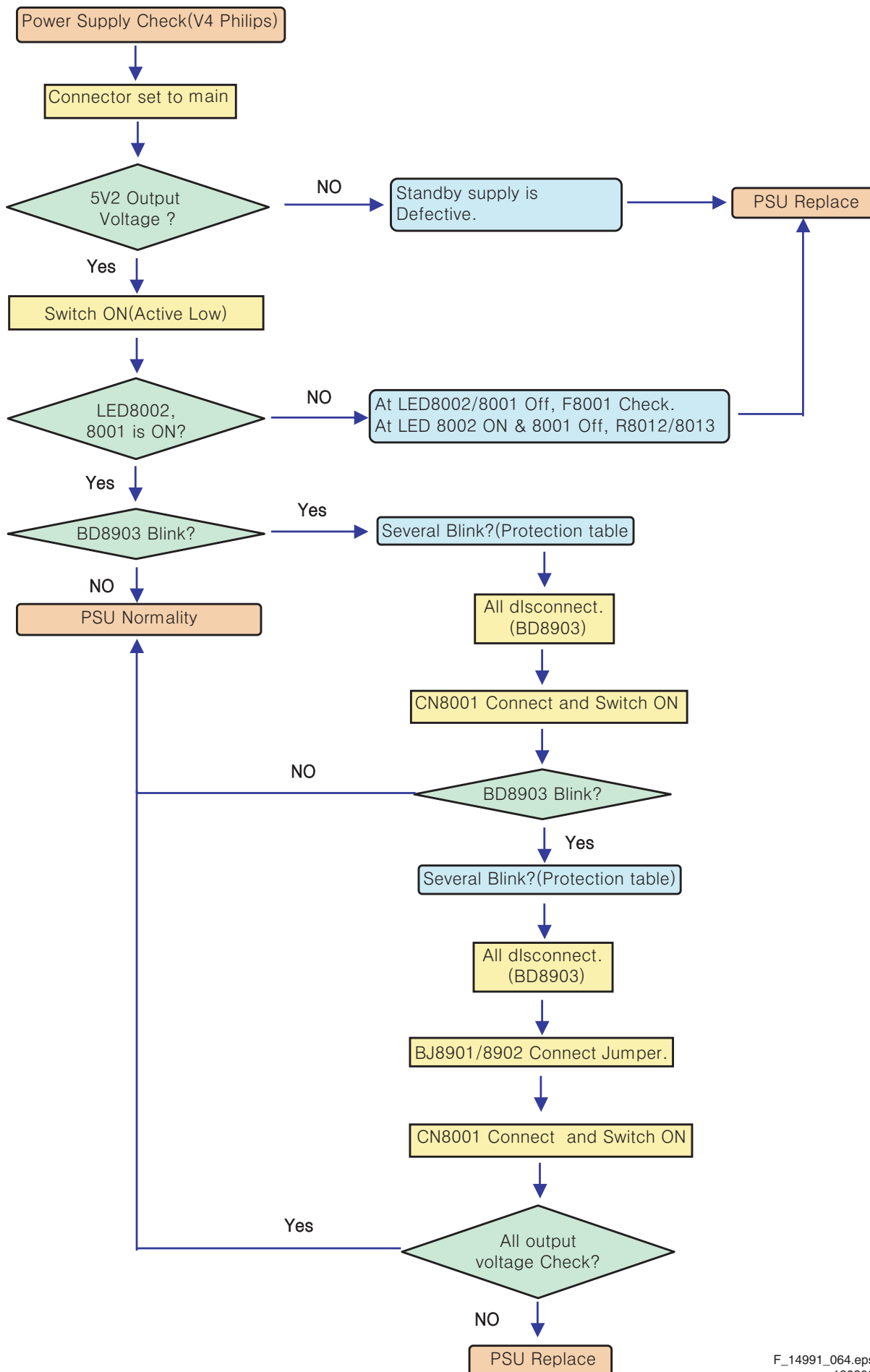


Figure 5-12 Power Supply Check for v4 models

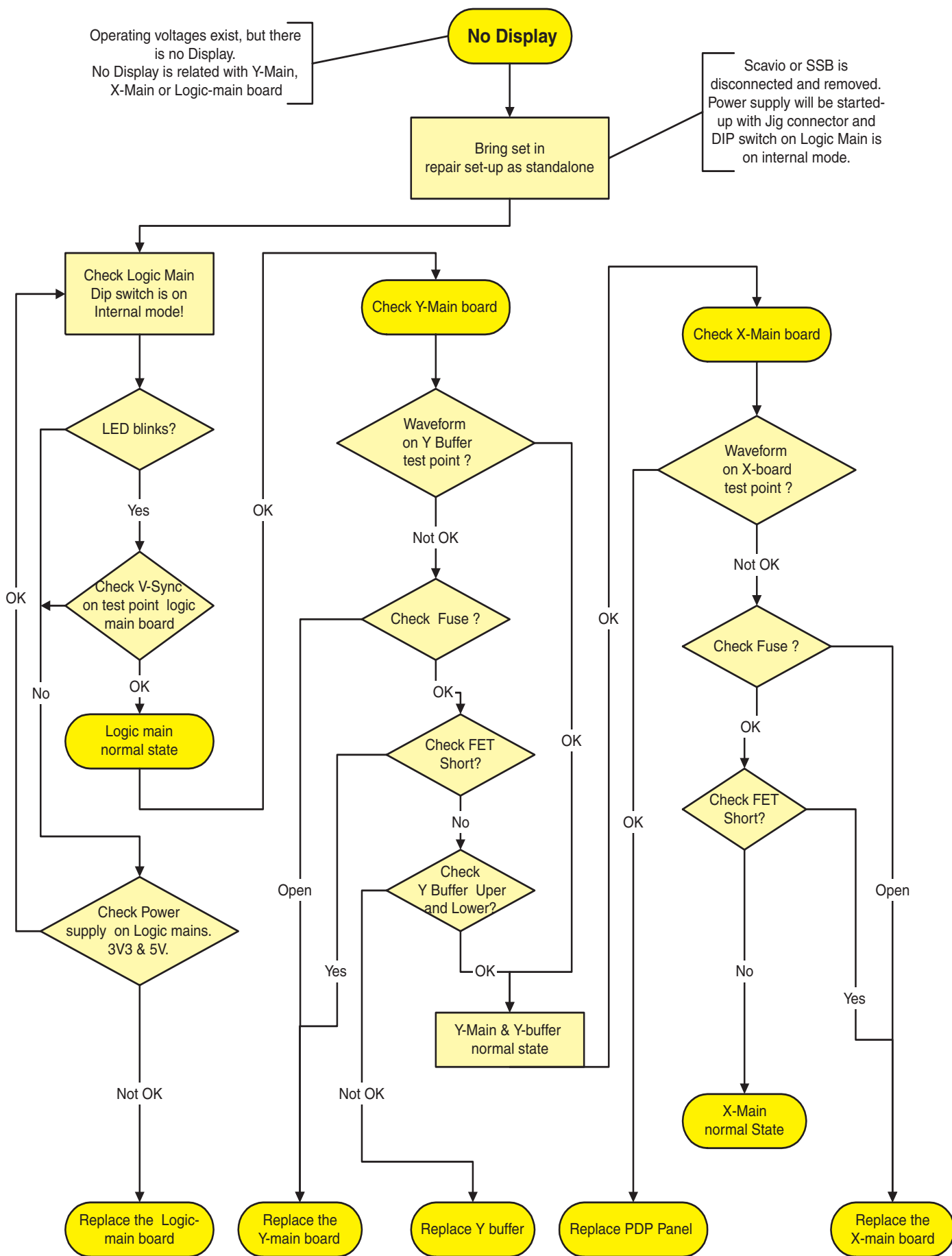


Figure 5-13 Fault symptom: "No Display"

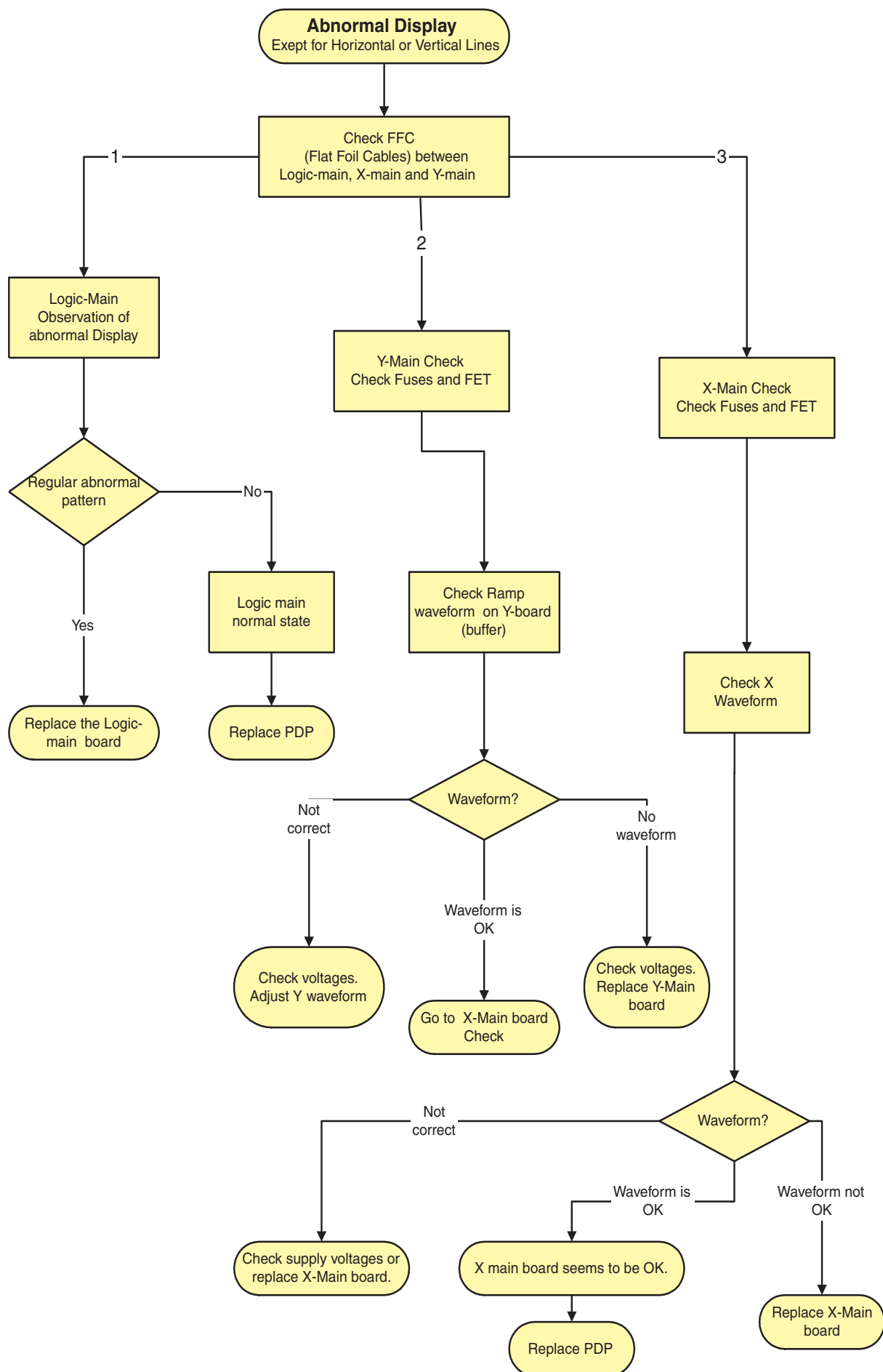


Figure 5-14 Fault symptom: "Abnormal Display"

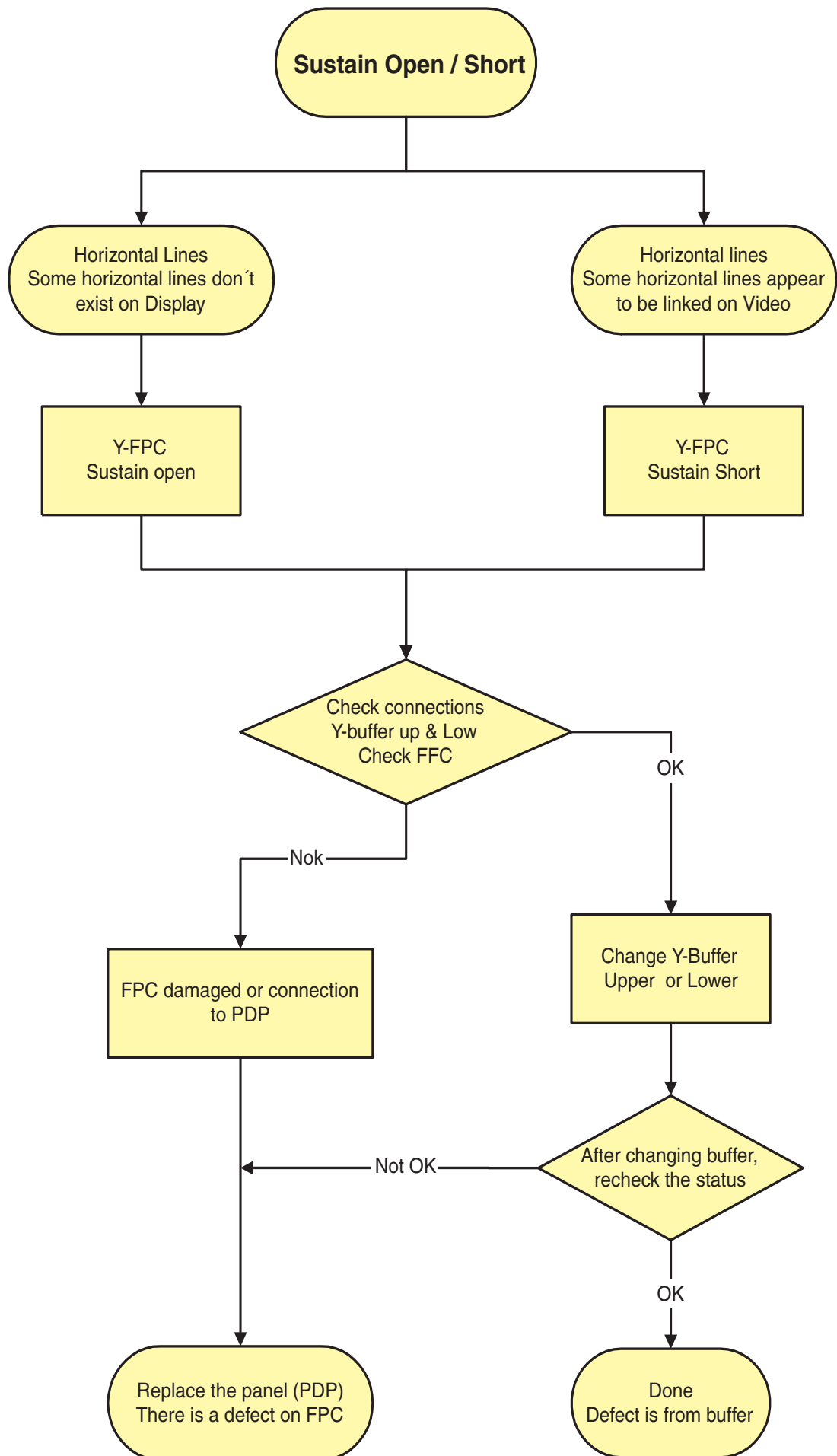


Figure 5-15 Fault symptom: "Sustain open / short"

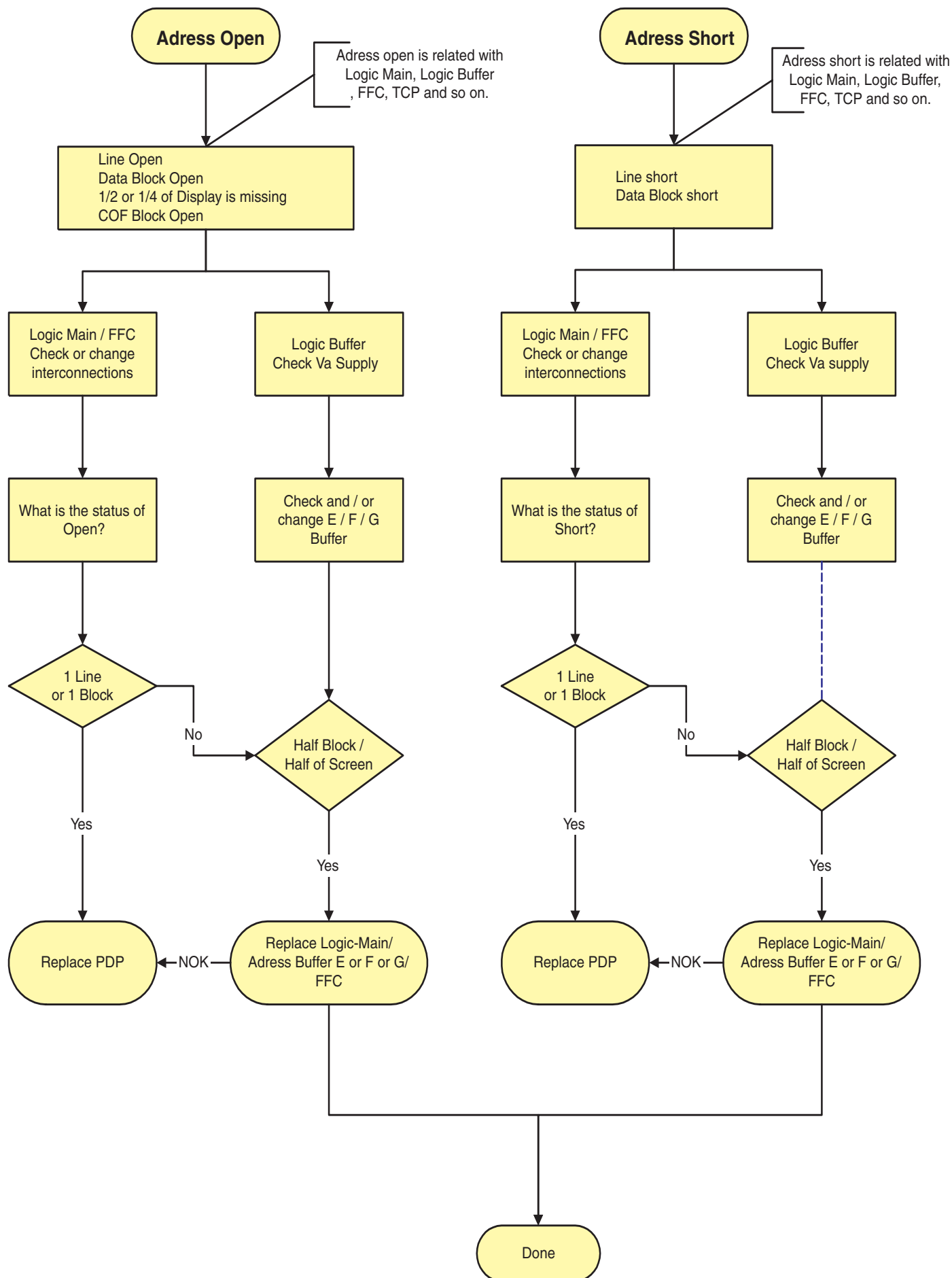


Figure 5-16 Fault symptom: "Address open / short"

5.3 Defect Description Form

This form must be used by the workshops for warranty claims:

DDF FLAT TV (panels & boards) version 1.1				Date last modified: 08/03/2005		
To be filled in by <u>WORKSHOP / WORK CENTER</u>						
Country:		<div style="font-size: 24pt; font-weight: bold;">Philips</div> <div style="font-size: 18pt; font-weight: bold;">LCD & Plasma</div> <div style="border: 1px solid black; padding: 5px; font-weight: bold;">DEFECT DESCRIPTION</div> <div style="border: 1px solid black; padding: 5px; font-weight: bold;">FORM</div>		Type nr./Model nr. set		
Customer Account nr.:				Serial nr. set		
				Type nr. display		
Job sheet nr.:				Serial nr. display		
		Part nr display (12nc)				
		Return number		0170 _ _ _ _ _		
GENERAL REPAIR DATA	Condition	<input type="checkbox"/> Constantly <input type="checkbox"/> Intermittently <input type="checkbox"/> After a while <input type="checkbox"/> In a hot environment <input type="checkbox"/> In a cold environment <input type="checkbox"/> Other :				
	Symptom(s)	<input type="checkbox"/> No backlight <input type="checkbox"/> No picture <input type="checkbox"/> Picture too bright <input type="checkbox"/> Shading / smearing on picture <input type="checkbox"/> Only partial picture <input type="checkbox"/> Unstabel picture <input type="checkbox"/> Flickering / flashing picture <input type="checkbox"/> Lines across/down image <input type="checkbox"/> Inactive row(s) <input type="checkbox"/> Inactive column(s) <input type="checkbox"/> Missing colour(s) <input type="checkbox"/> Other:				
PANEL REPAIR	Pixel Defect(s):	<input type="checkbox"/> Dark dots <input type="checkbox"/> Bright dots	Qty of dots :	Mark Defect(s)	----- Picture ----- Insert picture or mark defect !	
	Symptoms	Following defect symptoms are out of warranty: <div style="display: flex; justify-content: space-between;"> <div> <ul style="list-style-type: none"> • Broken glass • Scratch(es) on display </div> <div> <ul style="list-style-type: none"> • Number of dark/bright pixels within spec. • Burn in (only for Plasma TV) </div> </div>			These symptoms are not claimable.	
BOARD REPAIR	For Plasma TV repair only		Spare Part Nr. New Board	Barcode Nr. Defect Board	Barcode Nr. Replaced Board	
		1.				
		2.				
		3.				
		4.				
To be filled in by <u>EUROSERVICE</u>		RMA number:		Date of receipt:		
Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected. Note 2: Please fill out this form <u>completely</u> and correctly, otherwise Euroservice is unable to fulfil the repair request!						
Owner: PHILIPS CE EUROSERVICE						
DE10WEG						

Figure 5-17 Defect Description Form (DDF)

6. Block Diagrams, Test Point Overview, and Waveforms

- Index of this chapter:
- 6.1 Block Diagram for Logic Circuit
 - 6.2 PSU Board diagram

6.1 Block Diagram for Logic Circuit

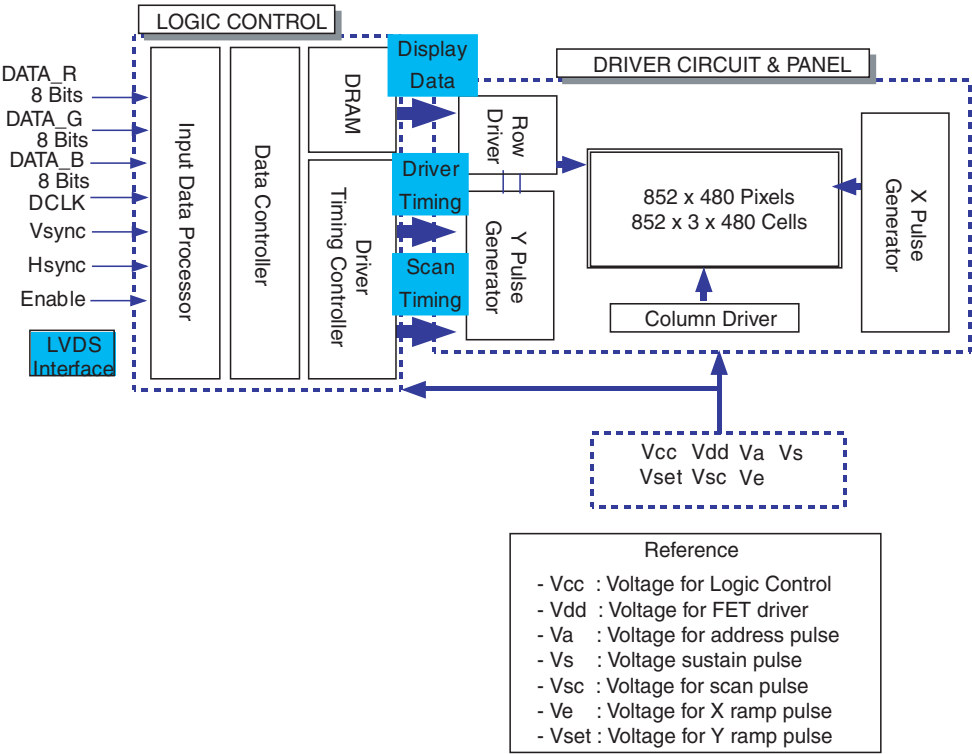


Figure 6-1 Block diagram (37" SD v4)

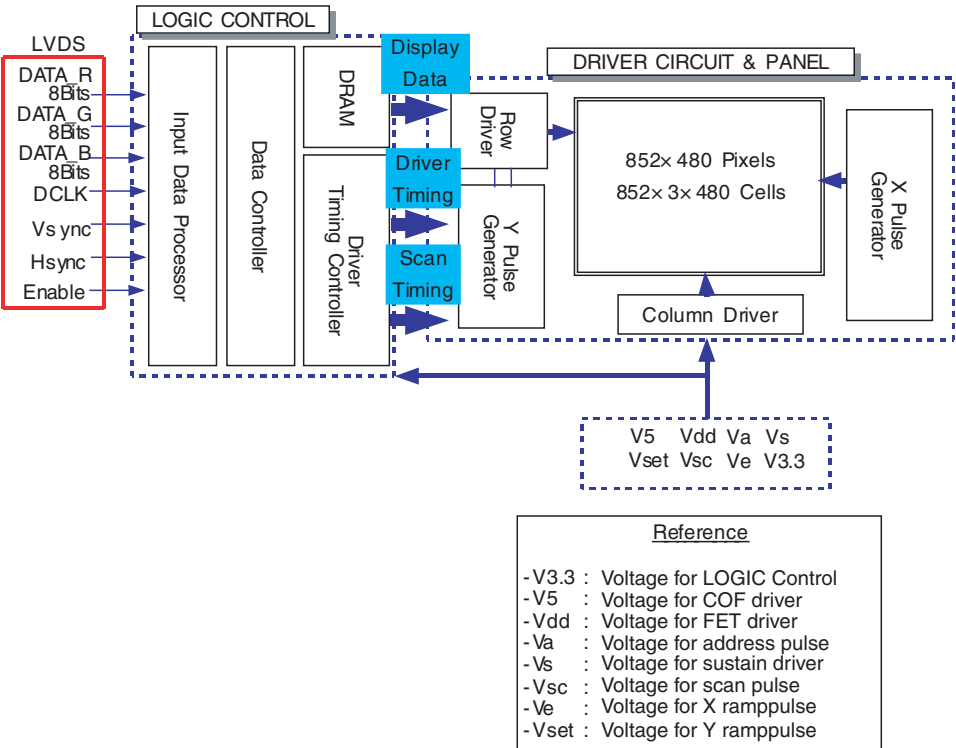
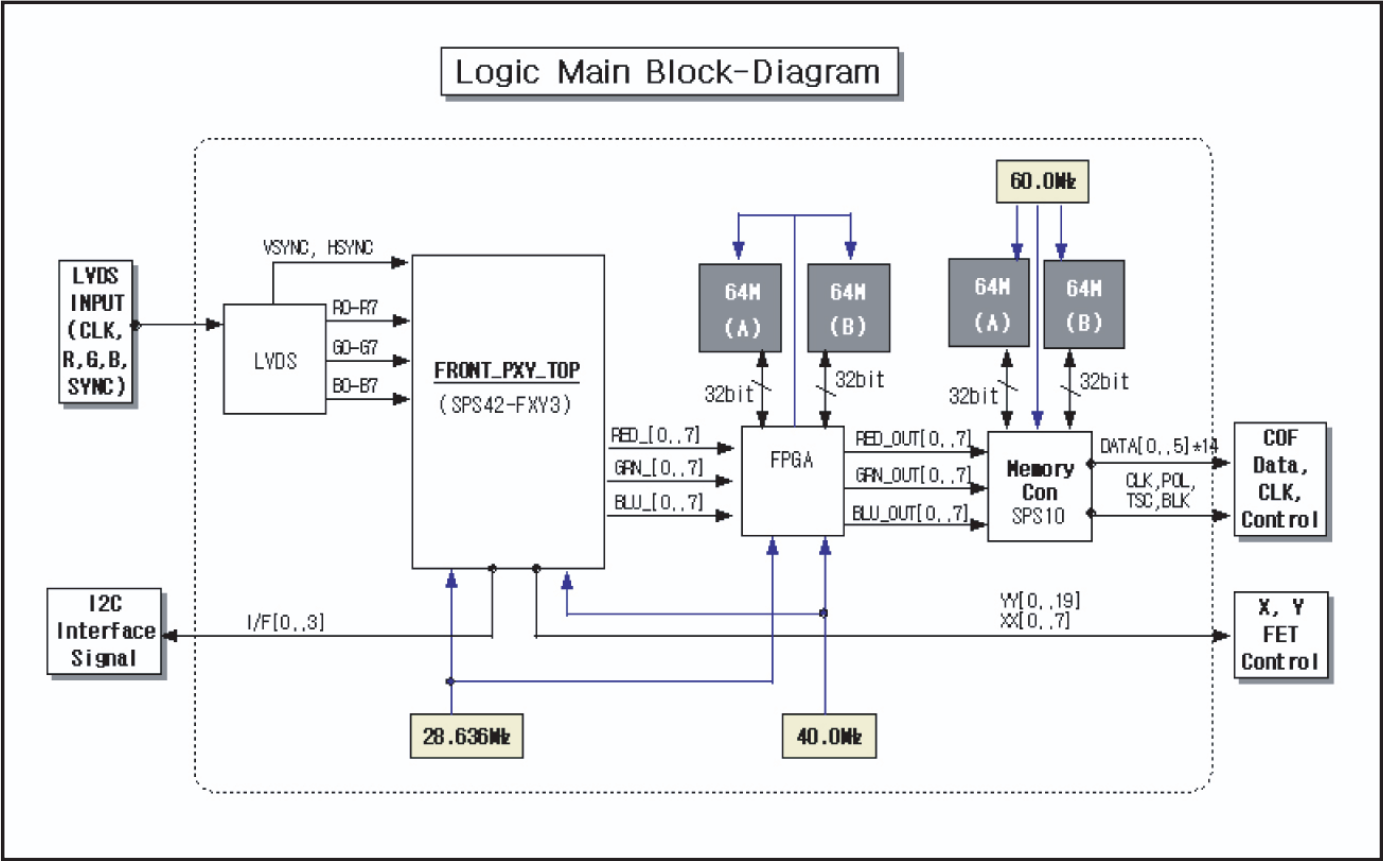
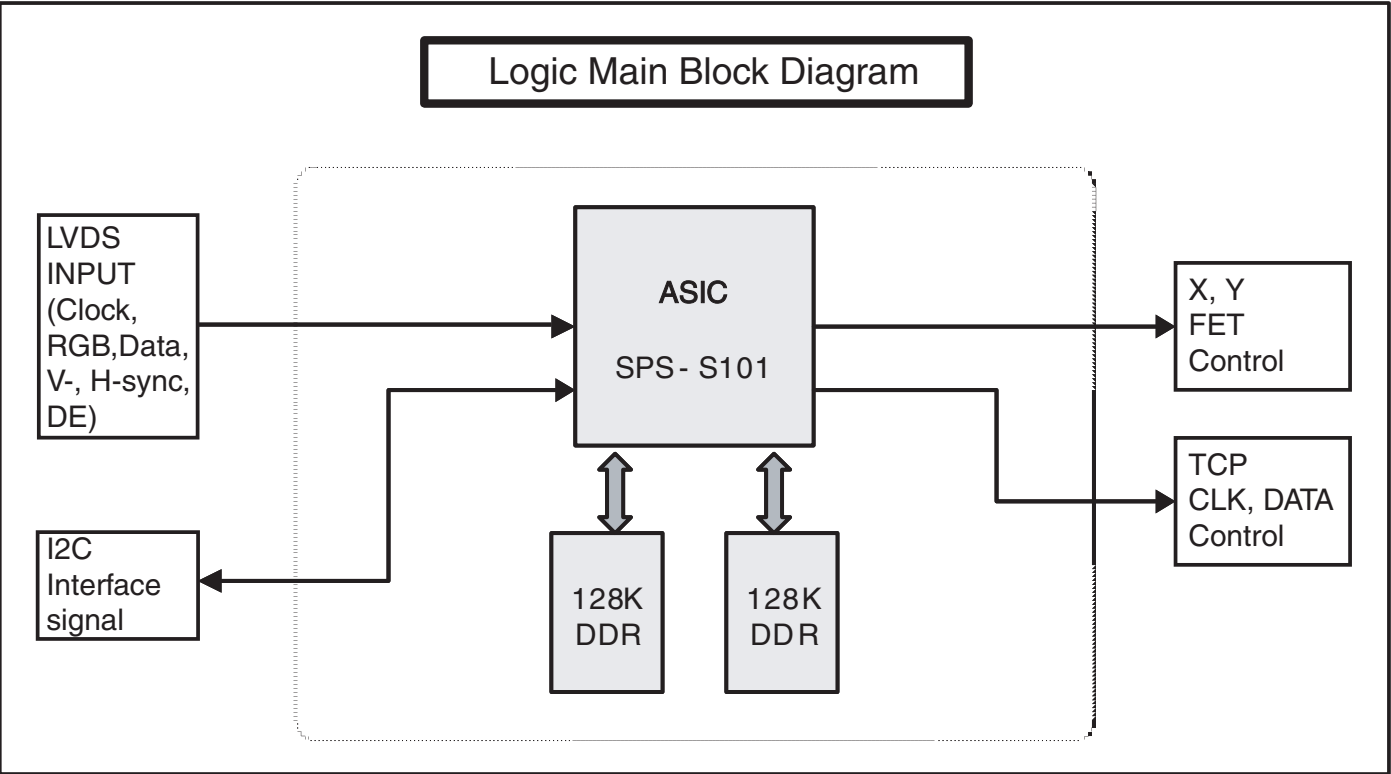


Figure 6-2 Block diagram (42" SD v2)



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Figure 6-3 Block diagram (42" SD v3)



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180705

Figure 6-4 Block diagram (42" SD v4)

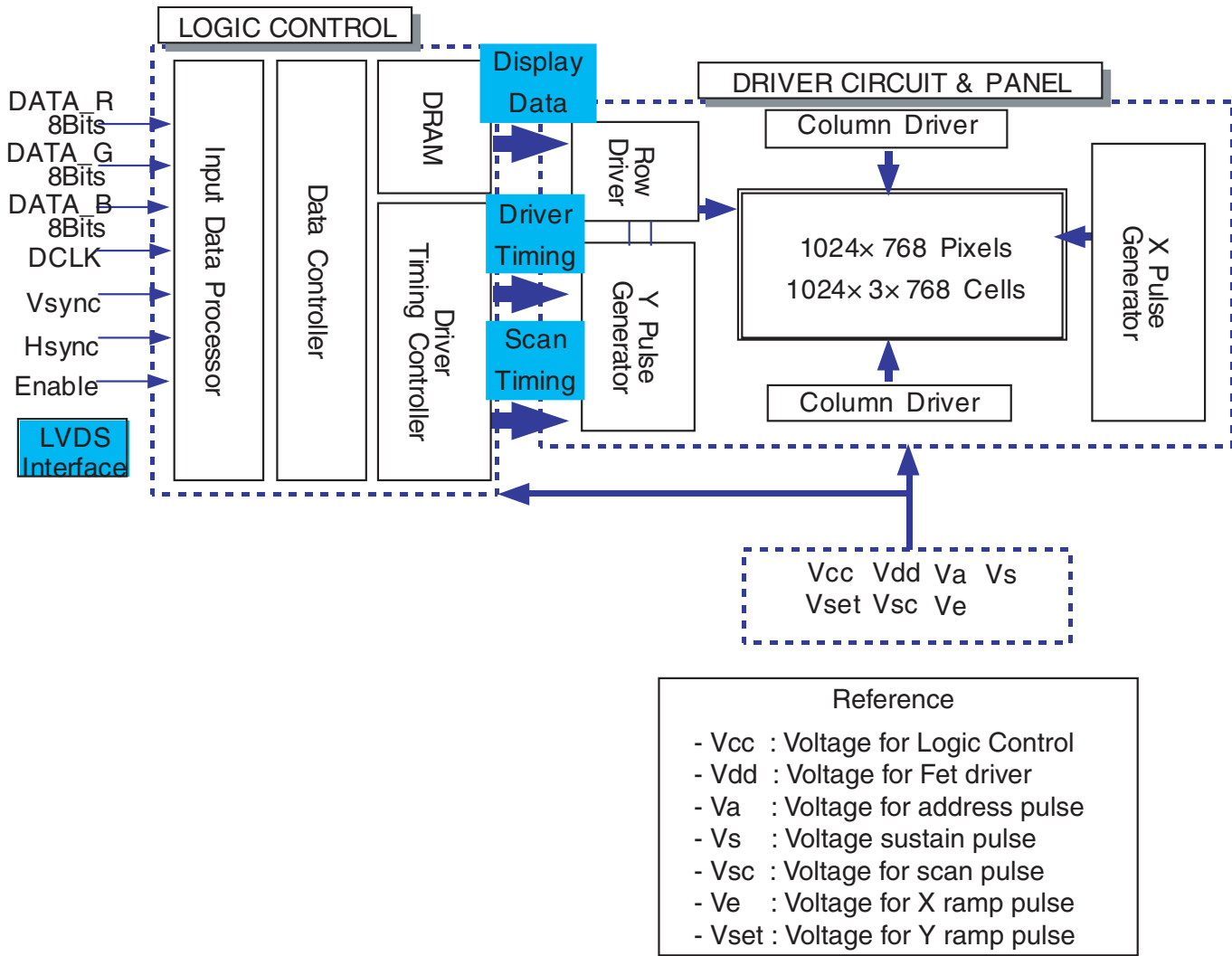


Figure 6-5 Block diagram (42" HD v3)

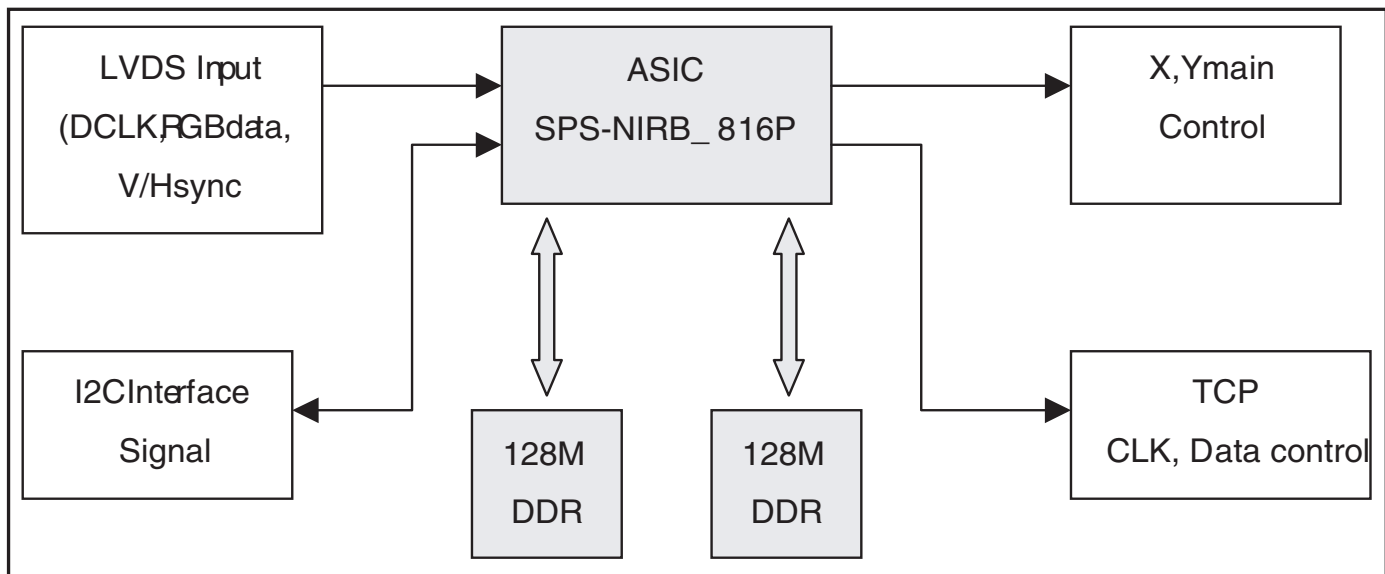
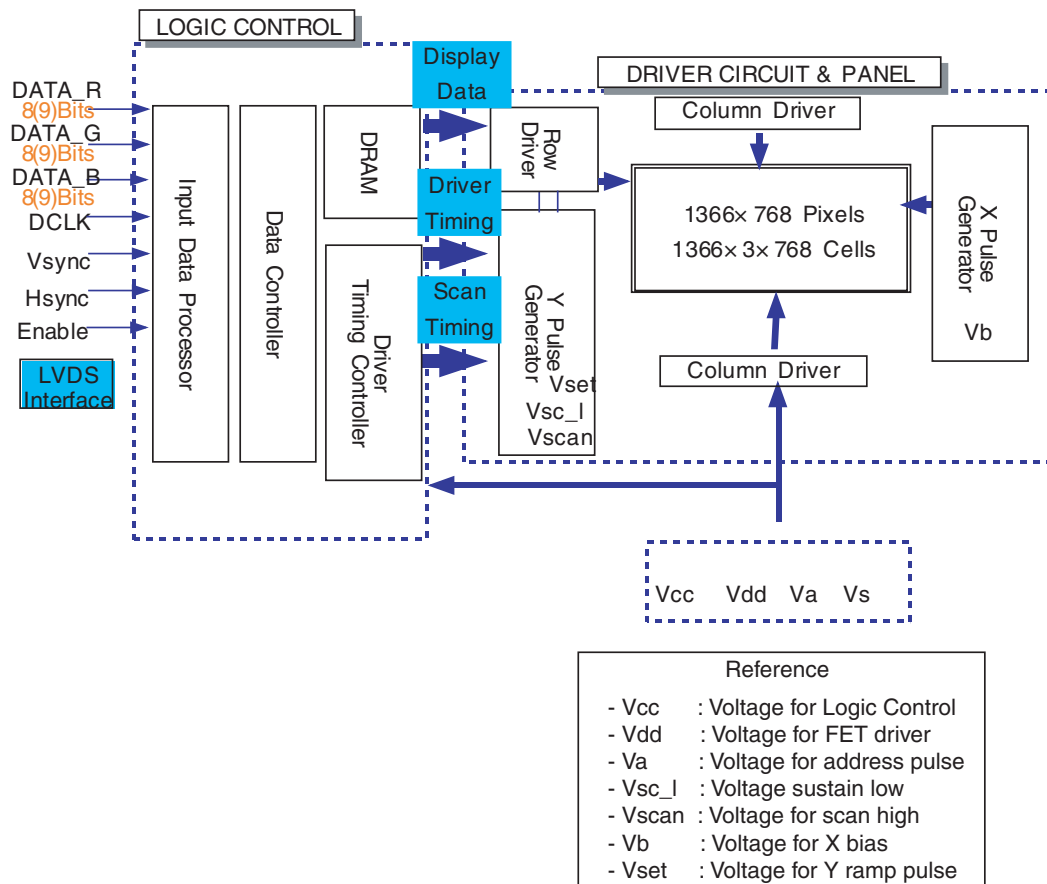
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Figure 6-6 Block diagram (42" HD v4)



6.2 PSU Board diagram

6.2.1 PSU 37" SD v4

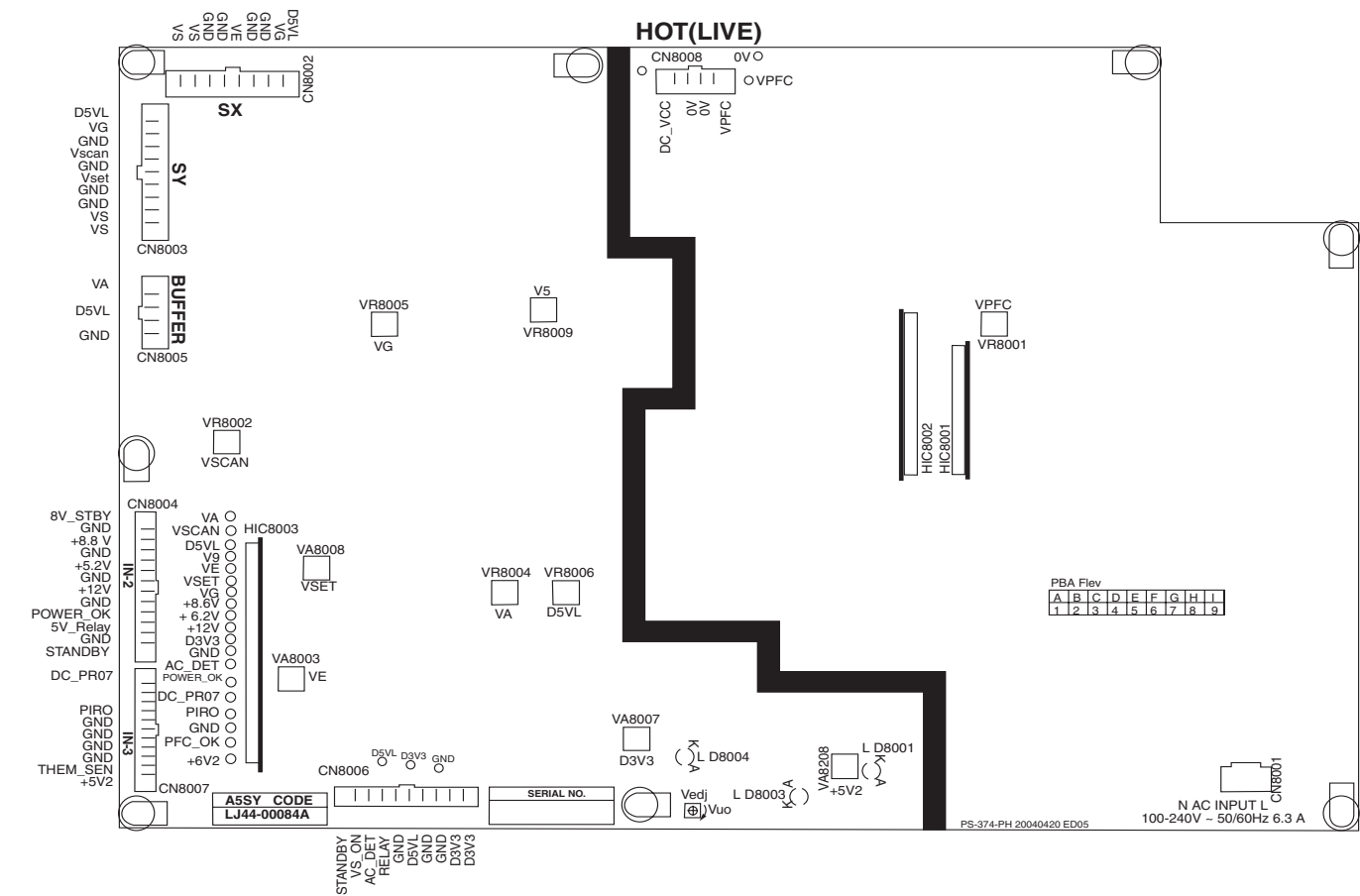


Figure 6-9 PSU layout

Table 6-1 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Nominal Load)	Output Voltage Variable Point
2	VS	170 V	160 V ~ 185 V
3	VA	70V	60 V ~ 80 V
4	VE	180 V	165 V ~ 195 V
5	VSET	173 V	160 V ~ 180 V
6	VSCAN	-160 V	-145 V ~ -175 V
7	D5VL	5.2 V	5.0 V ~ 6.0 V
8	D3V3	3.3 V	2.8 V ~ 3.8 V
9	VCC	15 V	Fixed
10	5V2	5.4 V	4.5 V ~ 5.6 V
11	9V_Standby	8.5 V ~ 9.5 V	Fixed

Check voltage label on the PDP for correct values.

6.2.2 PSU 42" SD v2

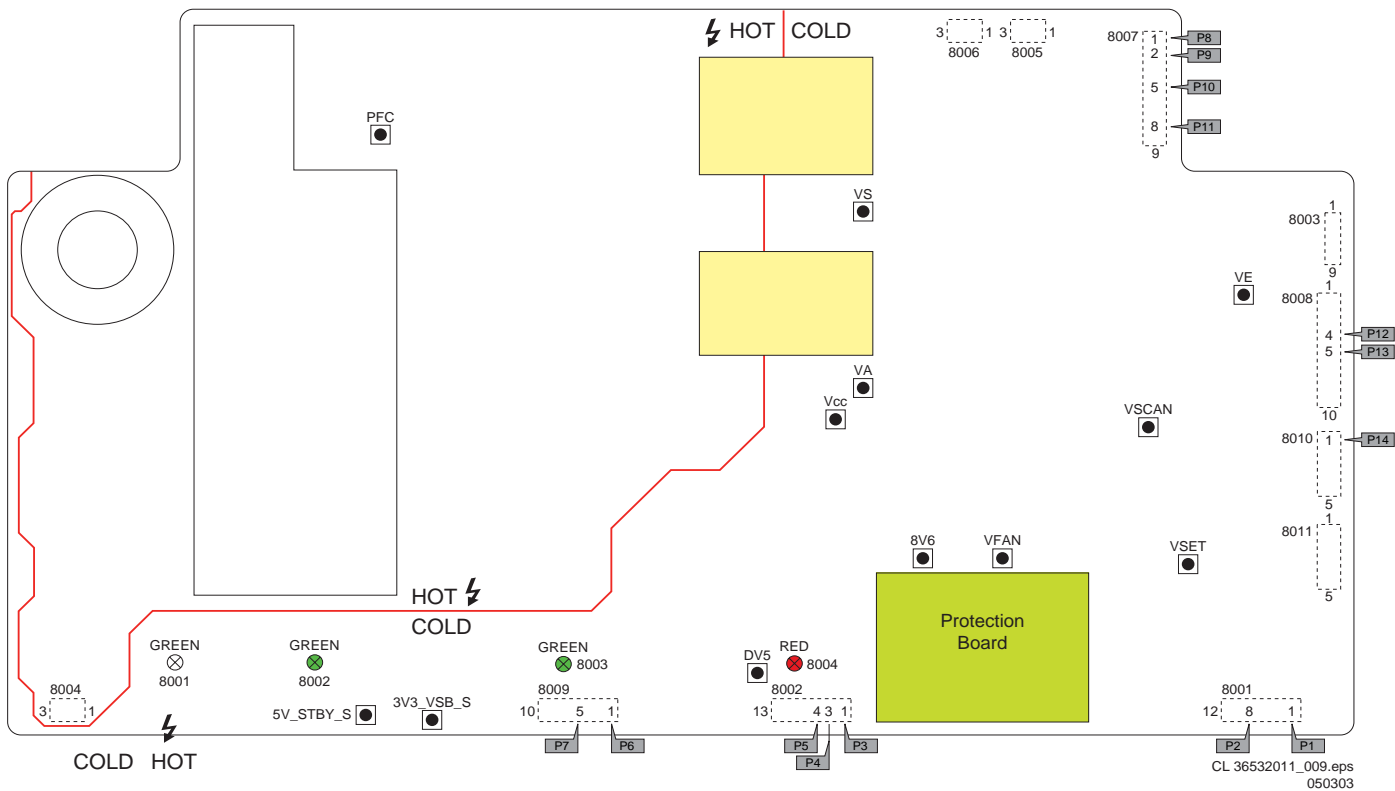


Figure 6-10 PSU layout

Table 6-2 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Nominal Load)	Output Voltage Variable Point
1	Vs	87V	78V ~ 92V
2	Va	79V	72V ~ 86V
3	Ve	107V	100V ~ 120V
4	Vset	93V	75V ~ 95V
5	Vscan	79V	65V ~ 85V
6	Vg	15V	Fixed
7	D5V	5.2V	5V ~ 5.6V
8	D3V3	3.3V	2.8V ~ 3.7V
Check voltage label on the PDP for correct values.			

6.2.3 PSU 42" SD v3

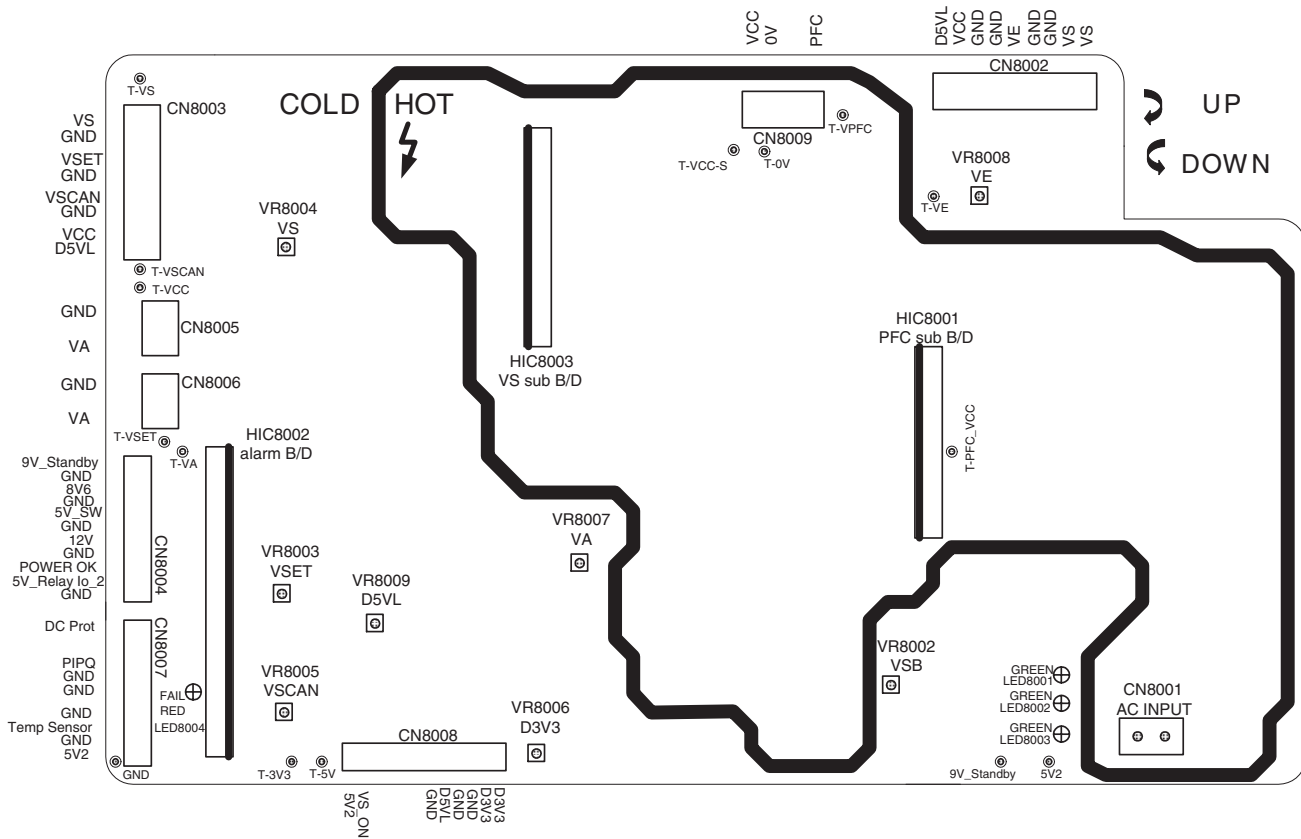


Figure 6-11 PSU layout

Table 6-3 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Nominal Load)	Output Voltage Variable Point
1	Vs	175V	160V ~ 185V
2	Va	70V	65V ~ 80V
3	Ve	160V	150V ~ 170V
4	Vset	173V	160V ~ 180V
5	Vscan	-60V	-55V ~ -75V
6	D5VL	5.2V	4.0V ~ 6V
7	D3V3	3.3V	5V ~ 5.6V
8	Vcc	15V	Fixed

Check voltage label on the PDP for correct values.

6.2.5 PSU 42" HD v3

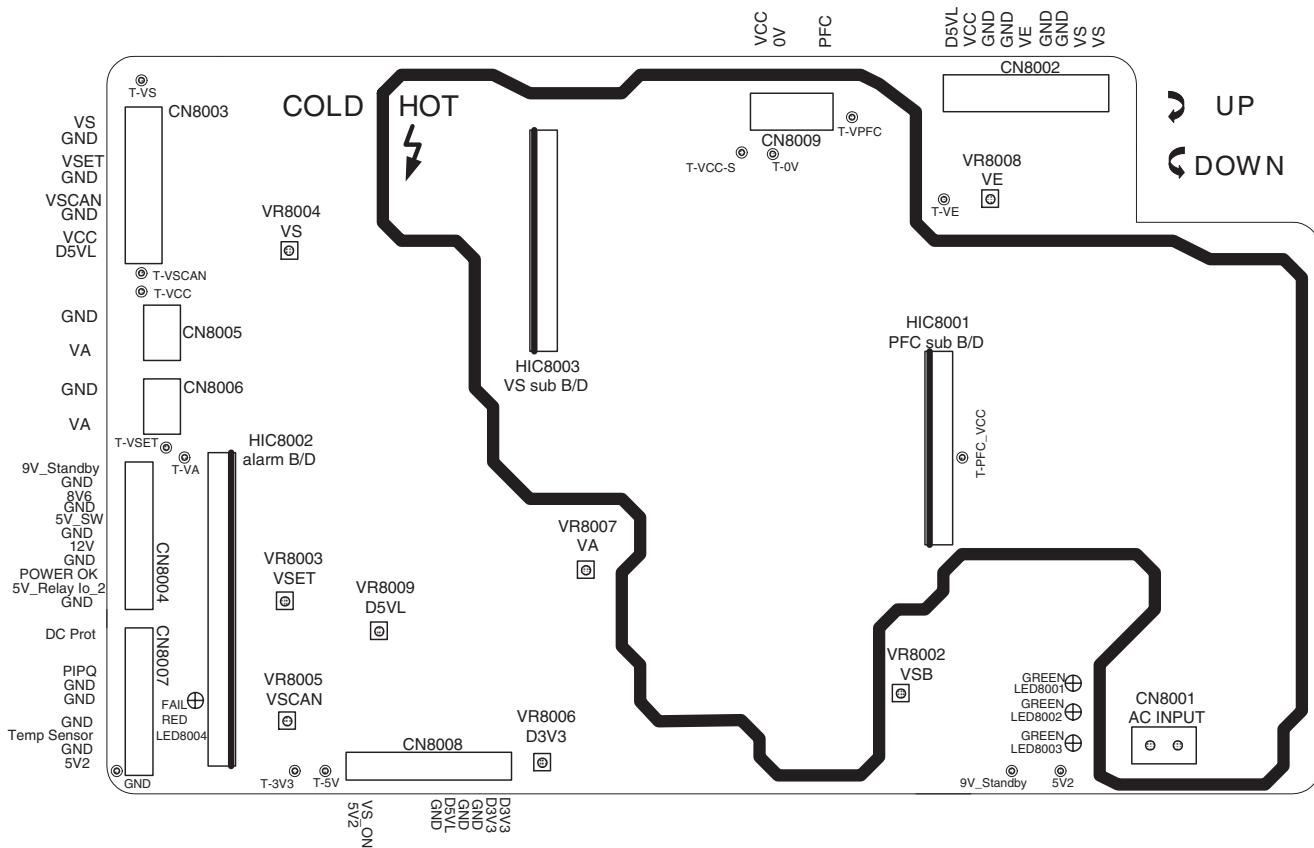


Figure 6-13 PSU layout

Table 6-5 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	PFC	385V \pm 2V	370V ~ 400V
2	VS	175V \pm 1%	160V ~ 185V
3	VA	70V \pm 1%	65V ~ 80V
4	VE	160V \pm 2%	150V ~ 170V
5	VSET	173V \pm 2%	160V ~ 180V
6	VSCAN	-60V \pm 2%	-55V ~ -75V
7	D5VL	5.2V \pm 2%	4.0V ~ 6.0V
8	D3V3	3.3V \pm 2%	2.8V ~ 4.0V
9	VCC	15V \pm 5%	Fixed
10	5V2	5.4V \pm 3%	3.5V ~ 6.0V
11	9V_Standby	8.5V ~ 9.5V	Fixed

Check voltage label on the PDP for correct values.

6.2.7 PSU 50" HD v3

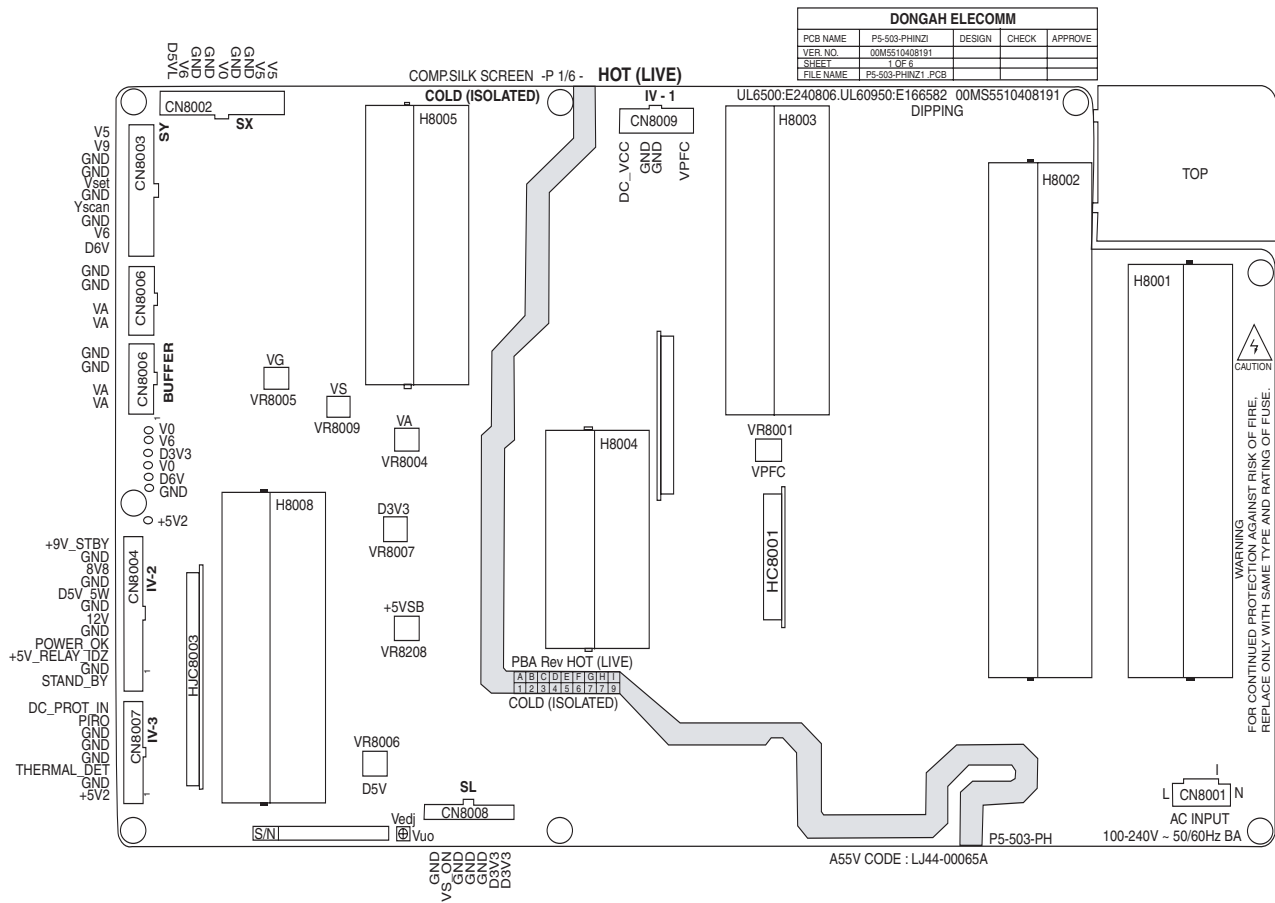


Figure 6-15 PSU layout

Table 6-7 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	PFC	385V \pm 2V	370V ~ 400V
2	VS	175V \pm 1%	160V ~ 185V
3	VA	70V \pm 1%	65V ~ 80V
4	VE	160V \pm 2%	150V ~ 170V
5	VSET	173V \pm 2%	160V ~ 180V
6	VSCAN	-60V \pm 2%	-55V ~ -75V
7	D5VL	5.2V \pm 2%	4.0V ~ 6.0V
8	D3V3	3.3V \pm 2%	2.8V ~ 4.0V
9	VCC	15V \pm 5%	Fixed
10	5V2	5.4V \pm 3%	3.5V ~ 6.0V
11	9V_Standby	8.5V ~ 9.5V	Fixed

Check voltage label on the PDP for correct values.

6.2.8 PSU 50" HD v4

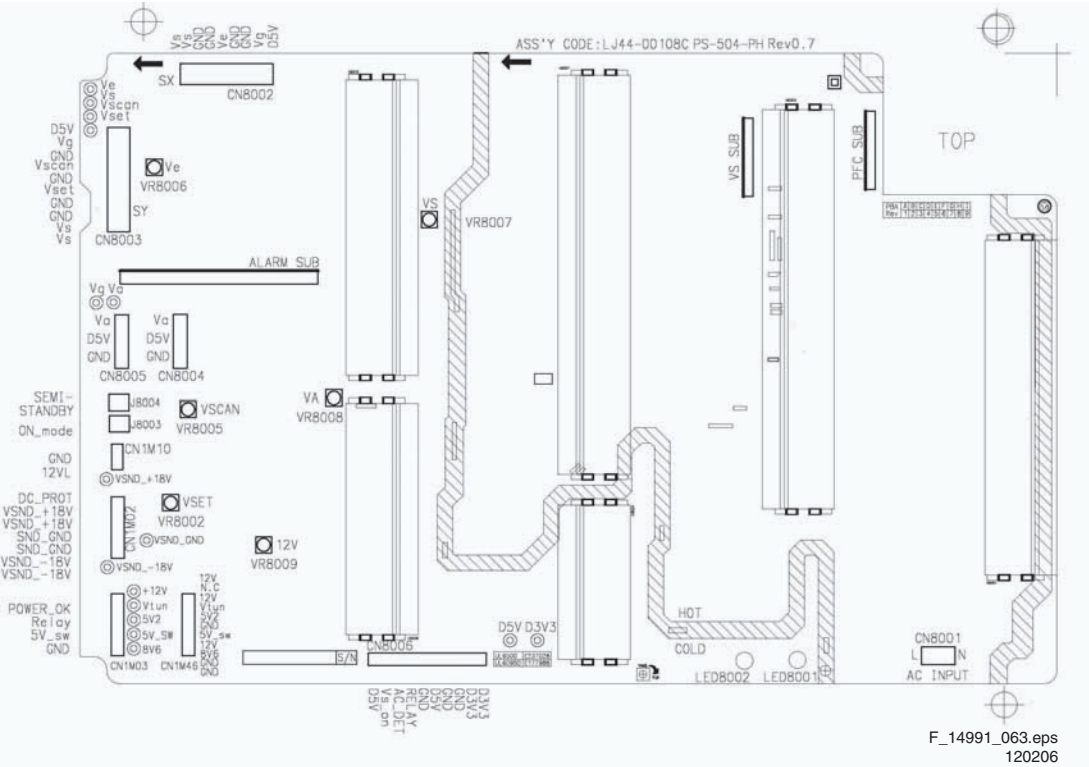


Figure 6-16 PSU layout

Table 6-8 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	VS	200V ± 1%	195V ~ 215V
2	VA	70V ± 1.5%	50V ~ 70V
3	VE	100V ± 1.5%	70V ~ 110V
4	VSET	195V ± 1.5%	180V ~ 210V
5	VSCAN	-175V ± 1.5%	-170V ~ -185V
6	VSB	5V ± 5%	Fixed
7	VG	15V ± 5%	Fixed
8	D5VL	5.2V ± 5%	Fixed
9	D3V3	3.3V ± 5%	Fixed

Check voltage label on the PDP for correct values.

7. Circuit Diagrams and PWB Layouts

Not applicable.

8. Alignments

Index of this chapter:

- 8.1 Alignments 37" SD v4
- 8.2 Alignments 42" SD v2
- 8.3 Alignments 42" SD v3
- 8.4 Alignments 42" HD v3
- 8.6 Alignments 42" HD v4
- 8.7 Alignments 50" HD v3
- 8.8 Alignments 50" HD v4
- 8.9 Alignment value overview (all screens)

Note:

- Figures can deviate due to the different model executions.

Important: Remove all non-default jumpers and reset all DIP switches, after the repair!

8.1 Alignments 37" SD v4

1. Set the pattern to Full White (place jumper CN2008 on the Logic Board).
2. Set Vsch (see Figure "Test point location LJ92-0102A") to -38V (see Figure "Waveform adjustment (Y-Board)"). Check with a digital multimeter, connected between the Y-scan test point and ground. Adjust the voltage with VR5000.
3. Check the waveform using an Oscilloscope.
 - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
 - Connect the "ODD" test point, located at the centre of Y_buffer (see Figure "Potentiometer locations LJ92-01149A"), to the other channel, and then check the first Subfield waveform of one TV-Field.
 - Check the waveform by adjusting Horizontal Division of the oscilloscope.
4. Adjust the flat time of the rising ramp of the 1st subframe to 40 μ S with VR5001 (see Figure "Rising ramp flat time adjustment").

5. Adjust the flat time of the falling ramp of the 1st subframe to 16 μ S with VR5002 (see Figure "Falling ramp flat time adjustment").
 - This is a difficult adjustment.
 - It is easier and more accurate to do the following:
 - Count 3 pulses between A and B;
 - Set the difference between A and B to 40 V; the time between C and D will then automatically be set to approximately 16 μ S
 - Settings of the oscilloscope: vertically 20VDC/div, horizontally 10 μ S/div.
6. Check with the oscilloscope if the voltage of Vsch is -38 V (see Figure "Y-scan H waveform").

Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the Reset waveform and then move to the 3rd Sub-field for adjusting.

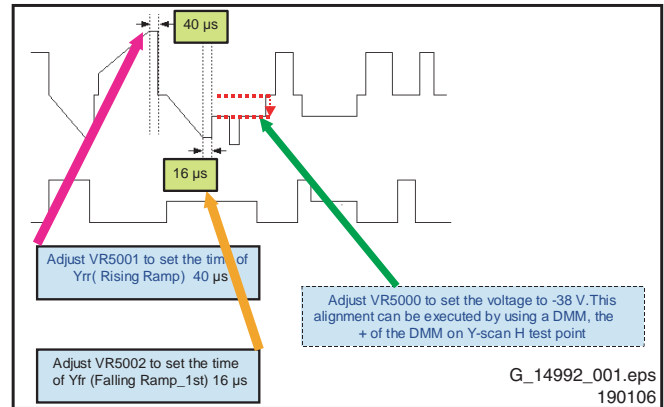


Figure 8-1 Waveform adjustment (Y-Board)

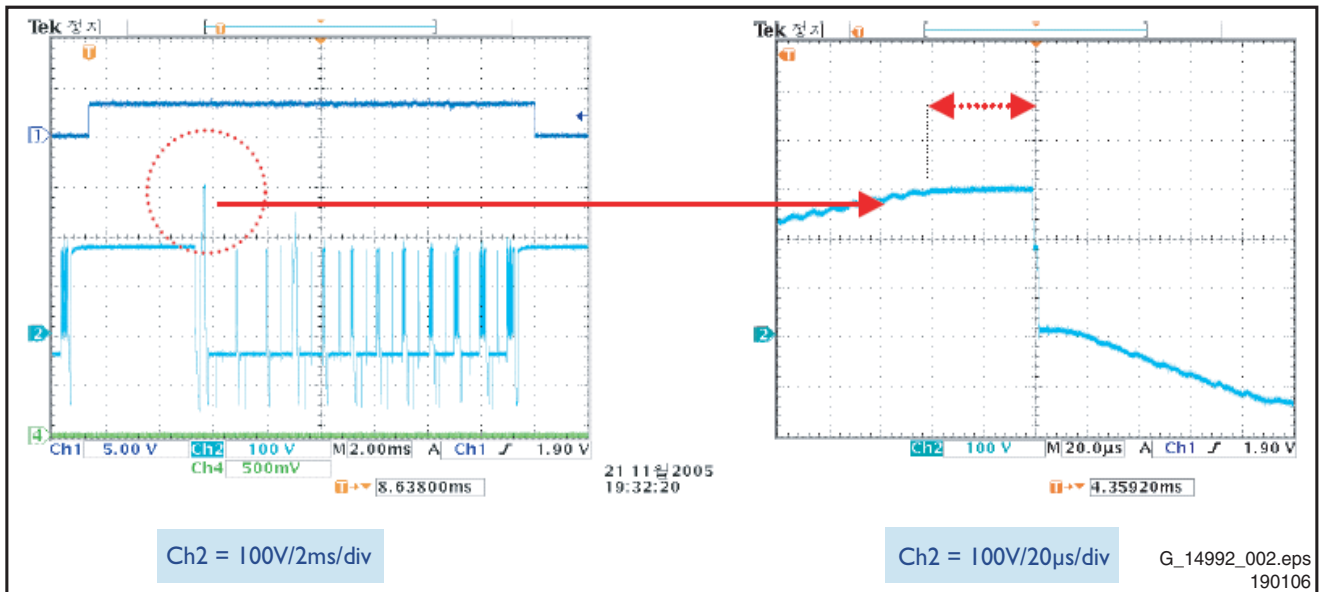


Figure 8-2 Rising ramp flat time adjustment (Y-Board)

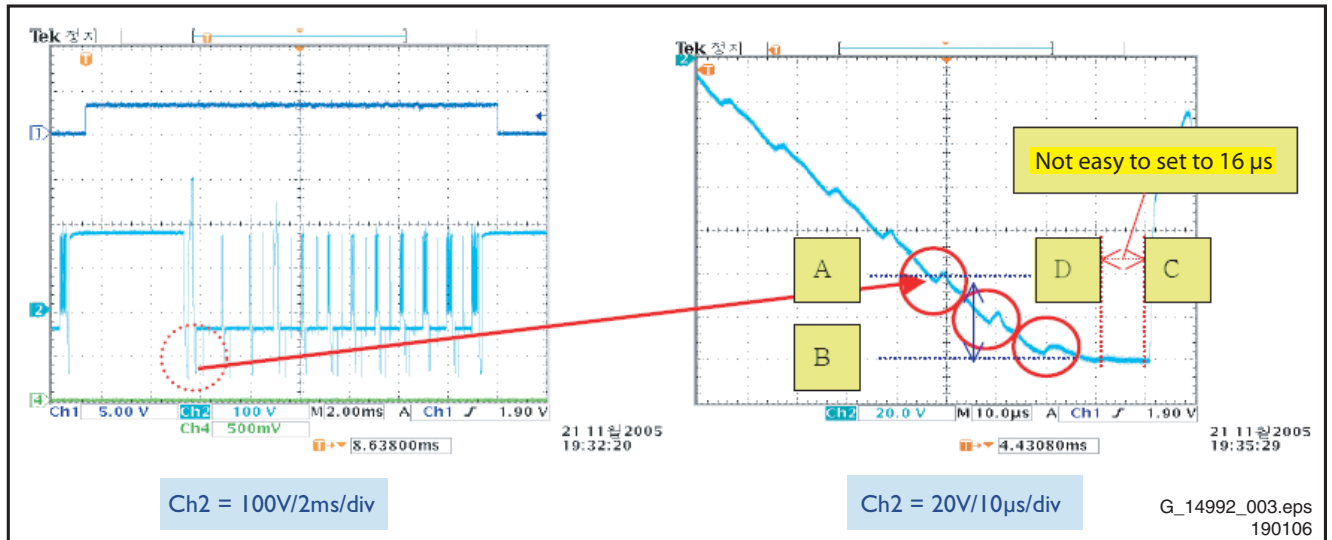


Figure 8-3 Falling ramp flat time adjustment (Y-Board)

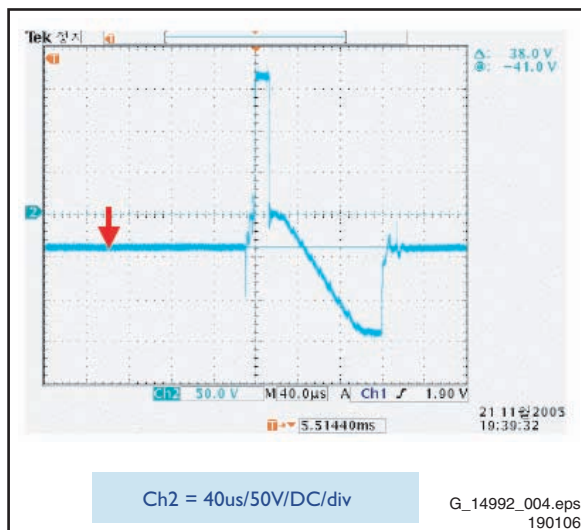


Figure 8-4 Y-scan H waveform (Y-Board)

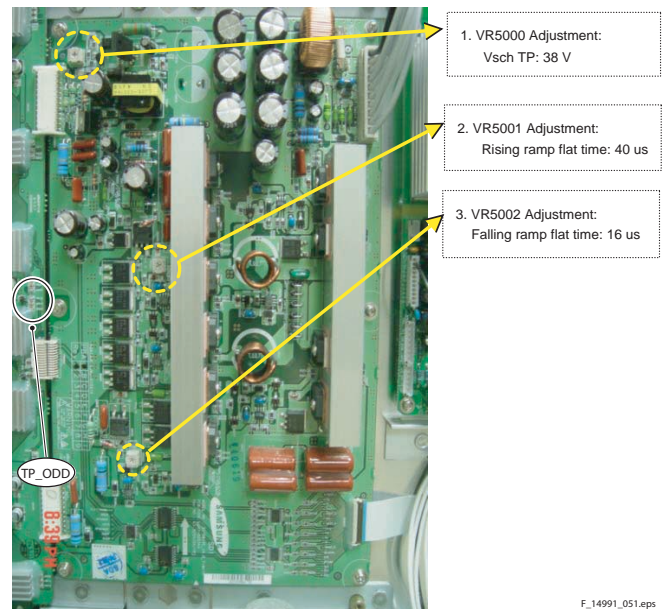


Figure 8-6 Potentiometer locations LJ92-01149A

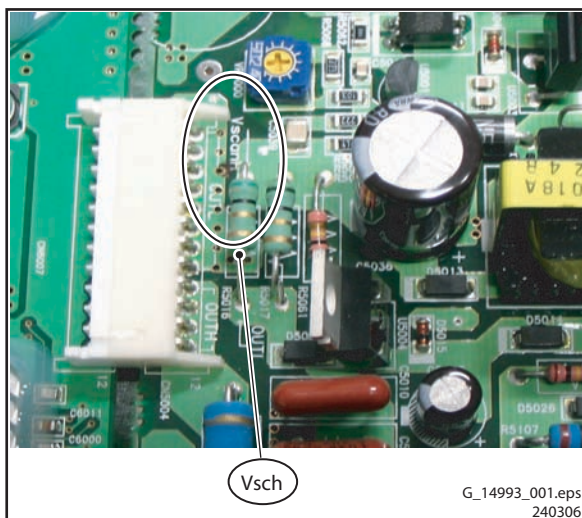


Figure 8-5 Test point location LJ92-01021A

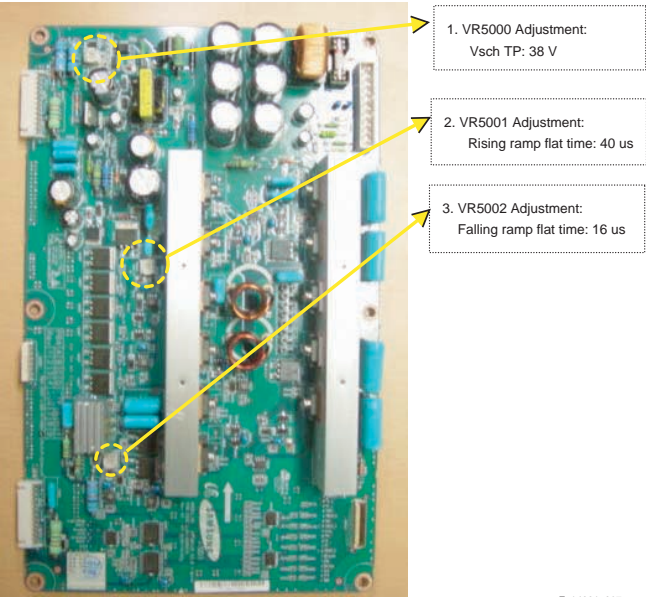


Figure 8-7 Potentiometer locations LJ92-01149B

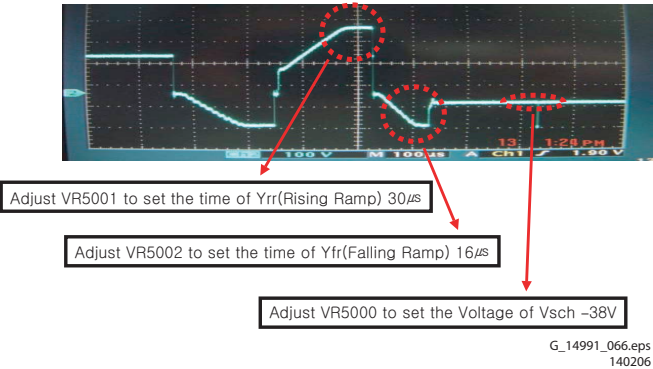
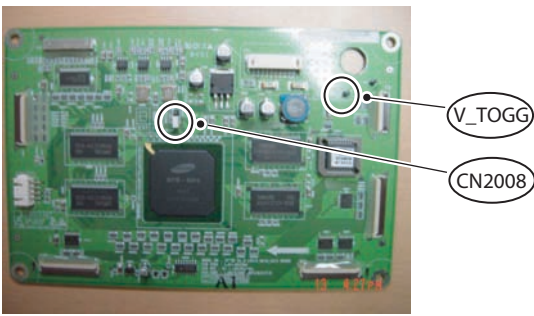
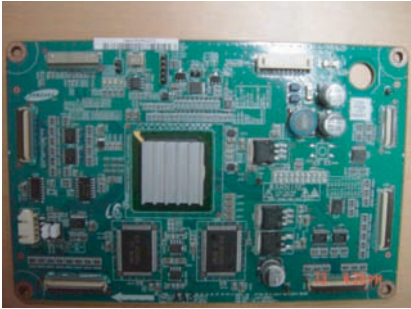


Figure 8-8 Wave form adjustment (Y-Main board)



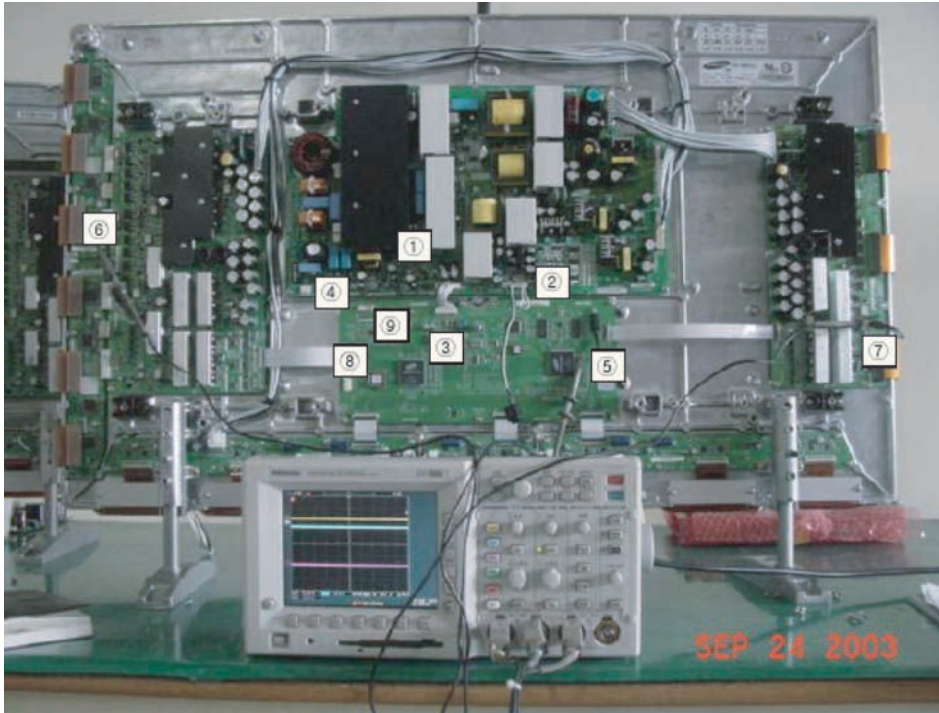
LJ92-01056A / LJ92-01145A



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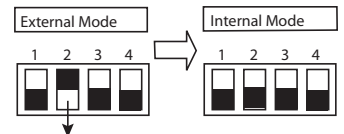
Figure 8-9 Logic PWB

8.2 Alignments 42" SD v2



1) Preparation

- 1 Insert jumper J8002 on PSU board
- 2 Connect the Jig connector switch
- 3 Put the Logic board dipswitches into internal mode, to generate a Full White screen



- 4 Connect the AC power jig

Connect the Oscilloscope:

- 5 CH1: V-SYNC (CN201)
- 6 CH2: Y-output (OUT4)
- 7 CH3: X-output (TP OUT)
- 8 Connect the Key-scan Board

2) Turn-On.

- Turn on the Power switch
- Check the LED on the Logic Board
- Check waveform of X- and Y-board (Refer to Picture below)

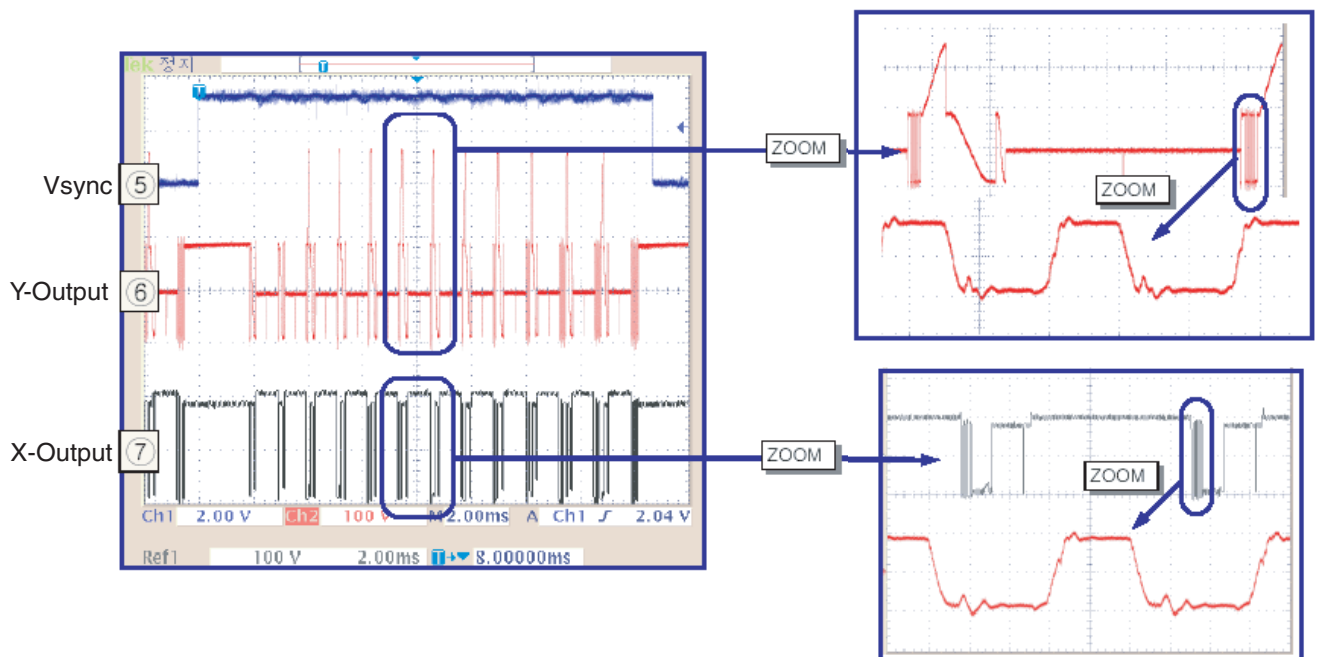


Figure 8-11 Waveform of X- and Y-board (42" SD v2)

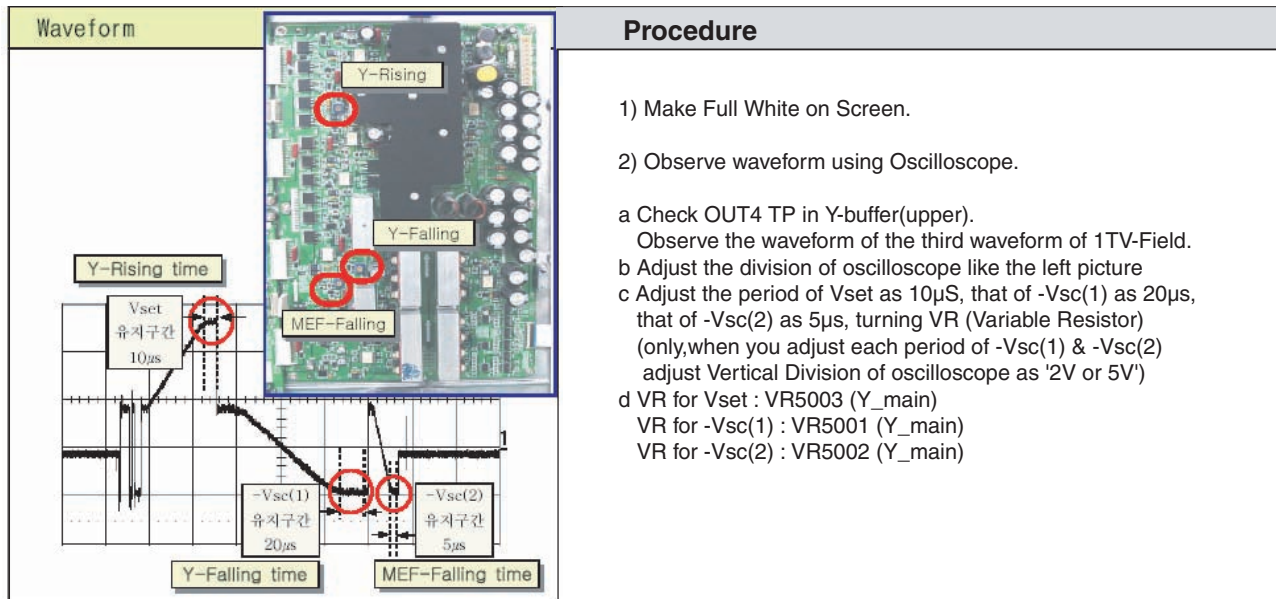


Figure 8-12 How to adjust the waveform (42" SD v2)

8.3 Alignments 42" SD v3

1. Put the dipswitches on the Logic Board in the internal position to get a Full White Pattern.
2. You can find the location of the test point and potentiometers in Figure "Potentiometer locations".
3. Adjust V_{sch} to 40 V with VR5004.
4. Check the waveform with an Oscilloscope.
 - Take the trigger signal from the testpoint marked "V-sync" on the Logic Board.
 - Connect the testpoint marked "OUT 4", located in the centre of Y_buffer Board to the other channel, and then check the first Subfield operating waveform of one TV-Field.
 - Check the waveform again after adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
 - Set the V_{set} to $10\mu s$ by adjusting VR5002.
 - Set the Falling maintenance time to $30\mu s$ by adjusting VR5003.
 - Change the waveform position of Oscilloscope to the 3rd Subfield and then set the Falling maintenance time to $30\mu s$ by adjusting the VR5001. GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.

Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the

Reset waveform and then move to the 3rd Sub-field for adjusting.

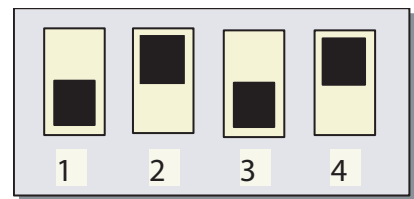


Figure 8-13 DIP switch mode: External

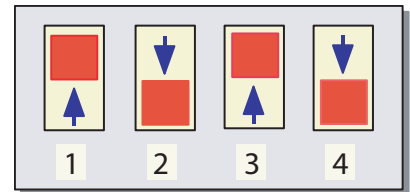


Figure 8-14 DIP switch mode: Internal

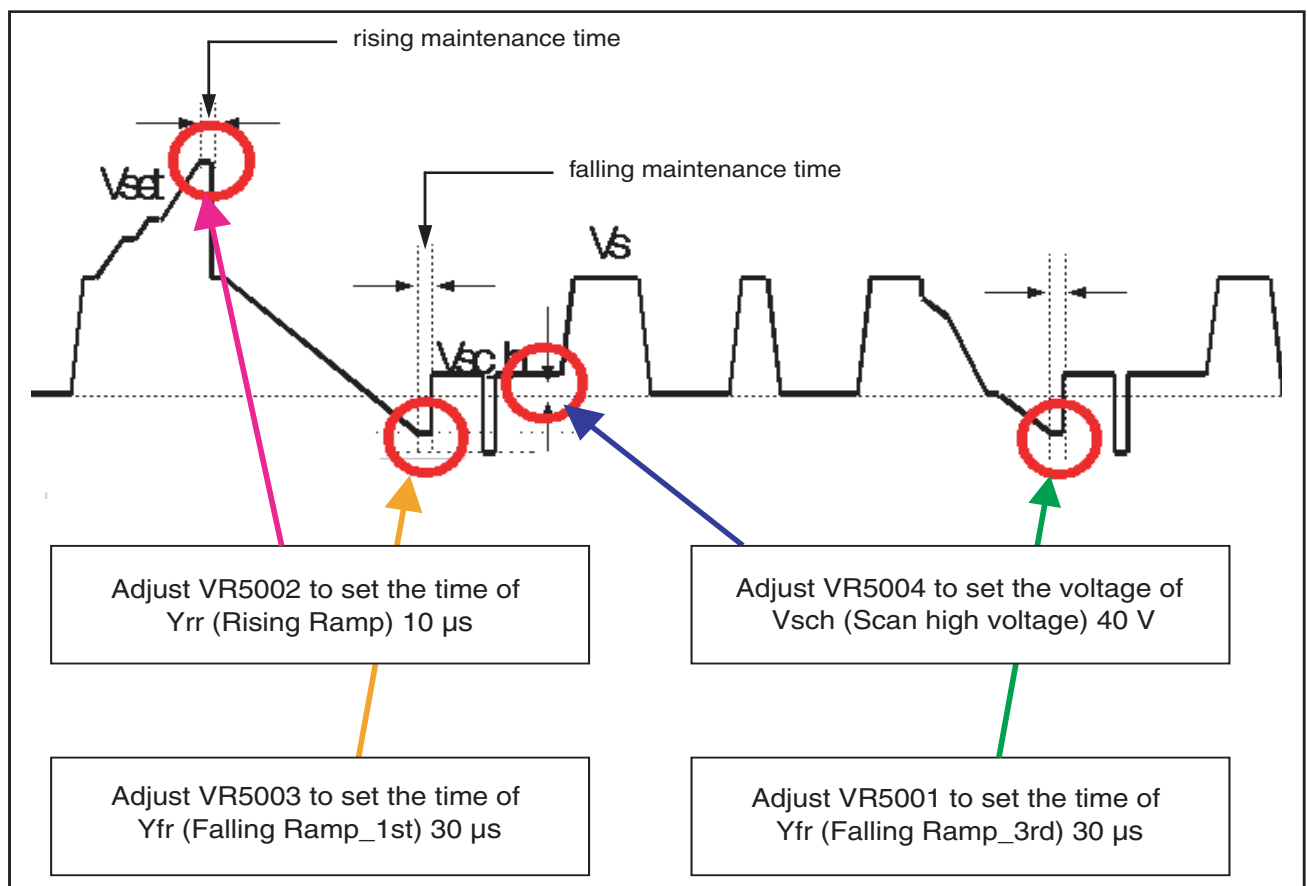


Figure 8-15 TCP ramp waveform inclination adjustment (Y-Board)

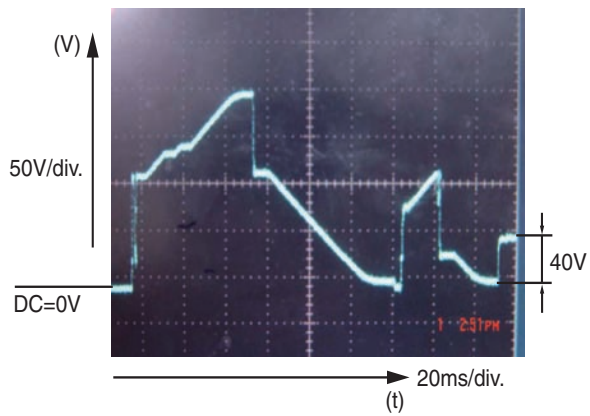


Figure 8-16 Rising ramp

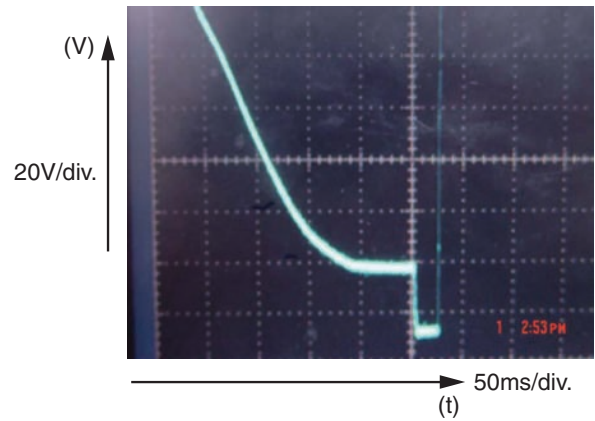


Figure 8-17 Falling ramp

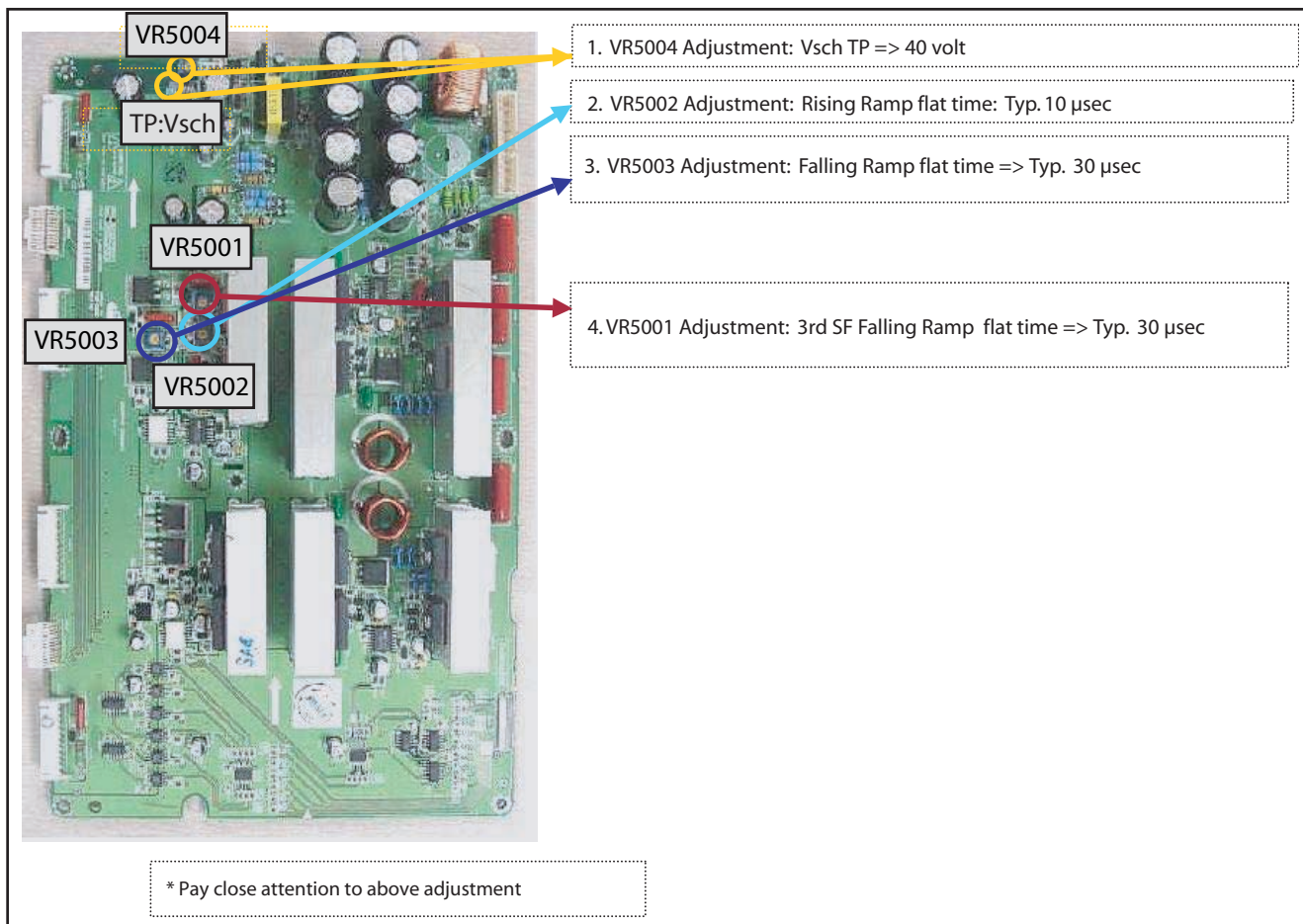
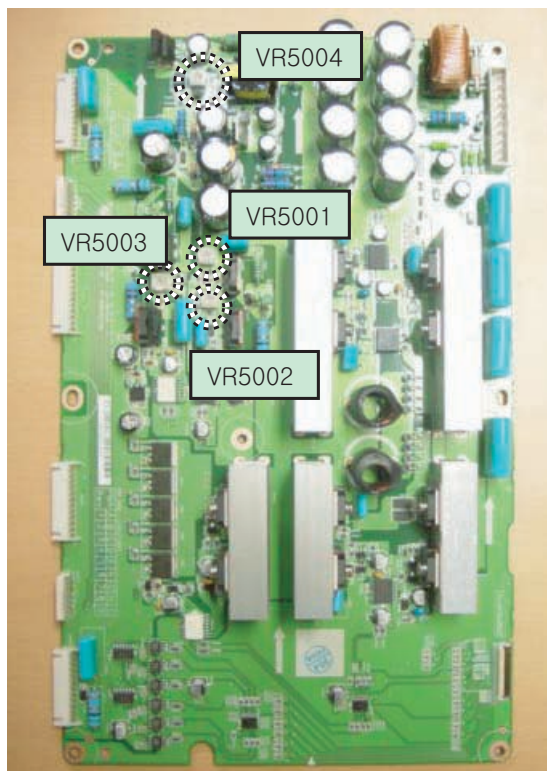
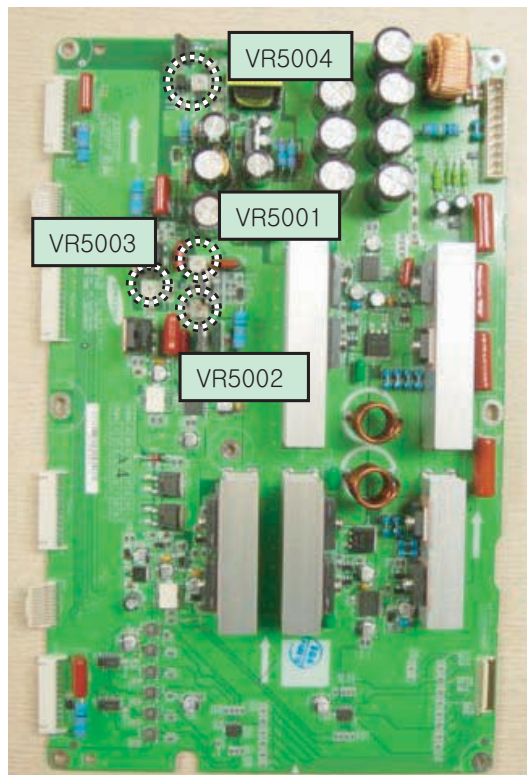


Figure 8-18 Potentiometer locations



LJ92-01284A

F_14991_070.eps
140206**Figure 8-19 Potentiometer locations LJ92-01284A**

LJ92-00944B

F_14991_069.eps
140206**Figure 8-20 Potentiometer locations LJ92-00944B**

8.4 Alignments 42" HD v3

1. Put the dipswitches on the Logic Board in the internal position to get a Full White Pattern.
2. Adjust V_{sch} to Clock-wise max by using VR5004 (V_{sch} should be connected to "+" unit of DMM).
3. Check the waveform using Oscilloscope.
 - Triggering through V_{TOGG} of LOGIC Board.
 - Connect the OUT 4 Test Point at the centre of Y_{buffer} to other channel, and then check the first Subfield operating waveform of one TV-Field.
 - Check the waveform again after adjusting Horizontal Division. Check the Reset waveform when the V_{TOGG} Level is changed.
 - Set the V_{set} to 20 μs by adjusting VR5002. GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.
 - Set the Falling maintenance time to 20 μs by adjusting VR5006.
 - Change the waveform position of Oscilloscope to the 3rd Subfield and then set the Falling maintenance time to 10 μs by adjusting the VR5003. GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.

Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the

Reset waveform and then move to the 3rd Sub-field for adjusting.

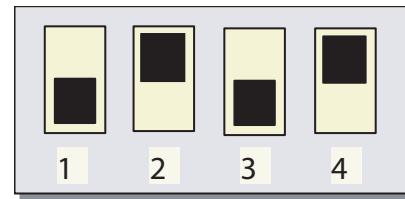


Figure 8-21 DIP switch mode: External

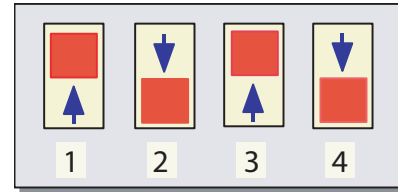


Figure 8-22 DIP switch mode: Internal

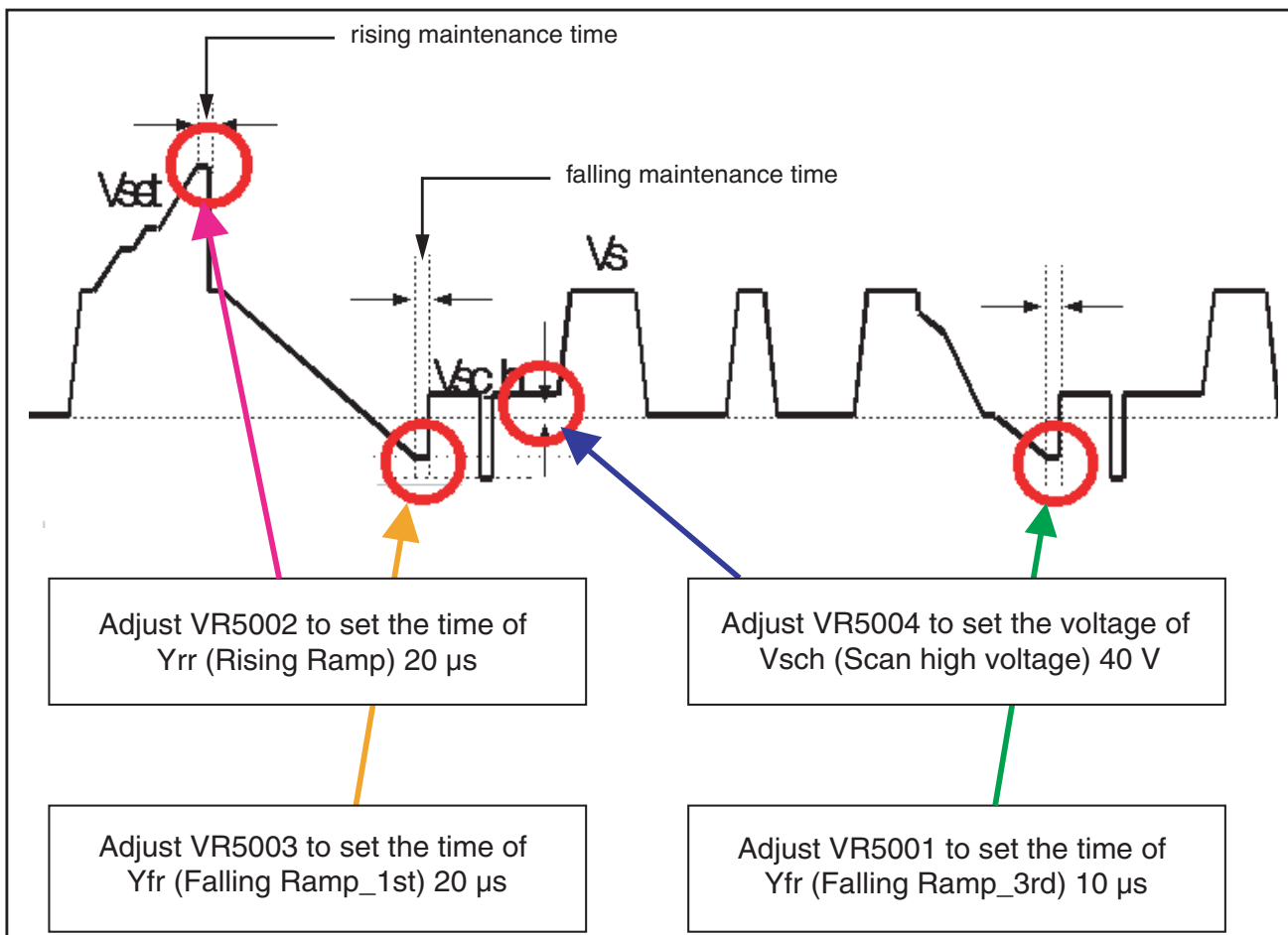


Figure 8-23 TCP ramp waveform inclination adjustment (Y-Board)

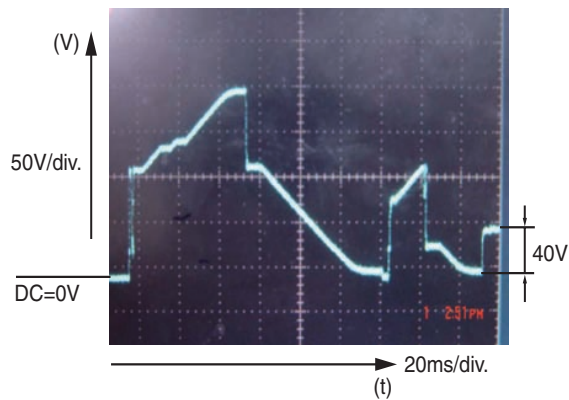


Figure 8-24 Rising ramp

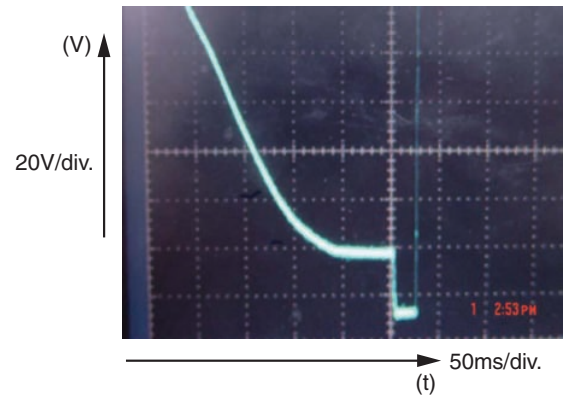


Figure 8-25 Falling ramp

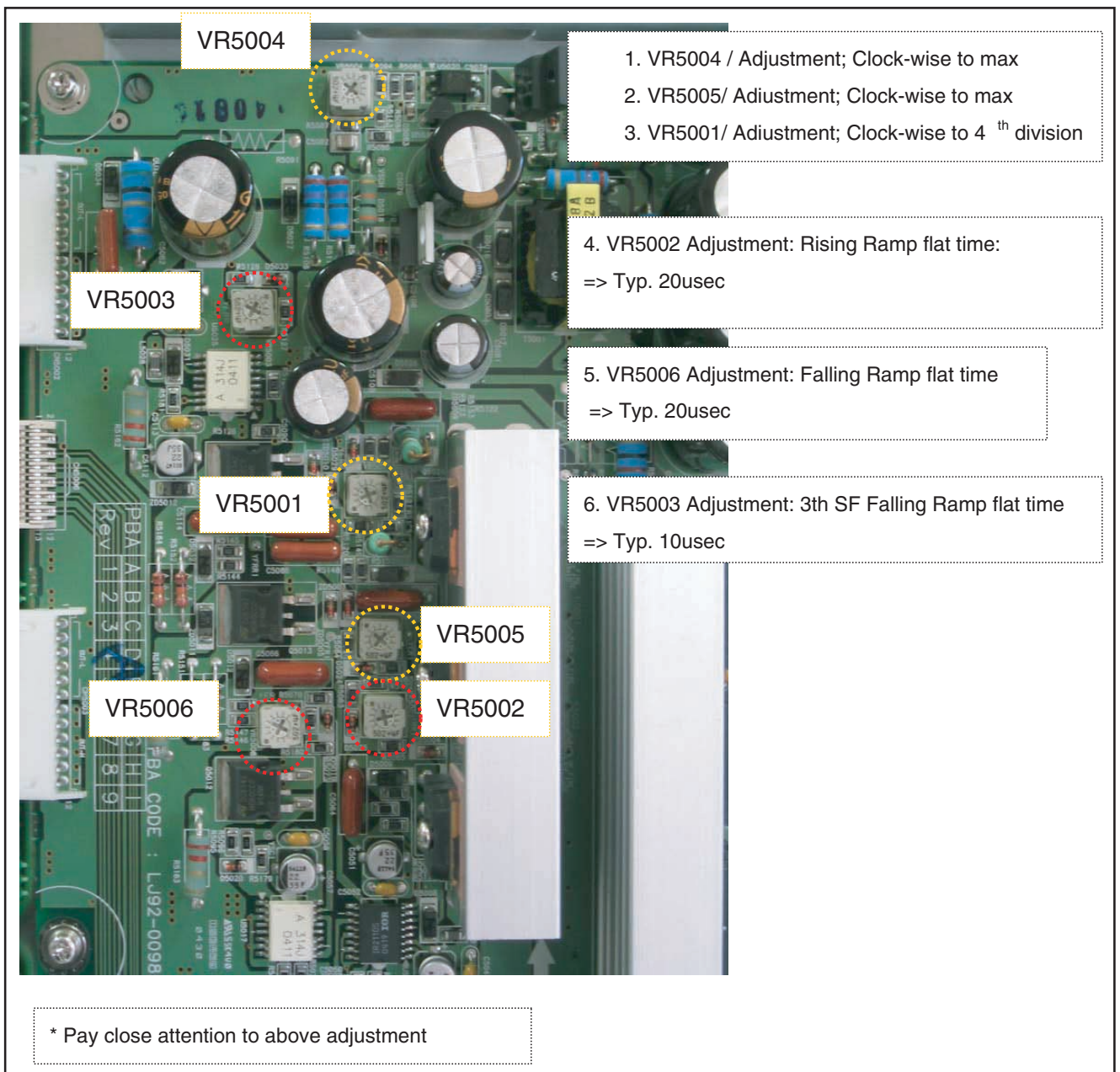
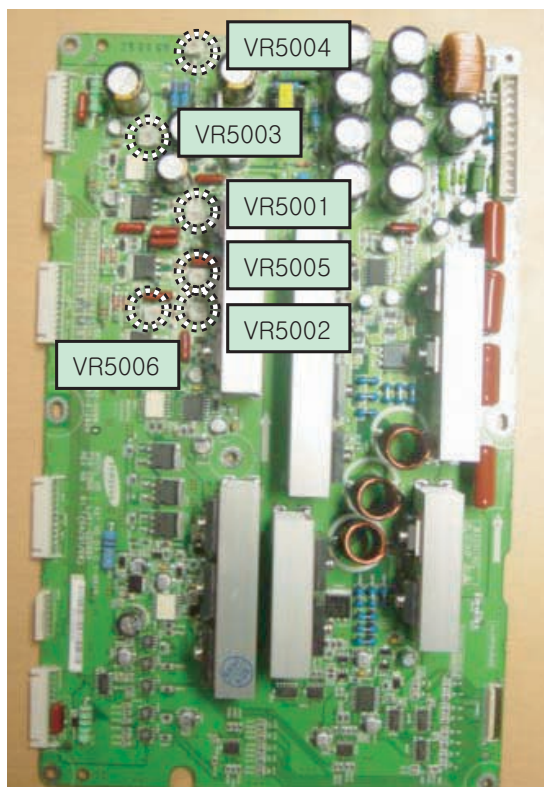
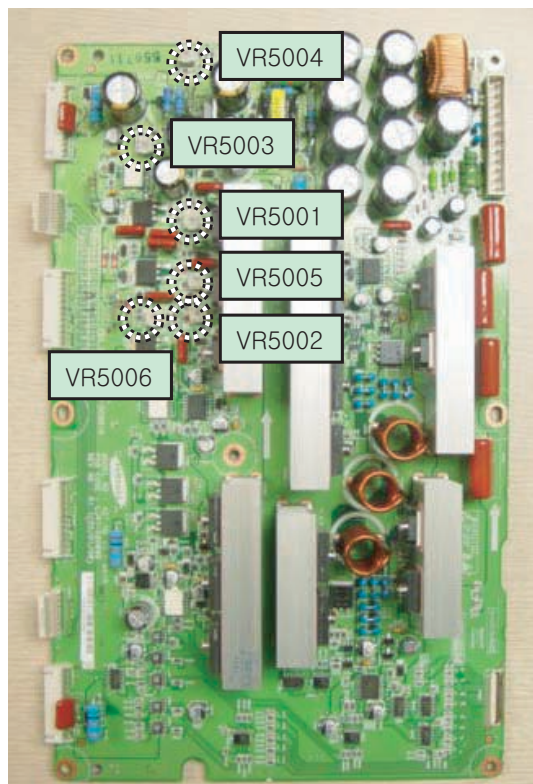


Figure 8-26 Potentiometer locations



LJ92-00981A

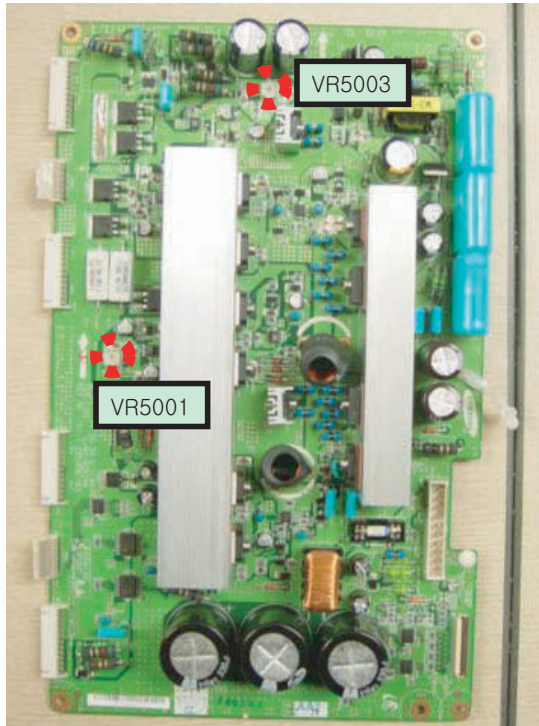
F_14991_071.eps
140206**Figure 8-27 Potentiometer locations LJ92-00981A**

LJ92-00981B

F_14991_072.eps
140206**Figure 8-28 Potentiometer locations LJ92-00981B**

8.5 Alignments 42" SD v4

1. Get Pattern to be Full White (place jumper CN2034 on Logic Board).
2. Check the waveform using an Oscilloscope.
 - Triggering through V_TOGG of LOGIC Board.
 - Connect the OUT 240 Test Point at the centre of Y_buffer to other channel, and then check the first aid-reset waveform from the last sustain of 1TV-Field.



LJ92-01337A

Figure 8-29 Potentiometer locations

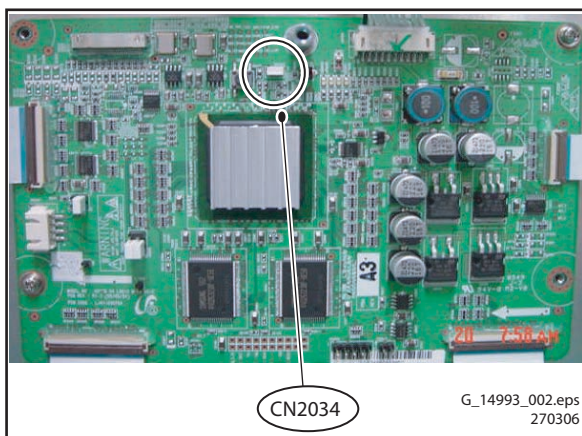


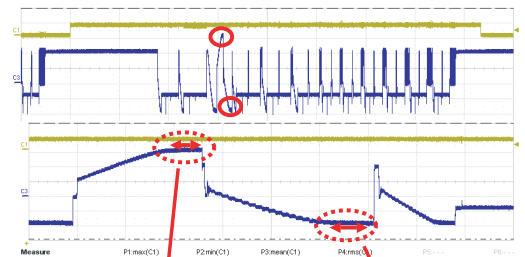
Figure 8-30 Jumper location (Logic board)

- Check the waveform again after adjusting Horizontal Division.
Check the Reset waveform when the V_TOGG Level is changed.
- Adjust the flat time of the rising ramp to 60μs with VR5001.
- Adjust the flat time of the falling ramp to 80μs with VR5003.

1.VR5001 Adjustment : Rising Ramp flat time :
→ 60 μs

2.VR5003 Adjustment : Falling Ramp flat time :
→ 80 μs

F_14991_074.eps
140206



Adjust VR5001 to set the time of Yrr(Rising Ramp) 60μs

Adjust VR5003 to set the time of Yfr(Falling Ramp) 80μs

F_14991_073.eps
140206

Figure 8-31 Wave form adjustment (Y-Main board)

8.6 Alignments 42" HD v4

1. Get Pattern to be Full White (place jumper CN2072 on Logic Board).
 2. Check the waveform using an Oscilloscope.
 - Triggering through V_TOGG of LOGIC Board.
 - Connect the OUT 240 Test Point at the centre of Y_buffer to other channel, and then check the first aid-reset waveform from the last sustain of one TV-Field.
 - Check the waveform again after adjusting Horizontal Division.
- Check the Reset waveform when the V_TOGG Level is changed.
- Set the 15V by adjusting VR5002.
 - Set the 100V and 50us by adjusting VR5001

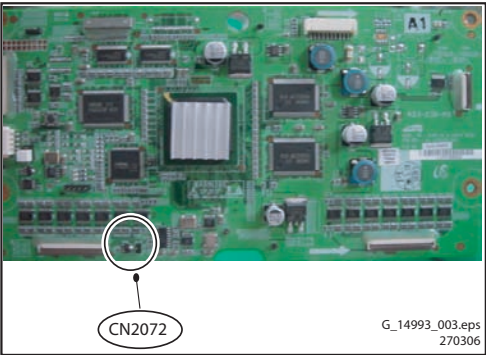


Figure 8-32 Jumper location (Logic board)

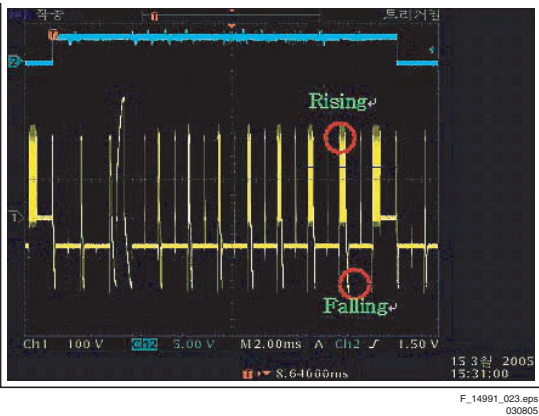


Figure 8-33 1st subfield from the last sustain within 1 frame

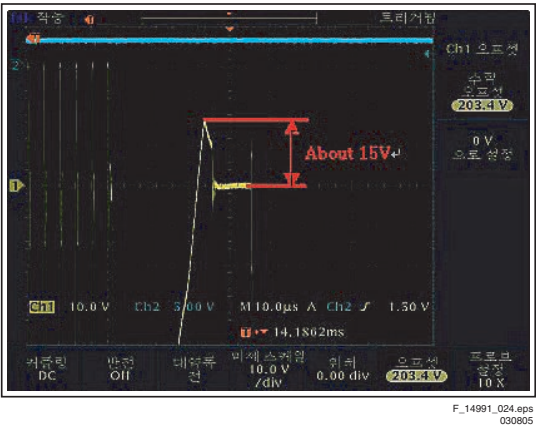


Figure 8-34 Rising ramp of aid-reset

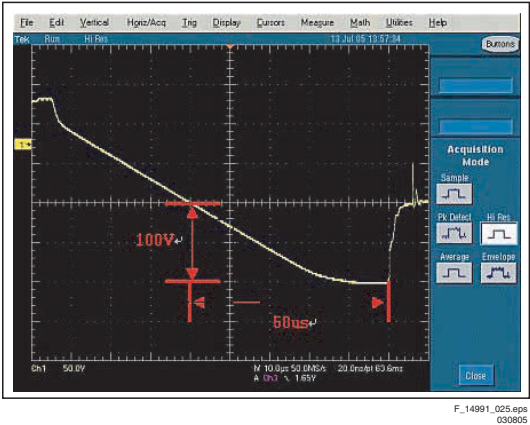


Figure 8-35 Falling ramp of aid-reset

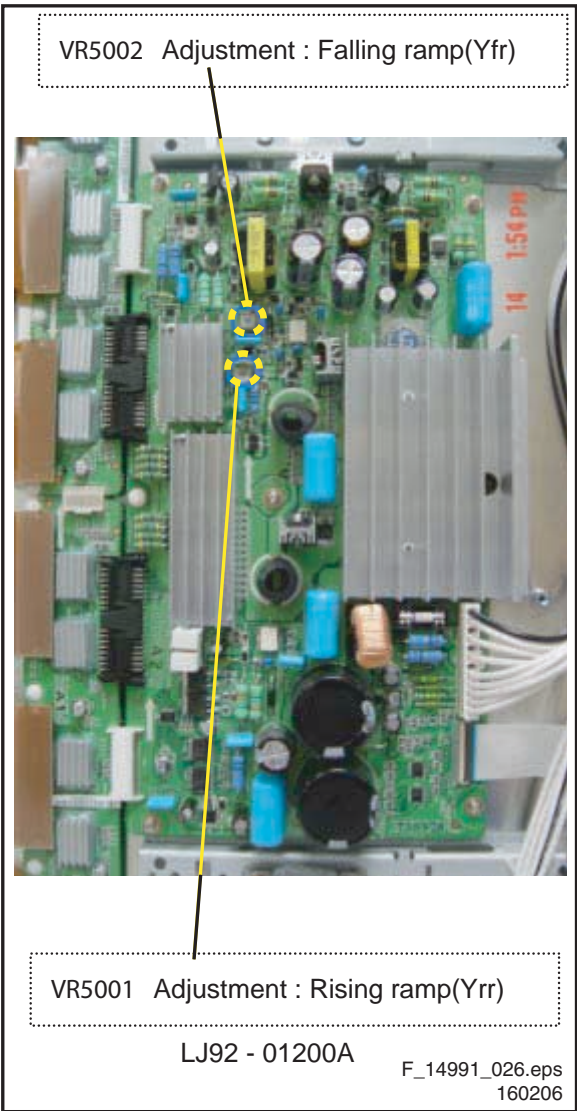


Figure 8-36 Potentiometer locations

8.7 Alignments 50" HD v3

1. Put the dipswitches on the Logic Board in the internal position to get a Full White Pattern (see Figure "DIP switch positions").
2. Adjust Vsch to 25 V by using VR5901_VSC_h (Vsc_h should be connected to "+" unit of DMM).
3. Check the waveform using Oscilloscope.
 - Triggering through V_TOGG of LOGIC Board.
 - Connect the OUT 4 Test Point at the centre of Y_buffer to other channel, and then check the first Subfield operating waveform of one TV-Field.
 - Check the waveform again after adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
 - Set the Rising Ramp Flat Time to 50 μ s by adjusting VR5000. GND maintenance section should be

checked after the Vertical Division is readjusted to '2 V or 5 V'.

- Set the Falling maintenance time to 35 μ s by adjusting VR5001.
- Change the waveform position of Oscilloscope to the 3rd Subfield and then set the Falling maintenance time to 20 μ s by adjusting the VR5002.
- GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.

Special notice: When you adjust the inclination of waveform, do check and adjustment being based on the Reset waveform of 1st Sub-field of 1st Frame and then move to 3rd Sub-field for adjusting.

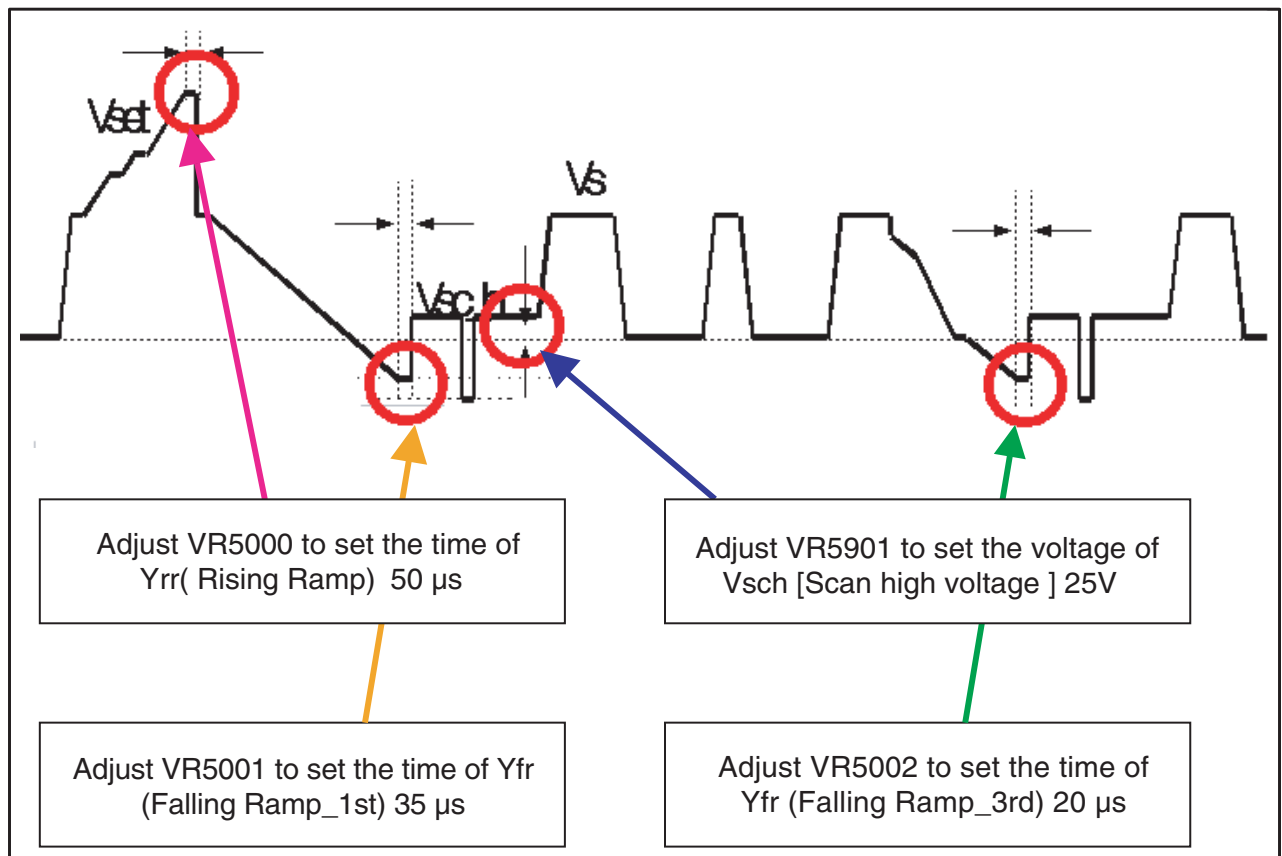


Figure 8-37 TCP ramp waveform inclination adjustment (Y-Board)

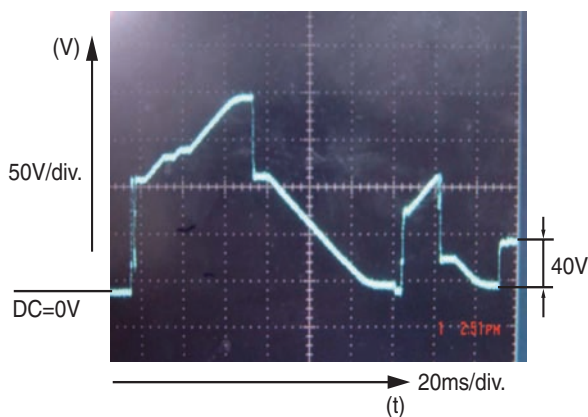


Figure 8-38 Rising ramp

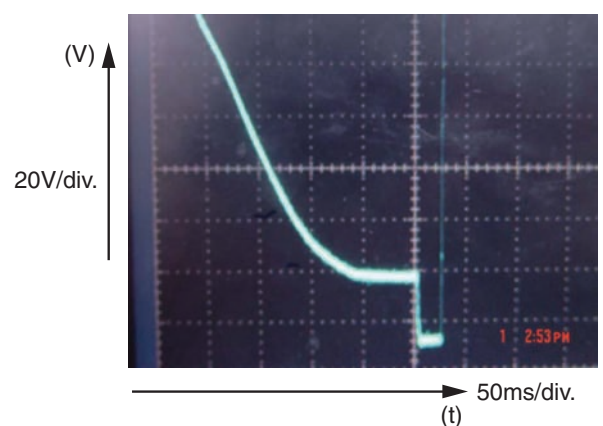


Figure 8-39 Falling ramp

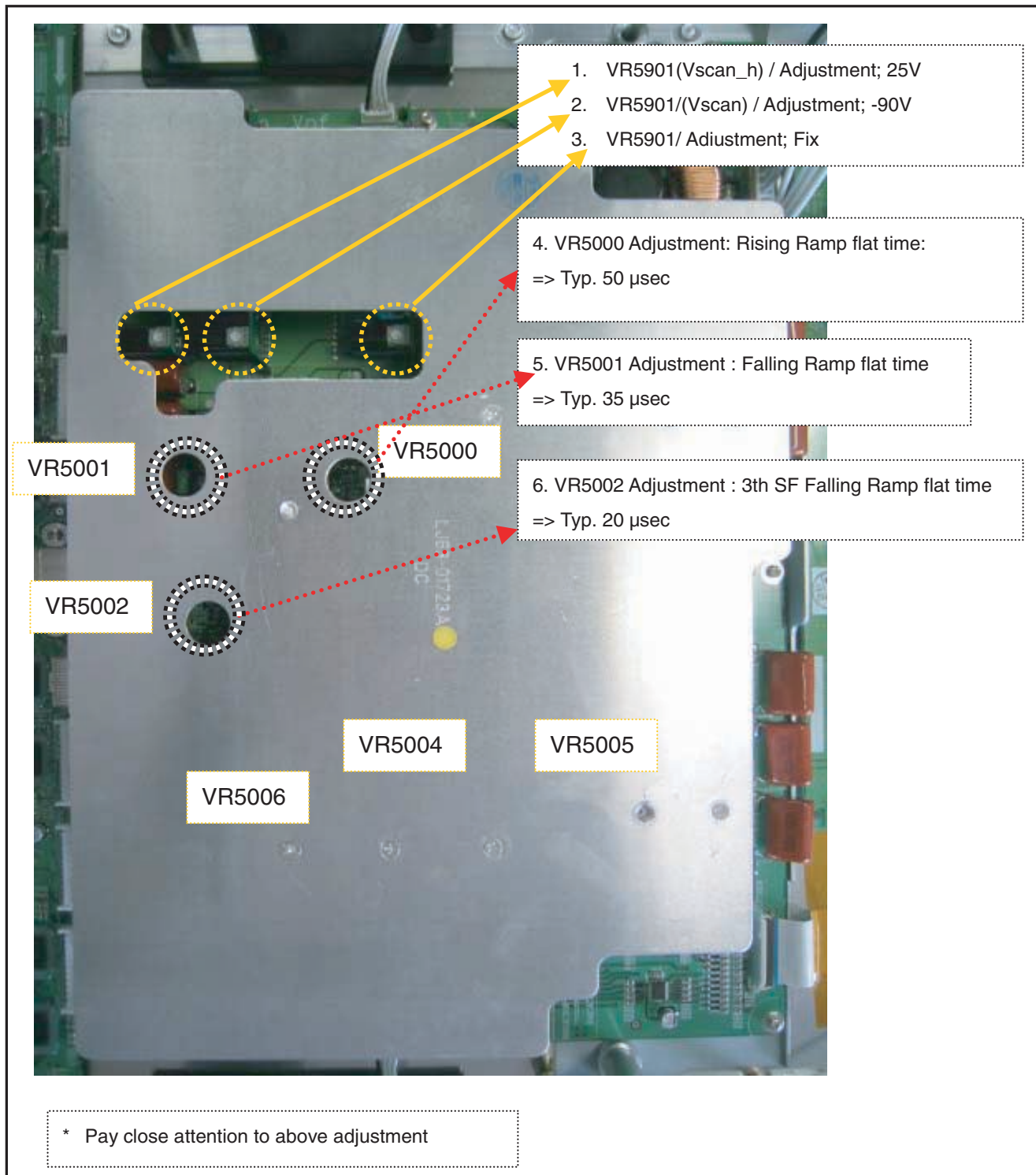
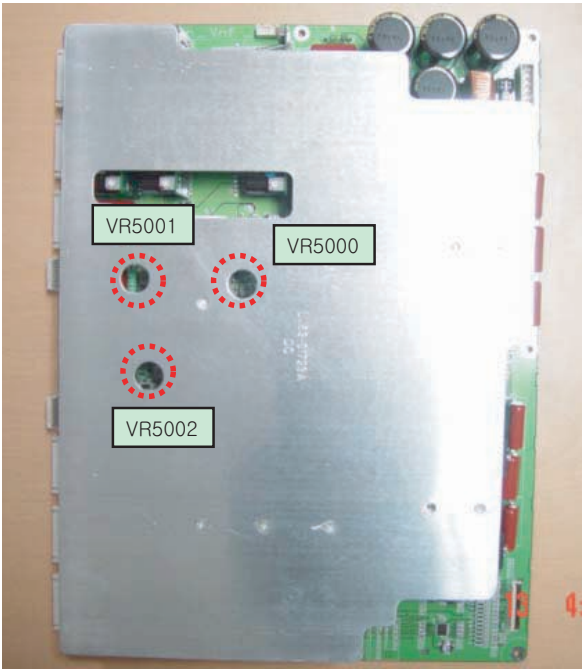
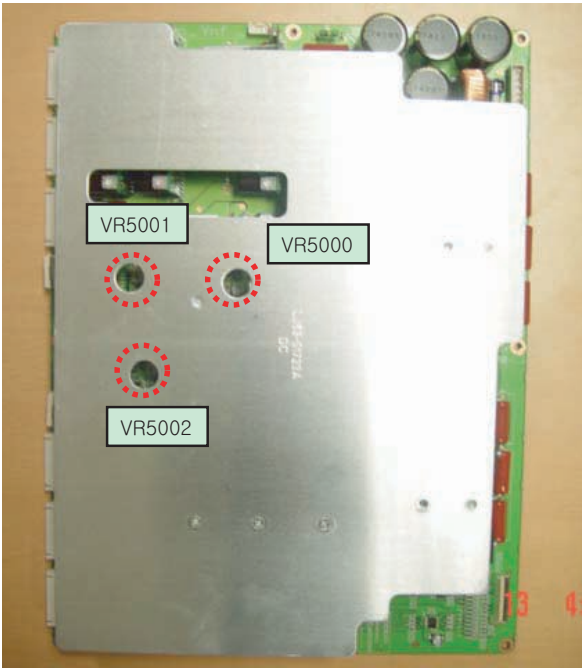


Figure 8-40 Potentiometer locations



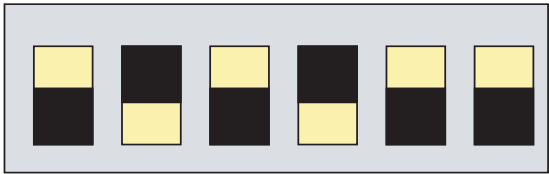
LJ92-00853A F_14991_076.eps
140206

Figure 8-41 Potentiometer locations LJ92-00853A

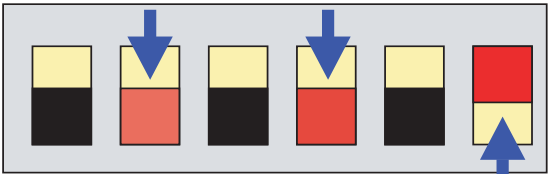


LJ92-00853B F_14991_077.eps
140206

Figure 8-42 Potentiometer locations LJ92-00853B



< External >



< Internal >

F_14991_050.eps
230306

Figure 8-43 DIP switch positions

Figure 8-45 TCP ramp waveform inclination adjustment (Y-Board)

F_14991_021a.eps
030805

Figure 8-46 Rising ramp

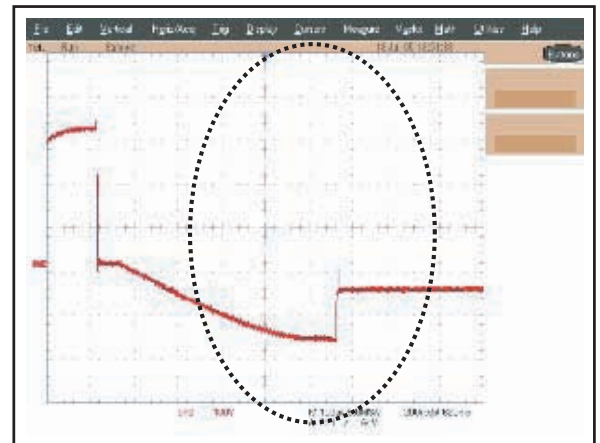
F_14991_021b.eps
030805

Figure 8-47 Falling ramp

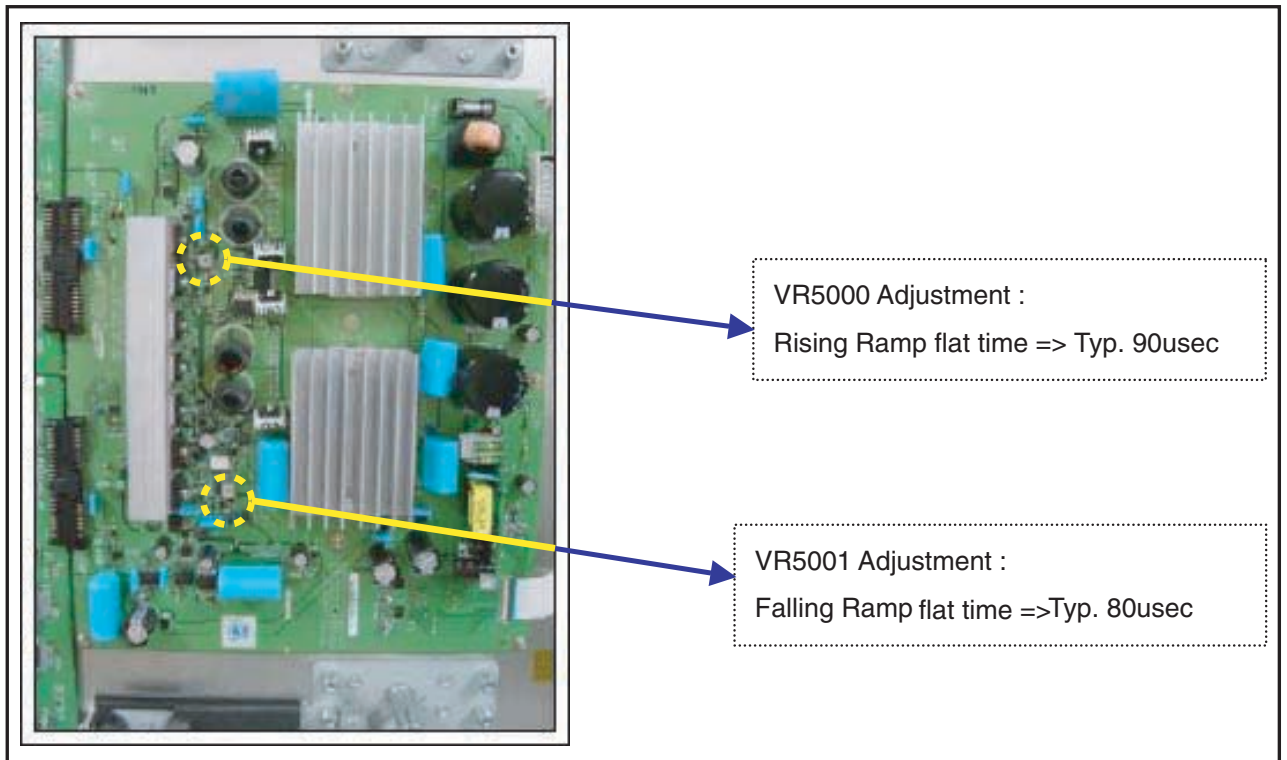
F_14991_022.eps
030805

Figure 8-48 Potentiometer locations

8.9 Alignment value overview (all screens)

Table 8-1 Alignment table Y PWB

Model	Wave Form	Item	Default
37"SD v4	Rising_Ramp	VR5001	30 μ s (30 ~ 40)
	Falling_Ramp_1st	VR5002	16 μ s (10 ~ 20)
	Vsch	VR5000	38 V
42" SD v2	Rising_Ramp (Vset)	VR5003	10 μ s
	-Vsc 1	VR5001	20 μ s
	-Vsc 2	VR5002	5 μ s
42" SD v3	Rising_Ramp	VR5002	10 μ s
	Falling_Ramp_1st	VR5003	30 μ s
	Falling_Ramp_3rd	VR5001	30 μ s
	Vsch	VR5004	40 V
42" SD v4	Rising_Ramp	VR5001	60 μ s
	Falling_Ramp_1st	VR5003	80 μ s
42" HD v3	Rising_Ramp	VR5002	10 μ s
	Falling_Ramp_1st	VR5003	20 μ s
	Falling_Ramp_3rd	VR5001	10 μ s
	Vsch Scan high voltage	VR5004	40 V
42" HD v4	Rising_Ramp	VR5001	15 V
	Falling_Ramp_1st	VR5002	50 μ s
50" HD v3	Rising_Ramp	VR5000	50 μ s
	Falling_Ramp_1st	VR5001	35 μ s
	Falling_Ramp_3rd	VR5002	20 μ s
	Vsch Scan high voltage	VR5901	25 V
50" HD v4	Rising_Ramp	VR5001	90 μ s
	Falling_Ramp_1st	VR5003	80 μ s

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

- 9.1 Main function of Each Assembly
- 9.2 Abbreviation List
- 9.3 IC Data Sheets

9.1 Main function of Each Assembly

9.1.1 X Main Board

The X Main board generates a drive signal by switching the FET in synchronization with logic main board timing, and supplies the X electrode of the panel with the drive signal through the connector.

1. Maintain voltage waveforms (including ERC).
2. Generate X rising ramp signal.
3. Maintain Ve bias between Scan intervals.

9.1.2 Y Main Board

The Y Main board generates a drive signal by switching the FET in synchronization with the logic Main Board timing and sequential supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

1. Maintain voltage waveforms (including ERC).
2. Generate Y-rising Falling Ramp.
3. Maintain V scan bias.

9.1.3 Logic Main Board

The Logic Main board generates and outputs the address drive output signal and the X,Y drive signal by processing the video signals. This Board buffers the address drive output signal and feeds it to the address drive IC (COF module, video signal- X Y drive signal generation, frame memory circuit / address data rearrangement).

9.1.4 Logic Buffer (E, F)

The Logic Buffer transmits data signal and control signal.

9.1.5 Y Buffer Board (Upper, Lower)

The Y Buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises eight scan driver ICs (ST microelectronics STV 7617: 64 or 65 output pins), but four ICs for the SD class.

9.1.6 AC Noise Filter

The AC Noise filter has function for removing noise (low frequency) and blocking surge. It affects safety standards (EMC, EMI).

9.1.7 TCP (Tape Carrier Package)

The TCP applies the Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise four data driver ICs (STV7610A: 96 pins output pins). Seven TCPs are required for signal scan.

9.2 Abbreviation List

AC	Alternating Current
COF	Circuit On Foil
DC	Direct Current
ERC	Energy Recovery Circuit
ESD	Electro Static Discharge
FET	Field Effect Transistor
FFC	Flat Foil Cable
FPC	Flexible Printed Circuit
FTV	Flat TeleVision
HD	High Definition
I/O	Input/Output
IC	Integrated Circuit
LB	Logic Buffer
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signalling
PCB	Printed Circuit Board (same as PWB)
PDP	Plasma Display Panel
PSU	Power Supply Unit
PWB	Printed Wiring Board (same as PCB)
RGB	Red, Green, Blue colour space
SD	Standard Definition
SDI	Samsung Display Industry (supplier)
SMPS	Switched Mode Power Supply
SSB	Small Signal Board
SF	Sub Field
TCP	Tape Carrier Package
VR	Variable Resistor
Vsc	Scan Voltage
YBL	Y Buffer Lower board
YBU	Y Buffer Upper board
YM	Y Main board

9.3 IC Data Sheets

Not applicable.

10. Spare Parts List

Notes;

- Determine the SDI part / model number of the PDP
- Find the SDI part number on the actual board to be replaced.
SDI part number begin with "LJ92" and for the SMPS and sub SMPS the part number will begin with "LJ44".
- Find the SDI board part number in the spare parts overview.
- Find the SDI part number in this overview that matches the part number that is actually on the original board.
- Cross the SDI board part number to the philips part number.
- Order the philips part number.

- Note:** The appearance of a leaded and lead-free board can be different; the colour of the PWB and also the layout of the components are sometimes different.



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081105

Figure 10-1 Lead-free logo SDI

Table 10-1 Spare parts overview 37" SD v4

PDP type	37" SD v4				Lead Free type being compatible with Lead type PWB
PDP 12NC	9322 217 39682 (8204 000 77261)				
PDP model type and version	S37SD-YD02				
Remarks	Lead type boards being not compatible with lead free type will not be phased out				
Boards	Codes for lead type PWB's		Codes for lead-free type PWB's		
Logic-Buffer (E)	LJ92-00976A	9965 000 26187	LJ92-01138B	9965 000 32616	N
Logic-Buffer (F)	LJ92-00977A	9965 000 26188	LJ92-01139B	9965 000 32617	N
Logic-Buffer (G)	LJ92-01002A	9965 000 26189	LJ92-01140B	9965 000 32618	N
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01022A	9965 000 26190	LJ92-01147A	9965 000 32619	N
Y-Buffer (down)	-	-	-	-	-
Logic-Board	LJ92-01056A (See Kit 1 Note) LJ92-01145A (See Kit 2 Note)	9965 000 26191	LJ92-01257A	9965 000 29322	N
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-01020A	9965 000 26192	LJ92-01268A	9965 000 32620	N
Y-Board	LJ92-01021A	9965 000 26193	LJ92-01149B	9965 000 32621	N
SMPS (PSU)	LJ44-00084A	9965 000 26194	LJ44-00084B	9965 000 32622	Y
SUB PSU	LJ44-00075A	9965 000 25131	LJ44-00075B	9965 000 32623	Y
		Kit 1	LJ93-00205A	9965 000 33796	
		Kit 2	LJ93-00204A	9965 000 33797	

Note:

Kit 1: 37" FCR kit consists of 4 boards (Logic + Y-main + Y and E buffer)

reference Symptom Cure information TV-05/0006

CORRECTION XI: PDP with "Lead" boards and use of Logic board (LJ92-01056A):

Replace the Logic board, the Y-Main board, the Y-buffer board, and the Logic buffer E board together.

These four boards are available in Service Kit number 1 (with order code 9965 000 33796 (LJ93-00205A)).

The content of Service Kit number 1 is:

- * Logic main board 9965 000 29322 (LJ92-01257A).
- * Y-Main board 9965 000 32621 (LJ92-01149B).
- * Y-Buffer board 9965 000 32619 (LJ92-01147A).
- * Logic-Buffer E 9965 000 32616 (LJ92-01138B).

Note:

FCR Kit: = False contouring reduction kit

Note:

Kit 2: 37" FCR kit consists of 2 boards (logic + Y-main)

reference Symptom Cure information TV-05/0006

CORRECTION XI

PDP with "Lead-free" boards and use of Logic board (LJ92-01145A):

Replace the Logic board and the Y-Main board together. These two boards are available in Service Kit number 2 (with order code 9965 000 33797 (LJ93-00204A)).

The content of Service Kit number 2 is:

- * Logic main board 9965 000 29322 (LJ92-01257A).
- * Y-Main board 9965 000 32621 (LJ92-01149B).

3) PDP with "Lead-free" boards and use of Logic board (LJ92-01257A):

In case this PDP has a defective board, replace this defective board only

Table 10-2 Spare parts overview 42" SD v2

PDP type	42"SDv2	
PDP model 12NC	9322 195 45682	
PDP model type and version	S42SD-YD06	
Remarks	Codes for lead type PWBs (this model has been produced with leaded type PWB's only)	
Boards	PWB Codes	
Logic-Buffer (E)	LJ92-00632A	9965 000 17726
Logic-Buffer (F)	LJ92-00633A	9965 000 17725
Logic-Buffer (G)	LJ92-00634A	9965 000 17724
Logic-Buffer (H)	-	-
Logic-Buffer (I)	-	-
Logic-Buffer (J)	-	-
Y-Buffer (up)	LJ92-00751A	9965 000 17727
Y-Buffer (down)	LJ92-00750A	9965 000 17728
Logic-Board	LJ92-00818A	9965 000 17729
SUBL	-	-
SUBR	-	-
X-Board	LJ92-00998A	9965 000 17720
Y-Board	LJ92-00999A	9965 000 17731
SMPS (PSU)	LJ44-00049A	9965 000 17730
SUB PSU	-	-

Table 10-3 Spare parts overview 42" SD v3

PDP type	42" SD v3				Lead Free type being compatible with Lead type PWB
PDP model 12NC	9322 215 27682				
PDP model type and version	S42SD-YD05				
Remarks	Lead type boards being phased out				
Boards	Codes for leaded type PWBs		Codes for lead-free type PWBs		
Logic-Buffer (E)	LJ92-00811A	9965 000 25109	LJ92-00811B	9965 000 32624	Y
Logic-Buffer (F)	LJ92-00812A	9965 000 25110	LJ92-00812B	9965 000 32625	Y
Logic-Buffer (G)	LJ92-00813A	9965 000 25111	LJ92-00813B	9965 000 32626	Y
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-00796A	9965 000 25112	LJ92-01285A	9965 000 32376	Y
Y-Buffer (down)	LJ92-00797A	9965 000 25113	LJ92-01286A	9965 000 32377	Y
Logic-Board	LJ92-00975D	9965 000 25114	LJ92-01247D	9965 000 32378	N (tbd)
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-00943A	9965 000 25115	LJ92-01283A	9965 000 32627	Y
Y-Board	LJ92-00944B	9965 000 25116	LJ92-01284A	9965 000 32379	Y
SMPS (PSU)	LJ44- 000 58A	9965 000 25108	LJ44-00058B	9965 000 32638	Y
SUB PSU	LJ44- 000 75A	9965 000 25131	LJ44-00075B	9965 000 32623	Y

Table 10-4 Spare parts overview 42" SD v4 (Part 1)

PDP type	42" SD v4				Boards from PP42SD015A and S42SD-YD07 (*) being compatible
PDP model 12NC	9322 226 37682				
PDP model type and version	S42SD-YD07 (*)		S42SD-YD07 (PP42SD015A)		
Remarks	No supply of new SMPS LJ44-00092B. Compatibility with LJ44-00101C + cable: tdb (15/2)		Version number used by SDI:PP42SD015B(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service information: tbd		
Logic-Buffer (E)	LJ92-01026A	9965 000 29205	LJ92-01026A	9965 000 29205	Y
Logic-Buffer (F)	LJ92-01027A	9965 000 29206	LJ92-01027A	9965 000 29206	Y
Logic-Buffer (G)	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01031A	9965 000 29207	LJ92-01031A	9965 000 29207	Y
Y-Buffer (down)	LJ92-01032A	9965 000 29208	LJ92-01032A	9965 000 29208	Y
Logic-Board	LJ92-01274D	9966 000 30042	LJ92-01274D	9966 000 30042	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-01029A	9965 000 29204	LJ92-01336A	9965 000 32628	Y
Y-Board	LJ92-01030A	9965 000 29209	LJ92-01337A	9965 000 32629	Y
SMPS (PSU)	LJ44-00092B	9965 000 29210	LJ44-00101A	9965 000 29210	N (tdb)
SUB PSU	-	-	-	-	-

Table 10-5 Spare parts overview 42" SD v4 (Part 2)

PDP type	42" SD v4					Service Information
PDP model 12NC	9322 226 96682			9322 233 81682		932223381682 being backwards compatible tbd
PDP model type and version	S42SD-YD07 (PP42SD015B)			S42SD-YD07 (PP42SD015F)		
Remarks	Version number used by SDI:PP42SD015B(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service information: tbd		PWB's from PP42SD015B and PP42SD015A being compatible	Version number used by SDI: PP42SD015F (SMPS Rev.0.7)		PWB's from PP42SD015B and PP42SD015F being compatible
Logic-Buffer (E)	LJ92-01026A	9965 000 29205	Y	LJ92-01026A	9965 000 29205	Y
Logic-Buffer (F)	LJ92-01027A	9965 000 29206	Y	LJ92-01027A	9965 000 29206	Y
Logic-Buffer (G)	-	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-	-
Y-Buffer (up)	LJ92-01031A	9965 000 29207	Y	LJ92-01031A	9965 000 29207	Y
Y-Buffer (down)	LJ92-01032A	9965 000 29208	Y	LJ92-01032A	9965 000 29208	Y
Logic-Board	LJ92-01274D	9966 000 30042	Y	LJ92-01274D	9966 000 30042	Y
SUBL	-	-	-	-	-	-
SUBR	-	-	-	-	-	-
X-Board	LJ92-01336A	9965 000 32628	Y	LJ92-01336A	9965 000 32628	Y
Y-Board	LJ92-01337A	9965 000 32629	Y	LJ92-01337A	9965 000 32629	Y
SMPS (PSU)	LJ44-00101B	9965 000 32630	N	LJ44-00101C	9965 000 33880	Y
SUB PSU	-	-	-	-	-	-

Table 10-6 Spare parts overview 42" HD v3

PDP type	42" HD v3				Lead Free type being compatible with Lead type PWB
PDP model 12NC	9322 215 25682				
PDP model type and version	S42AX-XD02				
Remarks	Lead type boards being phased out				
Boards	Codes for leaded type PWBs		Codes for lead-free type PWBs		
Logic-Buffer (E)	LJ92-00895A	9965 000 25101	LJ92-01264A	9965 000 32631	Y
Logic-Buffer (F)	LJ92-00896A	9965 000 25102	LJ92-01265A	9965 000 32632	Y
Logic-Buffer (G)	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-00993A	9965 000 25103	LJ92-00993B	9965 000 32633	Y
Y-Buffer (down)	LJ92-00994A	9965 000 25104	LJ92-00994B	9965 000 32634	Y
Logic-Board	LJ92-00990E	9965 000 25105	LJ92-01221C	9965 000 32635	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-00980A	9965 000 25106	LJ92-00980B	9965 000 32636	Y
Y-Board	LJ92-00981A	9965 000 25107	LJ92-00981B	9965 000 32637	Y
SMPS (PSU)	LJ44-00058A	9965 000 25108	LJ44-00058B	9965 000 32638	Y
SUB PSU	LJ44-00075A	9965 000 25131	LJ44-00075B	9965 000 32623	Y

Table 10-7 Spare parts overview 42" HD v4 (Part 1)

PDP type	42" HD v4				Boards from S42AX-YD01(*) and PP42AX- 007A being Compatible
PDP model 12NC	8204 000 78191		9322 225 38682		
PDP model type and version	S42AX-YD01 (*)		S42AX-YD01 (PP42AX-007A)		
Remarks	SMPS LJ44-00092A being phased out supply:LJ44-00101C + cables. Service information: tbd		(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service information: tbd		
Logic-Buffer (E)	LJ92-01054A	9965 000 29197	LJ92-01054A	9965 000 29197	Y
Logic-Buffer (F)	LJ92-01055A	9965 000 29198	LJ92-01055A	9965 000 29198	Y
Logic-Buffer (G)	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01117A	9965 000 29199	LJ92-01202A	9965 000 32639	Y
Y-Buffer (down)	LJ92-01118A	9965 000 29200	LJ92-01203A	9965 000 32640	Y
Logic-Board	LJ92-01053A	9965 000 29203	LJ92-01270B	9965 000 32641	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-01115A	9965 000 29196	LJ92-01199A	9965 000 32642	Y
Y-Board	LJ92-01200A	9965 000 32643	LJ92-01200A	9965 000 32643	Y
SMPS (PSU)	LJ44-00092A	9965 000 29202	LJ44-00101A	9965 000 29210	N
SUB PSU	-	-	-	-	-

Table 10-8 Spare parts overview 42" HD v4 (Part 2)

PDP type	42" HD v4					Service Information 9322 233 80682 being backwards compatible tbd
PDP model 12NC	9322 226 95682			9322 233 80682		
PDP model type and version	S42AX-YD01 (PP42AX-008A)		PWB's from PP42AX-007A and PP42AX-008A being Compatible	S42AX-YD01 (PP42AX-008B)		PWB's from PP42AX-008A and PP42AX-008B being compatible
Remarks	(SMPS Rev.0.65) New SMPS supply:LJ44-00101C + cables. Service information: tbd			(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service information: tbd		
Logic-Buffer (E)	LJ92-01054A	9965 000 29197	Y	LJ92-01054A	9965 000 29197	Y
Logic-Buffer (F)	LJ92-01055A	9965 000 29198	Y	LJ92-01055A	9965 000 29198	Y
Logic-Buffer (G)	-	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-	-
Y-Buffer (up)	LJ92-01202A	9965 000 32639	Y	LJ92-01202A	9965 000 32639	Y
Y-Buffer (down)	LJ92-01203A	9965 000 32640	Y	LJ92-01203A	9965 000 32640	Y
Logic-Board	LJ92-01270B	9965 000 32641	Y	LJ92-01270B	9965 000 32641	Y
SUBL	-	-	-	-	-	-
SUBR	-	-	-	-	-	-
X-Board	LJ92-01199A	9965 000 32642	Y	LJ92-01199A	9965 000 32642	Y
Y-Board	LJ92-01200A	9965 000 32643	Y	LJ92-01200A	9965 000 32643	Y
SMPS (PSU)	LJ44-00101B	9965 000 32630	N	LJ44-00101C	9965 000 33880	Y
SUB PSU	-	-	-	-	-	-

Table 10-9 Spare parts overview 50" HD v3

PDP type	50" HD v3					
PDP model 12NC	9322 215 26682					
PDP model type and version	S50HW-XD03 (PP50HW004C)					
Remarks	Lead type boards being phased out				Lead Free type being compatible with Lead type PWB	
Boards	Codes for leaded type PWBs		Codes for lead-free typePWBs			
Logic-Buffer (E)	LJ92-00917A	9965 000 25117	LJ92-00917B	9965 000 32614	Y	
Logic-Buffer (F)	LJ92-00918A	9965 000 25118	LJ92-00918B	9965 000 32615	Y	
Logic-Buffer (G)	LJ92-00919A	9965 000 25119	LJ92-00919B	9965 000 32646	Y	
Logic-Buffer (H)	LJ92-00920A	9965 000 25120	LJ92-00920B	9965 000 32647	Y	
Logic-Buffer (I)	LJ92-00921A	9965 000 25121	LJ92-00921B	9965 000 32648	Y	
Logic-Buffer (J)	LJ92-00922A	9965 000 25122	LJ92-00922B	9965 000 32649	Y	
Y-Buffer (up)	LJ92-00880A	9965 000 25123	LJ92-00880B	9965 000 32650	Y	
Y-Buffer (down)	LJ92-00881A	9965 000 25124	LJ92-00881B	9965 000 32651	Y	
Logic-Board	LJ92-00949C	9965 000 25125	LJ92-01224B	9965 000 32652	Y	
SUBL	LJ92-00923A	9965 000 25126	LJ92-00923B	9965 000 32653	Y	
SUBR	LJ92-00959A	9965 000 25127	LJ92-00959B	9965 000 32654	Y	
X-Board	LJ92-00852A	9965 000 25128	LJ92-00852B	9965 000 32655	Y	
Y-Board	LJ92-00853A	9965 000 25129	LJ92-00853B	9965 000 32656	Y	
SMPS (PSU)	LJ44-000 65A	9965 000 25130	LJ44-00065B	9965 000 32657	Y	
SUB PSU	LJ44-000 99A	9965 000 26195	LJ44-00099B	9965 000 32658	Y	

Table 10-10 Spare parts overview 50” HD v4 (Part 1)

PDP type	50" HD v4				
PDP model 12NC	9322 226 54682		9322 226 97682		
PDP model type and version	S50HW-XD04 (PP50HW-005A)		S50HW-XD04 (PP50HW-005B)		
Remarks	Codes for PWBs from 932222654682 PP50H-005A New SMPS supply:LJ44-00108C + cables. Service information: tbd		Codes for PWBs from 932222697682 PP50H-005B New SMPS supply:LJ44-00108C + cables. Service information: tbd		PWB's from PP50HW-005A and PP50HW-005B being compatible
Logic-Buffer (E)	LJ92-01103A	9965 000 30025	LJ92-01103A	9965 000 30025	Y
Logic-Buffer (F)	LJ92-01104A	9965 000 30026	LJ92-01104A	9965 000 30026	Y
Logic-Buffer (G)	LJ92-01105A	9965 000 30027	LJ92-01105A	9965 000 30027	Y
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01047A	9965 000 30028	LJ92-01047A	9965 000 30028	Y
Y-Buffer (down)	LJ92-01048A	9965 000 30029	LJ92-01048A	9965 000 30029	Y
Logic-Board	LJ92-01269B	9965 000 30032	LJ92-01269B	9965 000 30032	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-01045A	9965 000 30024	LJ92-01045A	9965 000 30024	Y
Y-Board	LJ92-01046A	9965 000 30030	LJ92-01046A	9965 000 30030	Y
SMPS (PSU)	LJ44-00108A	9965 000 33390	LJ44-00108B	9965 000 30031	N
SUB PSU	-	-	-	-	-

Table 10-11 Spare parts overview 50” HD v4 (Part 2)

PDP type	50" HD v4		Service information: 932223379682 being backwards compatible: tdb
PDP model 12NC	9322 233 79682		
PDP model type and version	S50HW-XD04 (PP50HW-005B)		PWB's from PP50HW-005B and PP50HW-005E being compatible
Remarks	Codes for PWBs from 932223379682 PP50H-005E		
Logic-Buffer (E)	LJ92-01103A	9965 000 30025	Y
Logic-Buffer (F)	LJ92-01104A	9965 000 30026	Y
Logic-Buffer (G)	LJ92-01105A	9965 000 30027	-
Logic-Buffer (H)	-	-	-
Logic-Buffer (I)	-	-	-
Logic-Buffer (J)	-	-	-
Y-Buffer (up)	LJ92-01047A	9965 000 30028	Y
Y-Buffer (down)	LJ92-01048A	9965 000 30029	Y
Logic-Board	LJ92-01269B	9965 000 30032	Y
SUBL	-	-	-
SUBR	-	-	-
X-Board	LJ92-01045A	9965 000 30024	Y
Y-Board	LJ92-01046A	9965 000 30030	Y
SMPS (PSU)	LJ44-00108C	9965 000 33879	Y
SUB PSU	-	-	-

Note: All 42- and 50-inch v4 panels are lead-free. Differences in table above are related to the SMPS (PSU).

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- **General:** Update of whole manual to the latest publication standards and information.
- **37" SD v4:** Errors corrected, and info updated.
- **42" SD v2:** Errors corrected, and info updated.
- **42" SD v3:** Errors corrected, and info updated.
- **42" SD v4:** New.
- **42" HD v3:** Errors corrected, and info updated.
- **42" HD v4:** New.
- **50" HD v3:** Errors corrected, and info updated.
- **50" HD v4:** New.

Manual xxxx xxx xxxx.2

- SMPS layouts and voltages updated
- Alignments updated
- Parts list updated

Manual xxxx xxx xxxx.3

- **General:** Correction of some minor errors.
- **Chapter 8, Alignments:** Errors corrected, and info updated.

Service Service Service

SDI PDP 2K6

S42SD-YD09 (42-inch SD, v5)
S42AX-YD02 (42-inch HD, w1)
S50HW-YD01 (50-inch HD, w1)
S63HW-XD05 (63-inch HD, v4)

Service Manual

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Subject to modification

EN 3122 785 16381



PHILIPS

1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

- 1.1 PDP Overviews
- 1.2 Serial Numbers
- 1.3 Chassis Overviews

Notes:

- Figures can deviate due to the different model executions.
- Specifications are indicative (subject to change).

1.1 PDP Overviews

Table 1-1 PDP overview

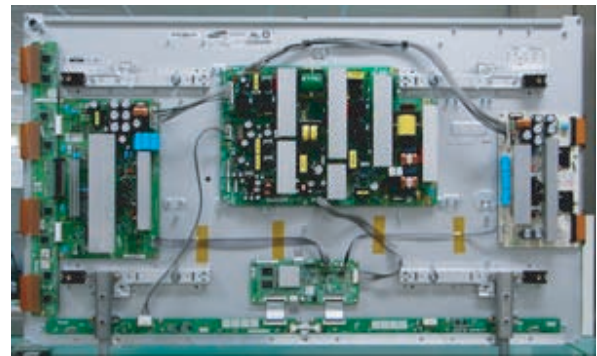
	PDP Type / Version	Model Name	H x V Pixel
1	42" SD v5	S42SD-YD09	852 x 480
2	42" HD w1	S42AX-YD02	1024 x 768
3	50" HD w1	S50HW-YD01	1366 x 768
4	63" HD v4	S63HW-XD05	1366 x 768

Table 1-2 PDP vs Chassis overview

Display type	Model #	Chassis	Chassis Manual #
42" SD v5	42PF5521D/10	LC4.41E AB	3122 785 16230
42" SD v5	42PF5521D/12	LC4.41E AB	3122 785 16230
42" HD w1	42PF9431D/37	BJ2.5U PA	3122 785 15930
42" HD w1	42PF9631D/37	BJ2.4U PA	3122 785 15920
50" HD w1	50PF9631D/37	BJ2.4U PA	3122 785 15920
50" HD w1	50PF9731D/37	BJ2.4U PA	3122 785 15920
63" HD v4	63PF9631D/37	BJ3.0U PA	3122 785 16460

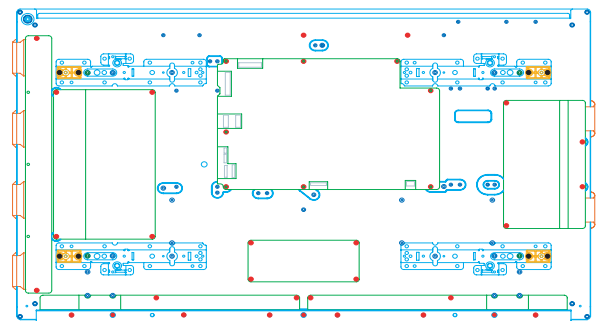
In above table the link is given between the SDI Plasma Display Panel and the Philips TV chassis (incl. chassis manual no.).

1.1.1 42" SD v5



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Figure 1-1 Rear view of plasma panel (42" SD v5)



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Figure 1-2 Location of mounting screws (42" SD v5)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 42" SD v5	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 (H) mm x 1.110 (V) mm	
4	Cell Pitch	R	0.365 (H) mm x 1.110 (V) mm
		G	0.365 (H) mm x 1.110 (V) mm
		B	0.365 (H) mm x 1.110 (V) mm
5	Display size	932.940 (H) x 532.800 (V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours (8-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 54 (D) mm	
11	Weight	1 Module	About 15.4 kg
14	Vertical frequency and Video/Logic Interface	60 Hz/ 50 Hz, LVDS	

1.1.2 42" HD w1

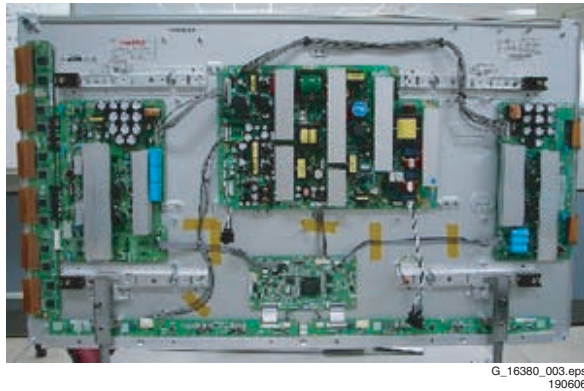


Figure 1-3 Rear view of plasma panel (42" HD w1)

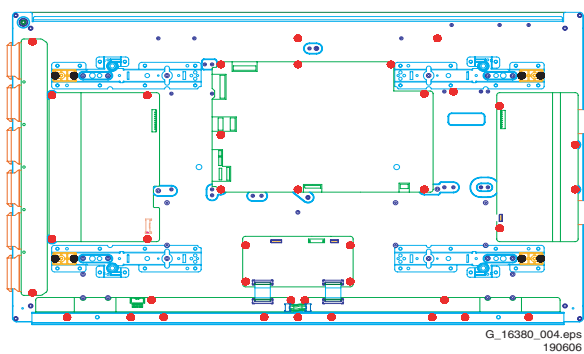


Figure 1-4 Location of mounting screws (42" HD w1)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 42" HD w1	
1	Pixel	1,024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)	
3	Pixel Pitch	0.912mm (H) x 0.693mm (V)	
4	Cell Pitch	R	Horizontal 0.304 mm Vertical 0.693 mm
		G	Horizontal 0.304 mm Vertical 0.693 mm
		B	Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	933.89 (H) x 532.22 (V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	1073.7 million colours (10-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 54 (D) mm	
11	Weight	1 Module	About 16.8 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.3 50" HD w1

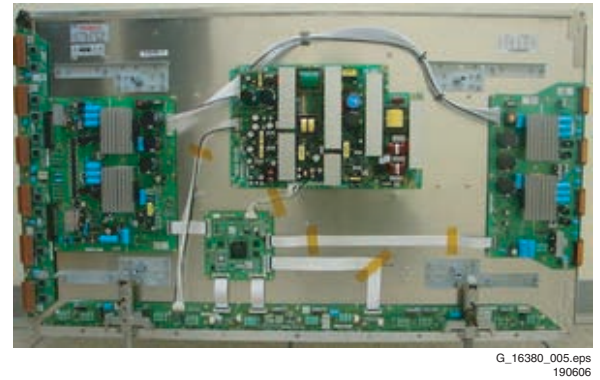


Figure 1-5 Rear view of plasma panel (50" HD w1)

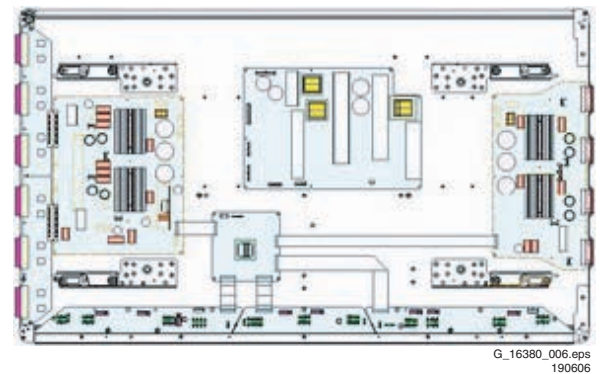


Figure 1-6 Location of mounting screws (50" HD w1)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 50" HD w1	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	0.810 mm (H) x 0.810 mm (V)	
4	Cell Pitch	R	Horizontal 0.270 mm Vertical 0.810 mm
		G	Horizontal 0.270 mm Vertical 0.810 mm
		B	Horizontal 0.270 mm Vertical 0.810 mm
5	Display size	1106.46 mm (H) x 622.08 mm (H)	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	549.75 billion colours (13-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1175 (W) x 678.5 (H) x 63.8 (D) mm	
11	Weight	Module 1	About 18.0 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.4 63" HD v4

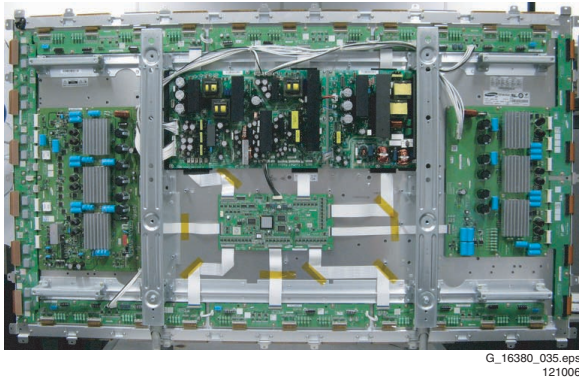


Figure 1-7 Rear view of plasma panel (63" HD v4)

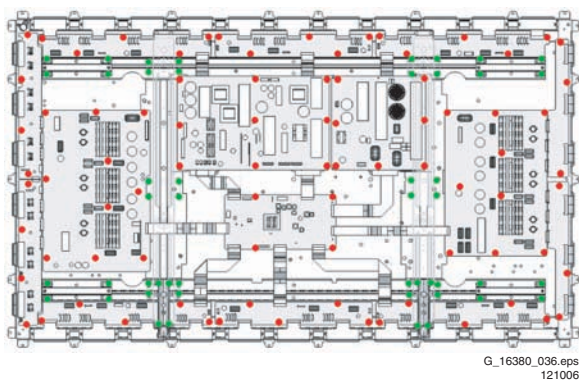


Figure 1-8 Location of mounting screws (63" HD v4)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 63" HD v4	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	1.02 mm (H) x 1.02 mm (V)	
4	Cell Pitch	R	Horizontal 0.34 mm Vertical 1.02 mm
		G	Horizontal 0.34 mm Vertical 1.02 mm
		B	Horizontal 0.34 mm Vertical 1.02 mm
5	Display size	1393.3 mm (H) x 783.4 mm (H)	
6	Screen size	Diagonal 63" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	1073.7 million colours (13-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	approx. 1680 (W) x 875 (H) x 750 (D) mm	
11	Weight	Module 3	About 44.0 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.2 Serial Numbers

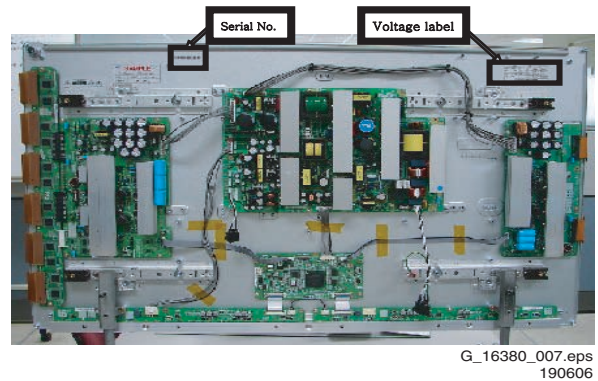


Figure 1-9 Location of the serial number

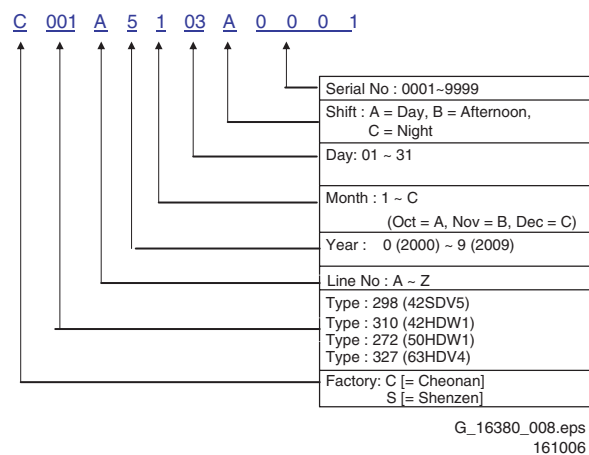
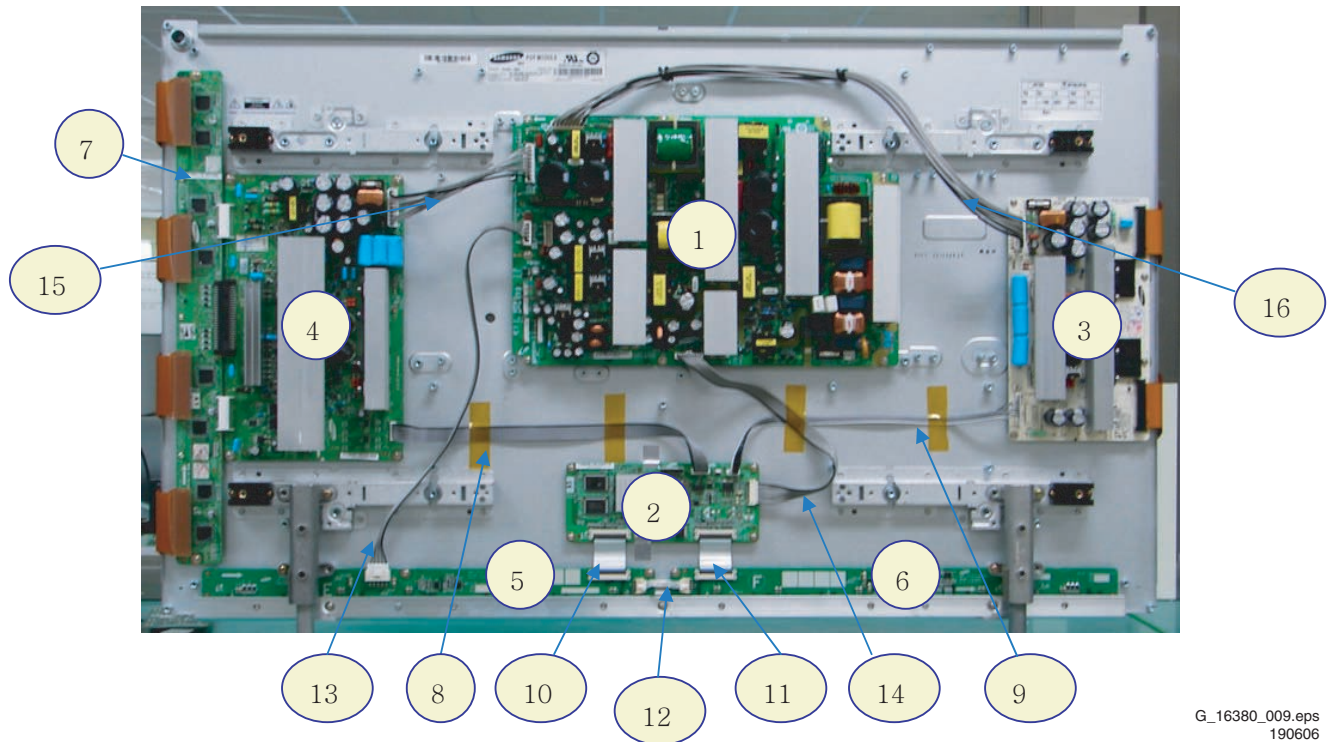


Figure 1-10 Explanation of the serial number

1.3 Chassis Overviews

1.3.1 42" SD v5



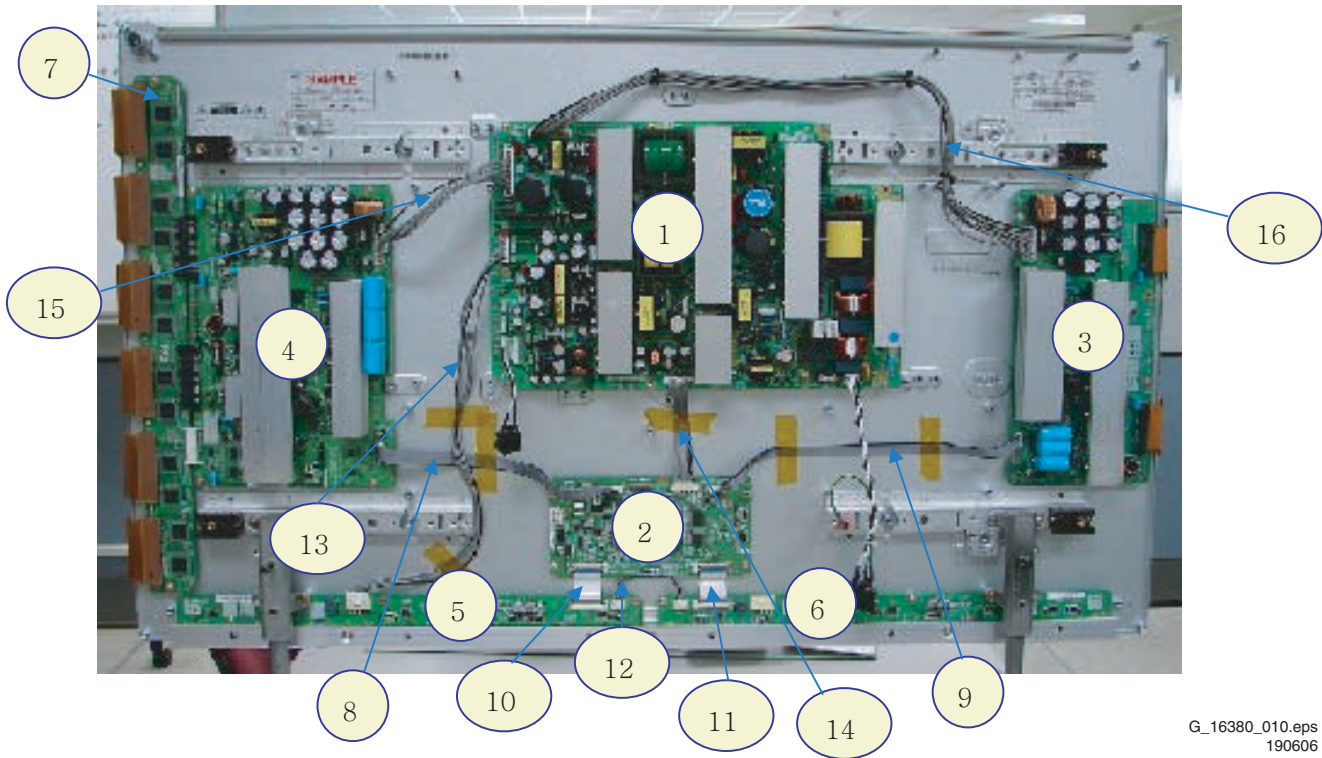
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Figure 1-11 PWB location (42" SD v5)

Table 1-3 PWB overview (42" SD v5)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB Logic Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB buffer
6	LOGIC F BUFFER Board	Assy PWB buffer
7	Y-BUFFER Board	Assy PWB buffer
8	LOGIC + Y-MAIN	Lead connector
9	LOGIC + X-MAIN	Lead connector
10	LOGIC + LOGIC BUF (E)	FFC cable-flat
11	LOGIC + LOGIC BUF (F)	FFC cable-flat
12	LOGIC BUF (E) + (F)	Lead connector
13	SMPS + LOGIC BUF (E)	Lead connector
14	SMPS + LOGIC MAIN	Lead connector
15	SMPS + Y-MAIN	Lead connector
16	SMPS + X-MAIN	Lead connector

1.3.2 42" HD w1



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Figure 1-12 PWB location (42" HD w1)

Table 1-4 PWB overview (42" HD w1)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER Board	Assy PWB Buffer
8	LOGIC + Y-MAIN	Lead connector
9	LOGIC + X-MAIN	Lead connector
10	LOGIC + LOGIC BUF(E)	FFC Cable-flat
11	LOGIC + LOGIC BUF(F)	FFC Cable-flat
12	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
13	SMPS + LOGIC BUF(E)	Lead connector
14	SMPS + LOGIC MAIN	Lead connector
15	SMPS + Y-MAIN	Lead connector
16	SMPS + X-MAIN	Lead connector

1.3.3 50" HD w1

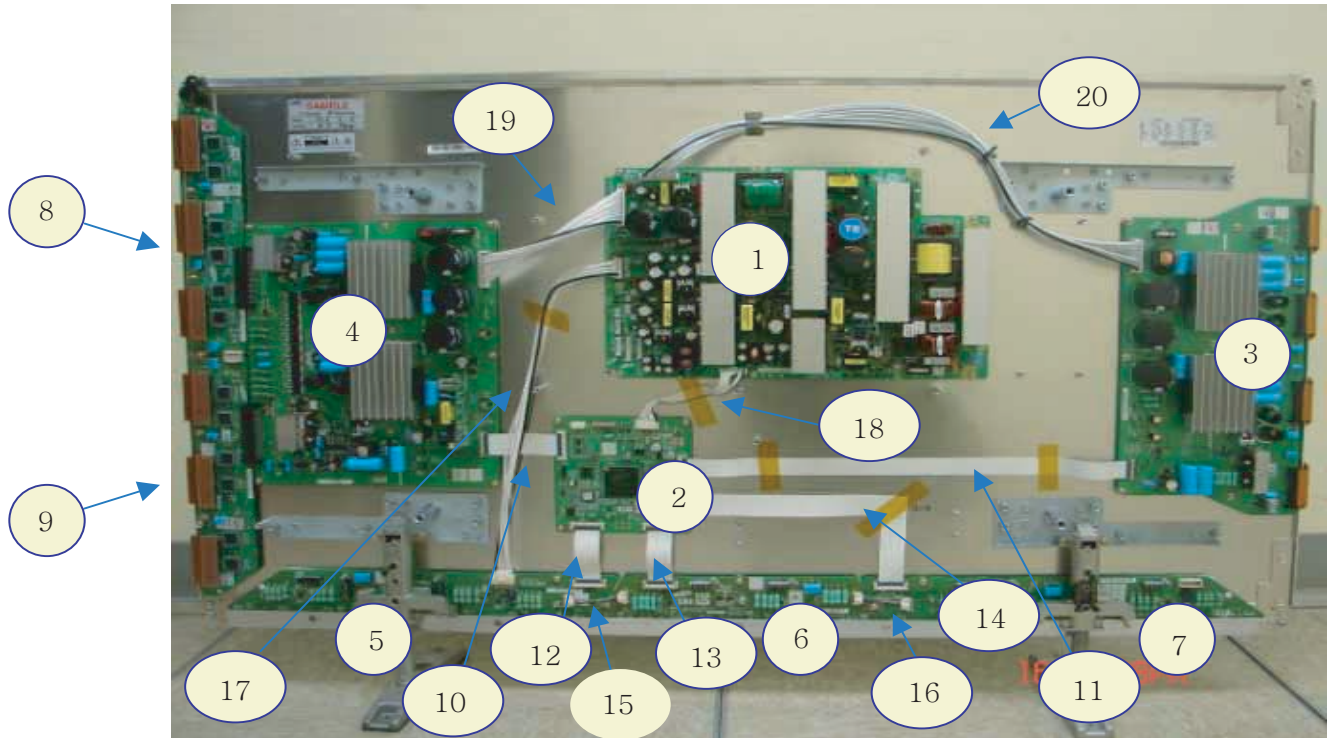
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Figure 1-13 PWB location (50" HD w5)

Table 1-5 PWB overview (50" HD w1)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer E
6	LOGIC F BUFFER Board	Assy PWB Buffer F
7	LOGIC G BUFFER Board	Assy PWB Buffer G
8	Y-BUFFER (Upper) Board	Assy PWB Buffer
9	Y-BUFFER (Lower) Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOGIC BUF (E)	FFC Cable-flat
13	LOGIC + LOGIC BUF (F)	FFC Cable-flat
14	LOGIC + LOGIC BUF (G)	FFC Cable-flat
15	LOGIC BUF (E) + LOG. BUF (F)	Lead connector
16	LOGIC BUF (F) + LOG. BUF (G)	Lead connector
17	SMPS + LOGIC BUF (E)	Lead connector
18	SMPS + LOGIC MAIN	Lead connector
19	SMPS + Y-MAIN	Lead connector
20	SMPS + X-MAIN	Lead connector

1.3.4 63" HD v4

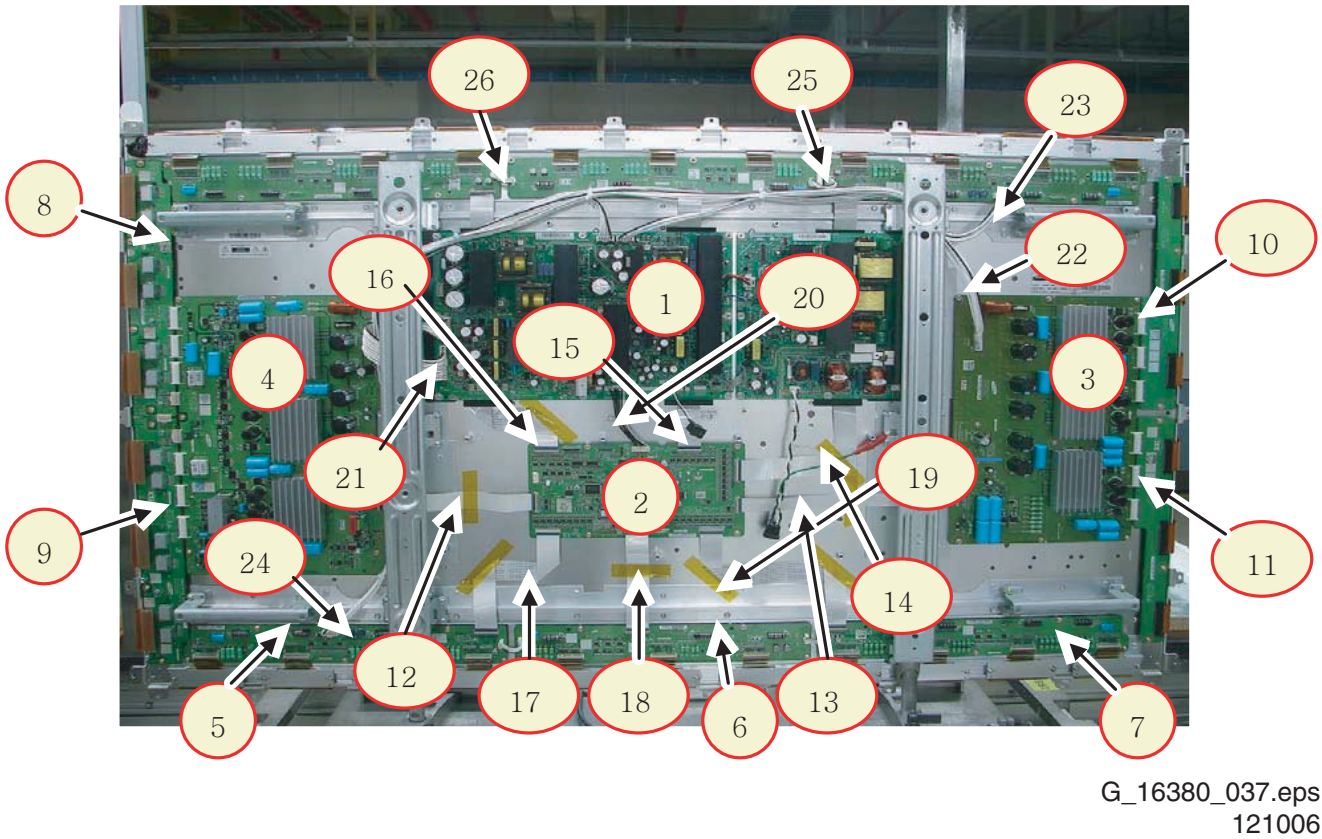


Figure 1-14 PWB location (63" HD v4)

Table 1-6 PWB overview (50" HD w1)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer E
6	LOGIC F BUFFER Board	Assy PWB Buffer F
7	LOGIC G BUFFER Board	Assy PWB Buffer G
8	Y-BUFFER (Upper) Board	Assy PWB Buffer
9	Y-BUFFER (Lower) Board	Assy PWB Buffer
10	X-BUFFER (Upper) Board	Assy PWB Buffer
11	X-BUFFER (Lower) Board	Assy PWB Buffer
12	LOGIC + Y-MAIN	FFC Cable-flat
13	LOGIC + X-MAIN	FFC Cable-flat
14	LOGIC + LOGIC BUF upper (E)	FFC Cable-flat
15	LOGIC + LOGIC BUF upper (F)	FFC Cable-flat
16	LOGIC + LOGIC BUF upper (G)	FFC Cable-flat
17	LOGIC + LOGIC BUF lower (E)	FFC Cable-flat
18	LOGIC + LOGIC BUF lower (F)	FFC Cable-flat
19	LOGIC + LOGIC BUF lower (G)	FFC Cable-flat
20	SMPS + LOGIC MAIN	Lead connector
21	SMPS + Y-MAIN	Lead connector
22	SMPS + X-MAIN	Lead connector
23	SMPS + LOGIC BUF upper (E)	Lead connector
24	SMPS + LOGIC BUF lower (E)	Lead connector
25	LOGIC BUF (E) + LOG. BUF (F)	Lead connector
26	LOGIC BUF (F) + LOG. BUF (G)	Lead connector

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

- 2.1 Handling Precautions
- 2.2 Safety Precautions
- 2.3 Notes

Notes:

- Only authorised persons should perform servicing of this module.
- When using/handling this unit, pay special attention to the PDP Module: it should not be enforced into any other way than next rules, warnings, and/or cautions.
- **"Warning"** indicates a hazard that may lead to death or injury if the warning is ignored and the product is handled incorrectly.
- **"Caution"** indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

2.1 Handling Precautions

- The PDP module use high voltage that is dangerous to humans. Before operating the PDP, always check for dust to prevent short circuits. Be careful touching the circuit device when power is "on".
- The PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- The PDP module has a lot of electric devices. The service engineer must wear equipment (for example, earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- The PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. The operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is "off". Operator must wait for discharging of remaining voltage during at least 1 minute.

2.2 Safety Precautions

2.2.1 Safety Precautions

- Before replacing a board, discharge forcibly the remaining electricity from the board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.
- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuff including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change: Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, it cause danger on safety. And, if you change the design or insert, manufacturer guarantee will be not effect.
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between

parts and circuit board. Check the cord of AC power preparing damage.

- Product Safety Mark: Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned "off", before next repair.
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

2.2.2 ESD Precautions

There are parts, which are easily damaged by electrostatics (for example Integrated Circuits, FETs, etc.) Electrostatic damage rate of product will be reduced by the following technics:

- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring (it must be operated after removing dust on it. It comes under precaution of electric shock).
- After removing the assembly, lay it with the tracks on a conductive surface to prevent charging.
- Do not use chemical stuff containing Freon. It generates positive electric that can damage ESD sensitive devices.
- You must use a soldering device for ground-tip when soldering or de-soldering these devices.
- You must use anti-static solder removal device. Most removal devices do not have antistatic which can charge a enough positive electric enough for damaging these devices.
- Before removing the protective material from the lead of a new device, bring the protective material into contact with the chassis or assembly.
- When handing an unpacked device for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the device.
- Do not take a new device from the protective case until the it is ready to be installed. Most devices have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminium)

2.3 Notes

A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel, it is recommended to do some maintenance by a qualified service employee only.

2.3.1 Safe PDP Handling

- The work procedures shown with the "Note" indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times, other than when adjusting and checking the product, be sure to turn "off" the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of PWBs, start the servicing work at least 30 seconds after the main power has been turned "off". Especially when installing and removing the Power Supply PWB and the SUS PWB in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned "off".

- While the main power is “on”, do not touch any parts or circuits other than the ones specified. The high voltage Power Supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit PWB, be sure to remove static electricity from your body before handling the circuit PWB.
- Be sure to handle the circuit PWB by holding the large parts as the heat sink or transformer. Failure to observe this

precaution may result in the occurrence of an abnormality in the soldered areas.

- Do not stack the circuit PWB. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original

3. Directions For Use

Not applicable.

4. Mechanical Instructions

Index of this chapter:

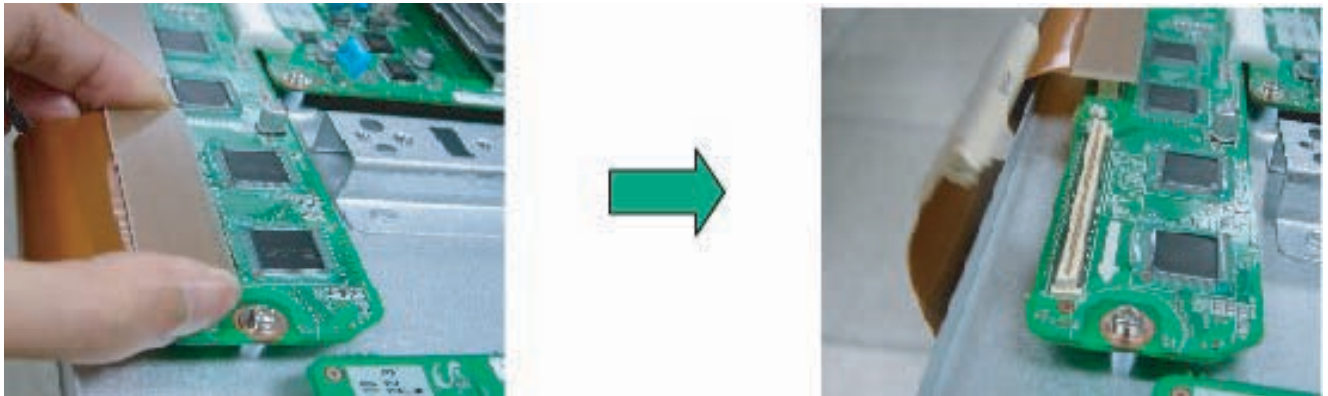
- 4.1 Dis-assembling / Re-assembling
 - 4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)
 - 4.1.2 Flat Cable Connector of X-main Board
 - 4.1.3 FFC and TCP from Connector
 - 4.1.4 Exchange of LBE and LBF board - 42" SD v5
 - 4.1.5 Exchange of LBE and LBF board - 42" HD w1
 - 4.1.6 Exchange of LBE, LBF and LBG board - 50" HD w1
 - 4.1.7 Exchange of LB-E, LB-F and LB-G board - 63" HD v4
 - 4.1.8 Exchange YB and YM board - 42" SD v5
 - 4.1.9 Exchange YB and YM board - 42" HD w1
 - 4.1.10 Exchange YBU, YBL and YM board - 50" HD w1
 - 4.1.11 Exchange YBU, YBL and YM board - 63" HD v4

4.1 Dis-assembling / Re-assembling

4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)

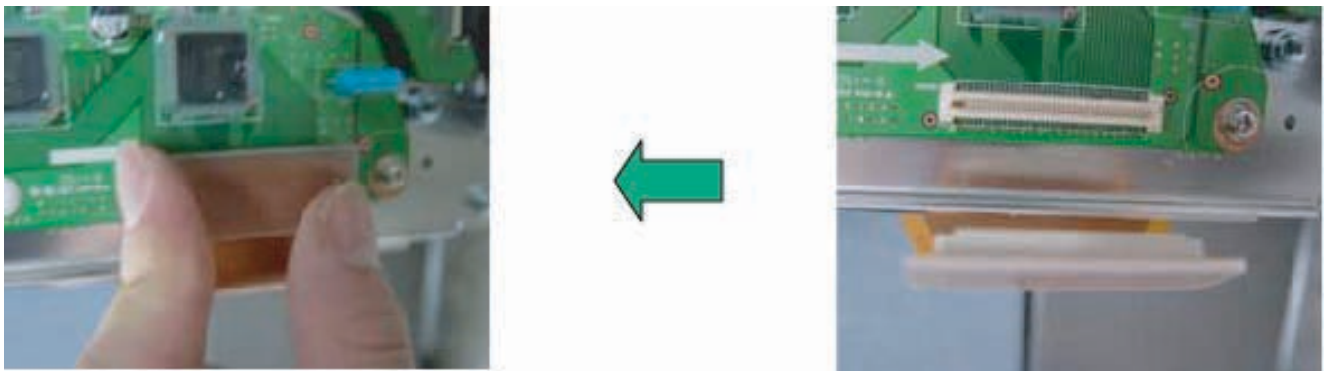
- Dis-assembly: Pull out the FPC from the connector by holding the lead of the FPC with both hands.
- Re-assembly: Push the lead of FPC with same force on both sides into the connector.

Note: Be careful not to damage the connector pin during connecting.



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Figure 4-1 Dis-assembly FPC of Y-buffer

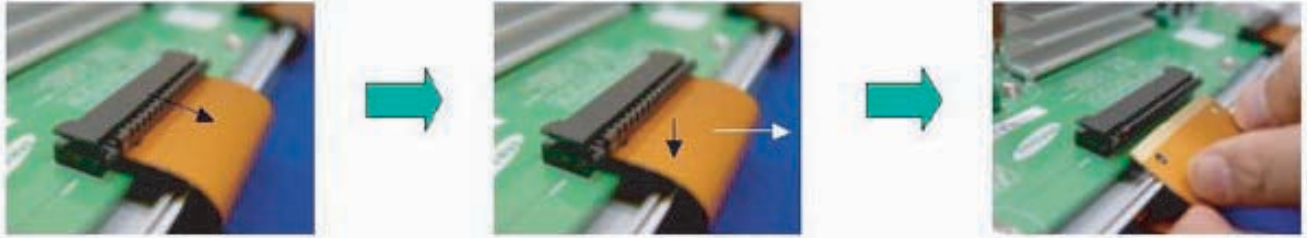


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Figure 4-2 Re-assembly FPC of Y-buffer

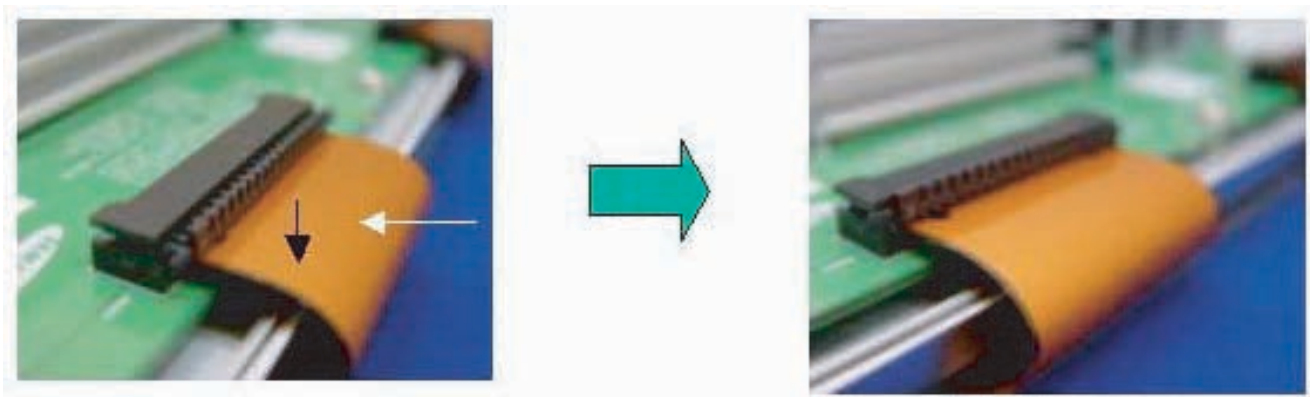
4.1.2 Flat Cable Connector of X-main Board

- Dis-assembly:
 1. Pull out the clamp of connector.
 2. Pull Flat cable out press down lightly.
 3. Turn the Flat Cable reversely.
- Re-assembly: Put the Flat Cable into the connector press down lightly until you hear a "Click".



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Figure 4-3 Dis-assembly FCC of X-main board



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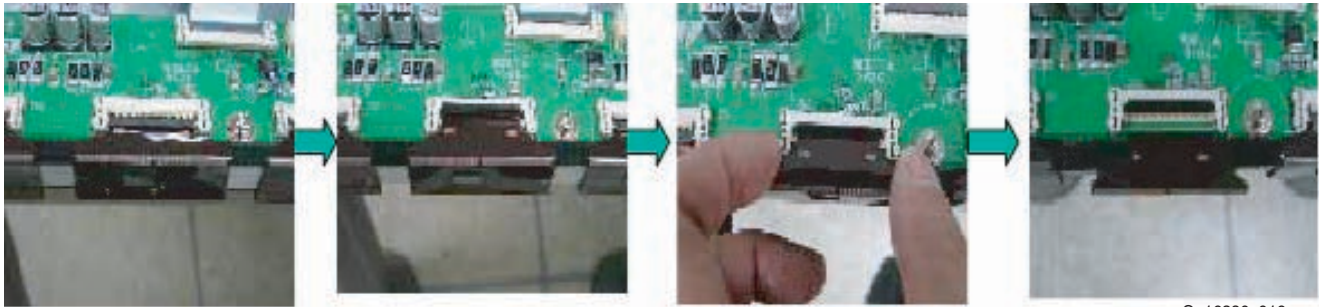
Figure 4-4 Re-assembly FCC of X-main board

4.1.3 FFC and TCP from Connector

- Dis-assembling of TCP:
 1. Open the clamp carefully.
 2. Pull the TCP out from its connector.
- Re-assembling of TCP:
 1. Put the TCP into the connector carefully
 2. Close the clamp completely, until you hear a "Click".

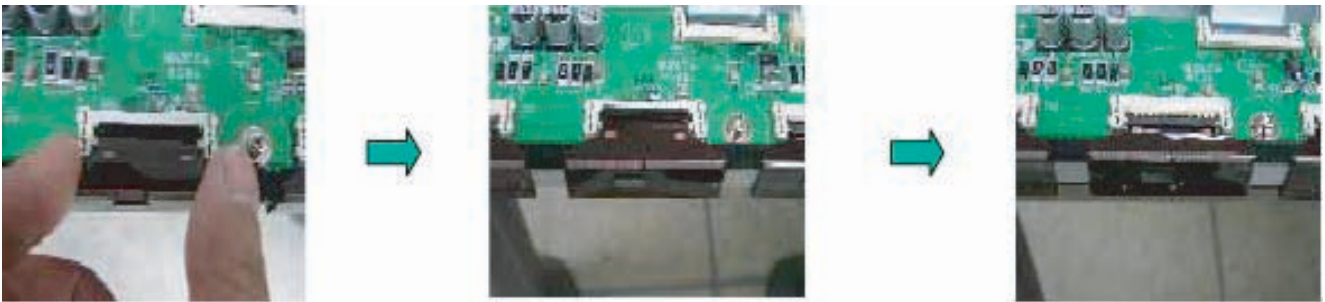
Notes:

- Checking whether the foreign material is on the connector inside before assembling of TCP.
- Be careful, do not damage the board by ESD during handling of TCP.



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Figure 4-5 Dis-assembly of TCP



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Figure 4-6 Re-assembly of TCP



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Figure 4-7 Mis-assembly of TCP



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Figure 4-8 Dis- and re-assembly of FFC

4.1.4 Exchange of LBE and LBF board - 42" SD v5

1. Remove the screws in order of 1-3-2 from the heatsink and remove the heatsink ("Photos 1 & 3")
2. Remove the TCP, FFC, and the power cable from the connectors.
3. Remove all the screws from the defective board ("Photo 2").
4. Remove the defective board.
5. Place the new board and screw it tight.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and the power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the screw mounting order 2-3-1.

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.

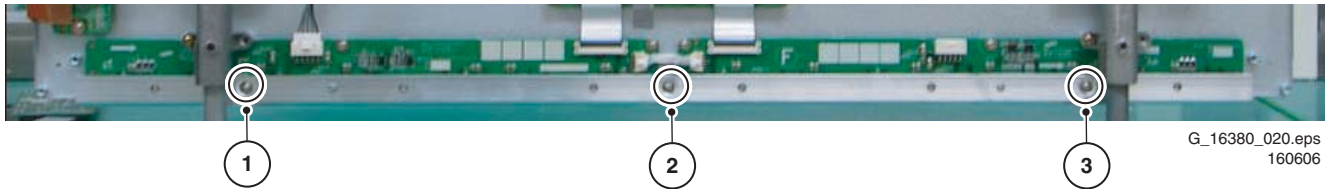


Figure 4-9 Photo 1 - Heatsink 42" SD v5

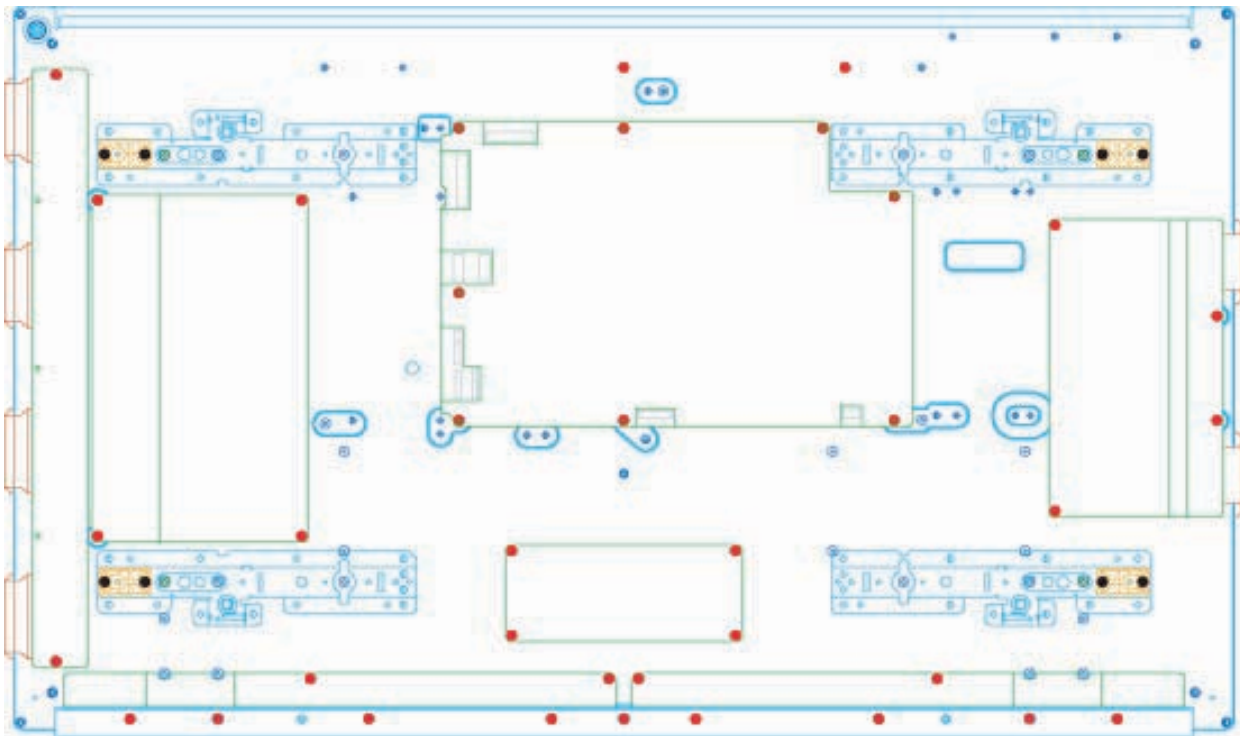


Figure 4-10 Photo 2 - Exchange of LBE and LBF board 42" SD v5

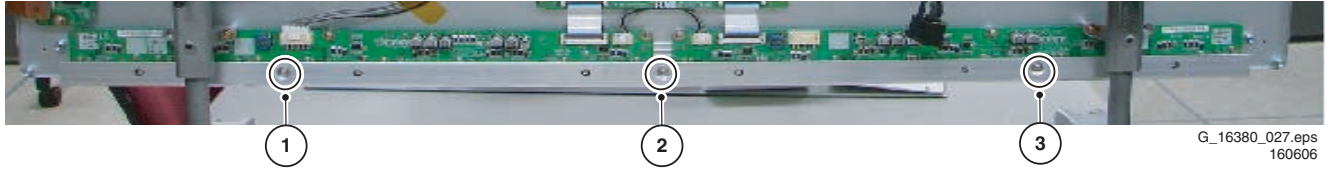


Figure 4-11 Photo 3 - Heat sink removal

4.1.5 Exchange of LBE and LBF board - 42" HD w1

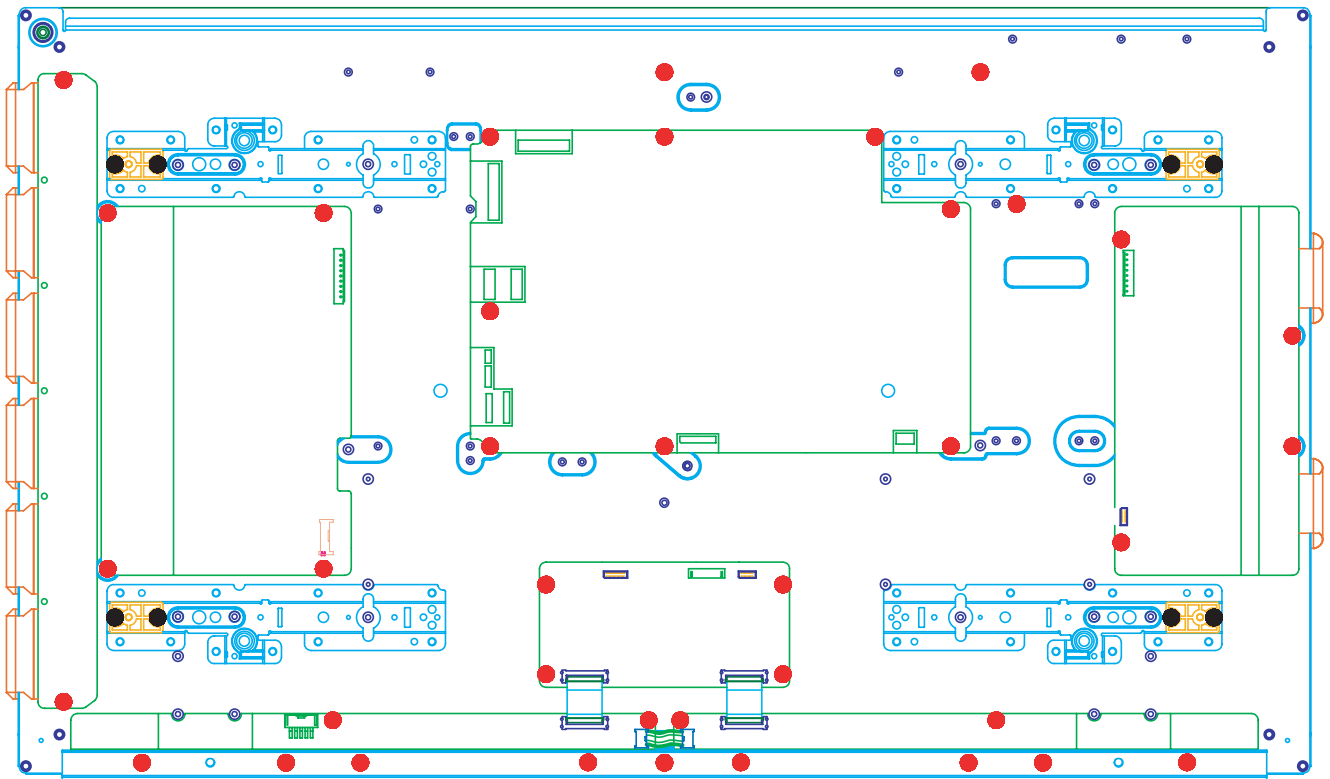
1. Remove the screws in order of 1-3-2 from the heatsink and remove the heatsink ("Photos 1 & 3").
2. Remove the TCP, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Place the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the screw mounting order 2-1-3.

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.



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Figure 4-12 Photo 1 - Heatsink 42" HD w1



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Figure 4-13 Photo 2 - Exchange of LBE, LBF board 42" HD w1



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Figure 4-14 Photo 3 - Heat sink removal

4.1.6 Exchange of LBE, LBF and LBG board - 50" HD w1

1. Remove the screws in order of 2-3-1-4 from the heatsink and remove the heatsink ("Photo 3").
2. Remove the TCP, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Replace the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the same screw mounting order as described above

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.



Figure 4-15 Photo 1 - Heatsink 50" HD w1

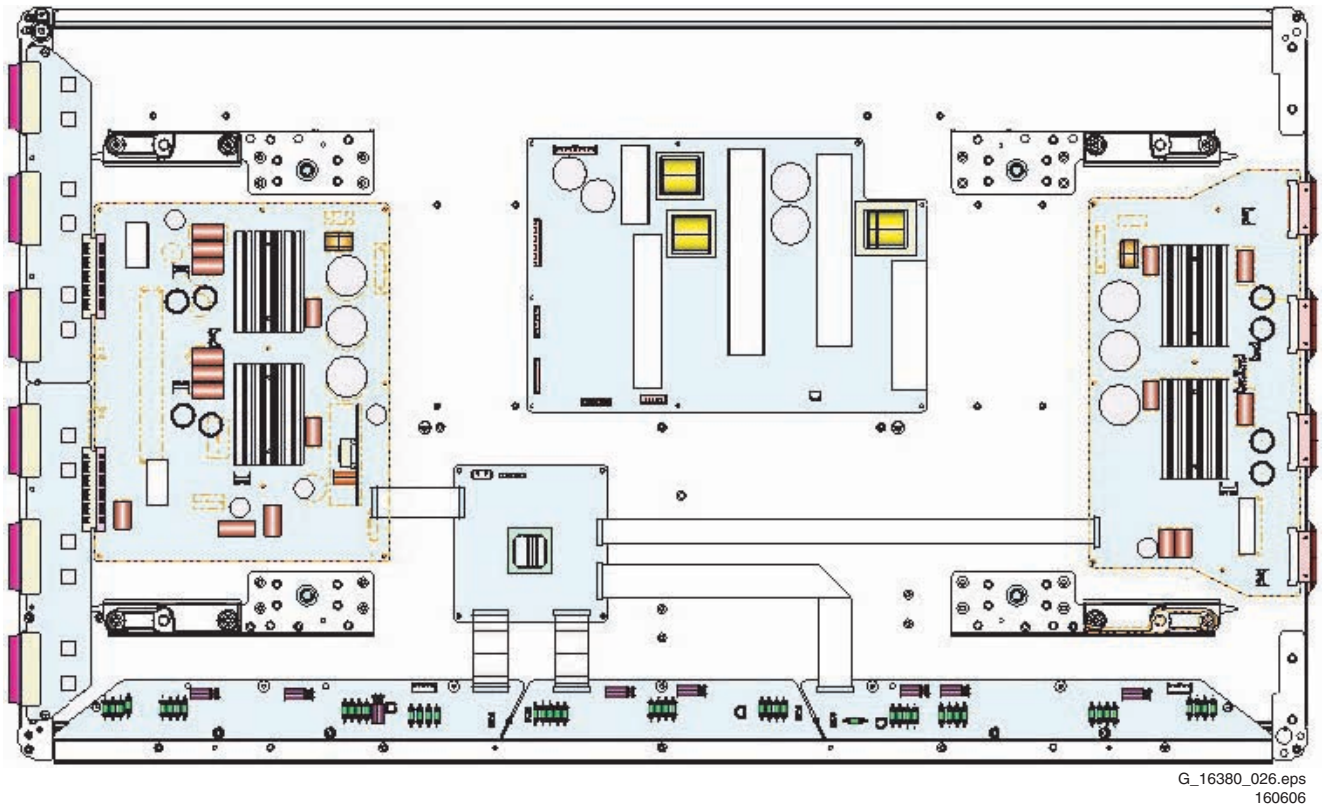


Figure 4-16 Photo 2 - Exchange of LBE, LBF, LBG board 50" HD w1



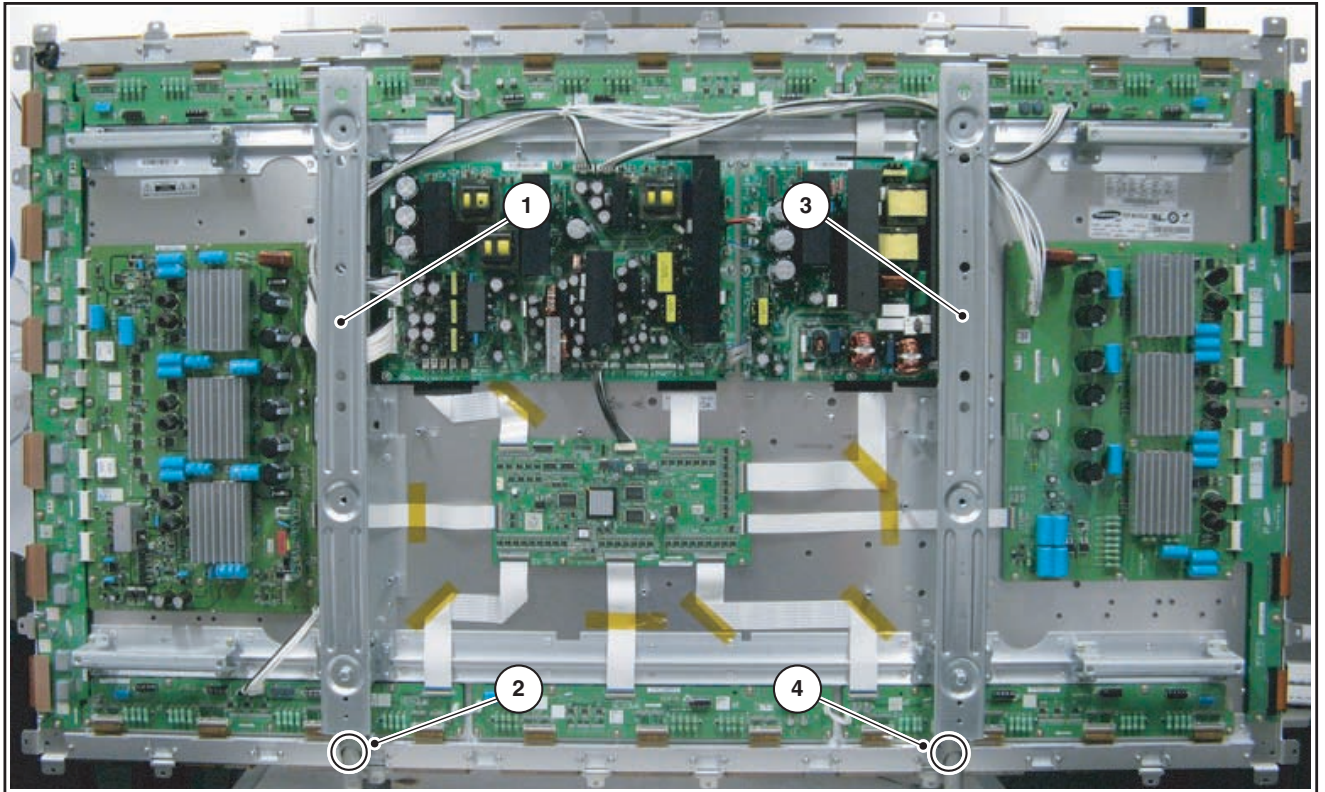
Figure 4-17 Photo 3 - Heat sink removal

4.1.7 Exchange of LB-E, LB-F and LB-G board - 63" HD v4

1. Refer to the Service Manual of the set to strip it so far, you have access to the Logic Buffer board that you need to replace.
2. For the lower LB-E, remove brackets [1] and [2]; for the lower LB-G, remove brackets [3] and [4]. For both LB-F's and the upper LB-E and LB-G you do not need to remove these brackets.

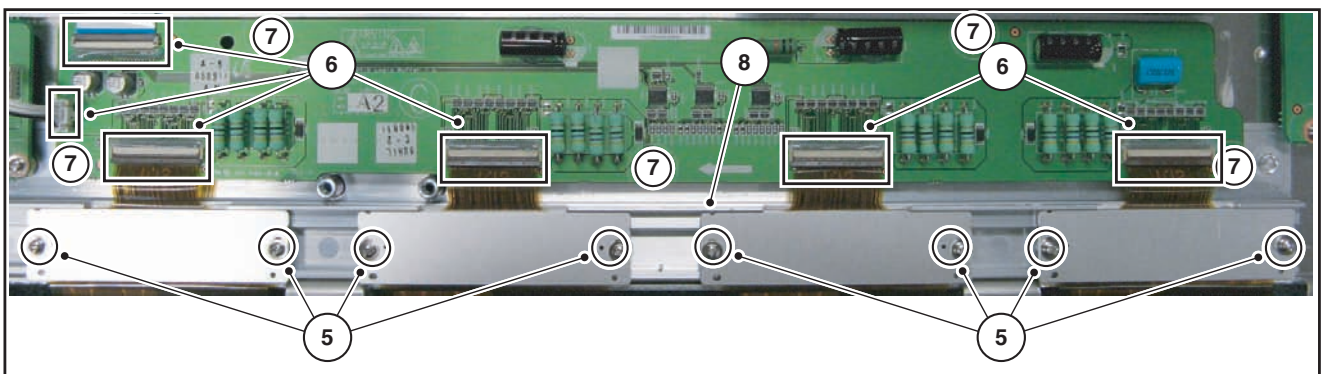
Note: The following description is correct for the lower LBG; the replacement procedure of the other LB's is similar.

3. Remove the fixation screws [5] from the TPC heatsinks of the defective board.
4. Unplug the TPC, FFC, and power cable(s) from the connectors [6].
5. Remove the fixation screws from the defective board [7].
6. Remove the defective board.
7. Replace the new board and then screw tightly.
8. Clean the connectors.
9. Re-connect the TCP, FFC, and power cable to the connectors.
10. Re-assemble the TCP heat sinks. Slide the heatsink against strip [8] before you tighten it.



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Figure 4-18 Brackets 63" HD v4

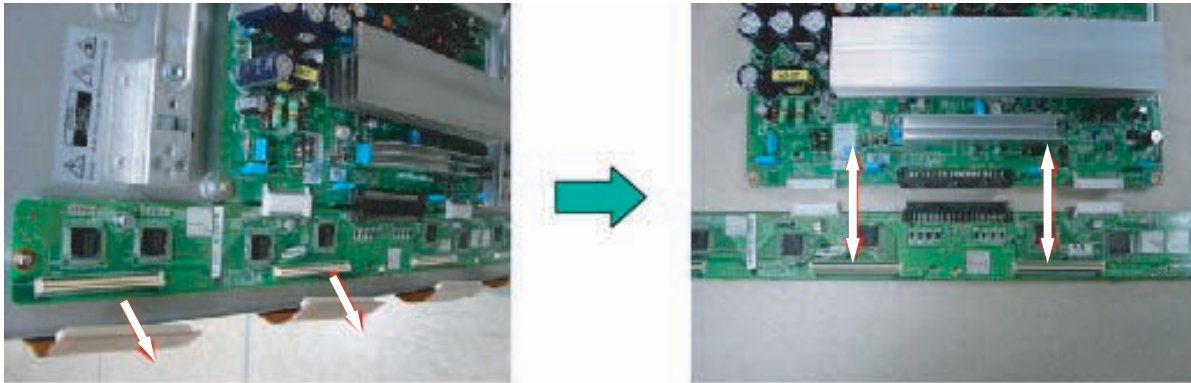


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Figure 4-19 Exchange of lower LB-G board 63" HD v4

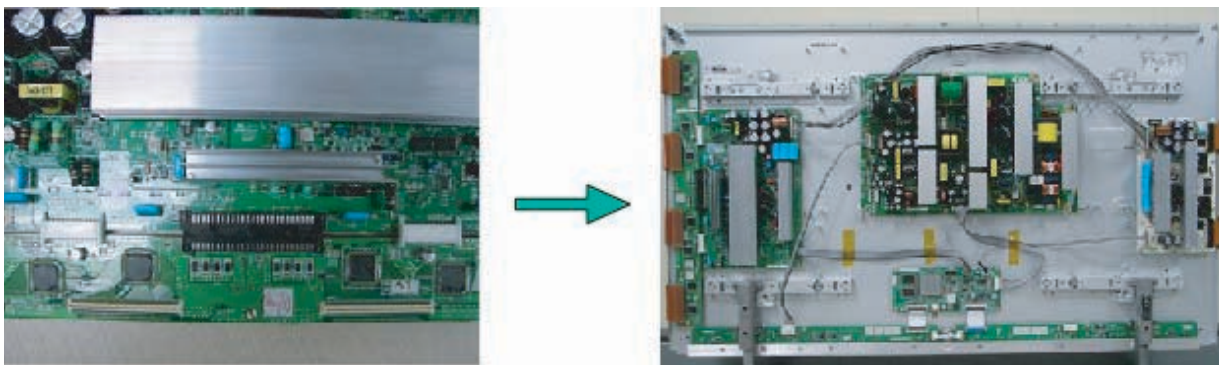
4.1.8 Exchange YB and YM board - 42" SD v5

1. Unplug all of the FPC connectors of Y-Buffer. See "Photo 1".
2. Unplug connectors CN5001 and CN5008 from Y-Main. See "Photo 2".
3. Loosen all the screws of Y-Buffer and Y-Main. See "Photo 3".
4. Remove the board from the chassis.
5. Unplug connectors CN5003, CN5004 and CN5005 between Y-Buffer and Y-Main.
6. Remove Y-Buffer from Y-main.
7. Replace the defective board.
8. Re-assemble Y-Buffer and Y-Main.
9. Plug in connectors CN5003, CN5004 and CN5005 between Y-Buffer and Y-Main. See "Photo 4".
10. Arrange the boards on the chassis and tighten them.
11. Connect the FPC connectors. See "Photo 5".
12. Supply the electric power to the module and then check the waveform of the board.
13. Turn "off" the power after the waveform is adjusted.



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Figure 4-20 Photo 1 and 2: Dis-assembly of YB and YM - 42" SD v5



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Figure 4-21 Photo 3 and 4: Re-assembly of YB and YM - 42" SD v5

4.1.9 Exchange YB and YM board - 42" HD w1

1. Unplug all of the FPC connectors of Y-Buffer. See "Photo 1".
2. Loosen all the screws of Y-Buffer and Y-Main. See "Photo 3".
3. Remove the board from the chassis.
4. Unplug connectors CN5004, CN5011 and CN5012 between Y-Buffer and Y-Main.
5. Remove Y-Buffer from Y-main.
6. Replace the defective board.
7. Re-assemble Y-Buffer and Y-Main.
8. Plug in connectors CN5004, CN5011 and CN5012 between Y-Buffer and Y-Main. See "Photo 4".
9. Arrange the boards on the chassis and tighten them.
10. Connect the FPC connectors.
11. Supply the electric power to the module and then check the waveform of the board.
12. Turn "off" the power after the waveform is adjusted.

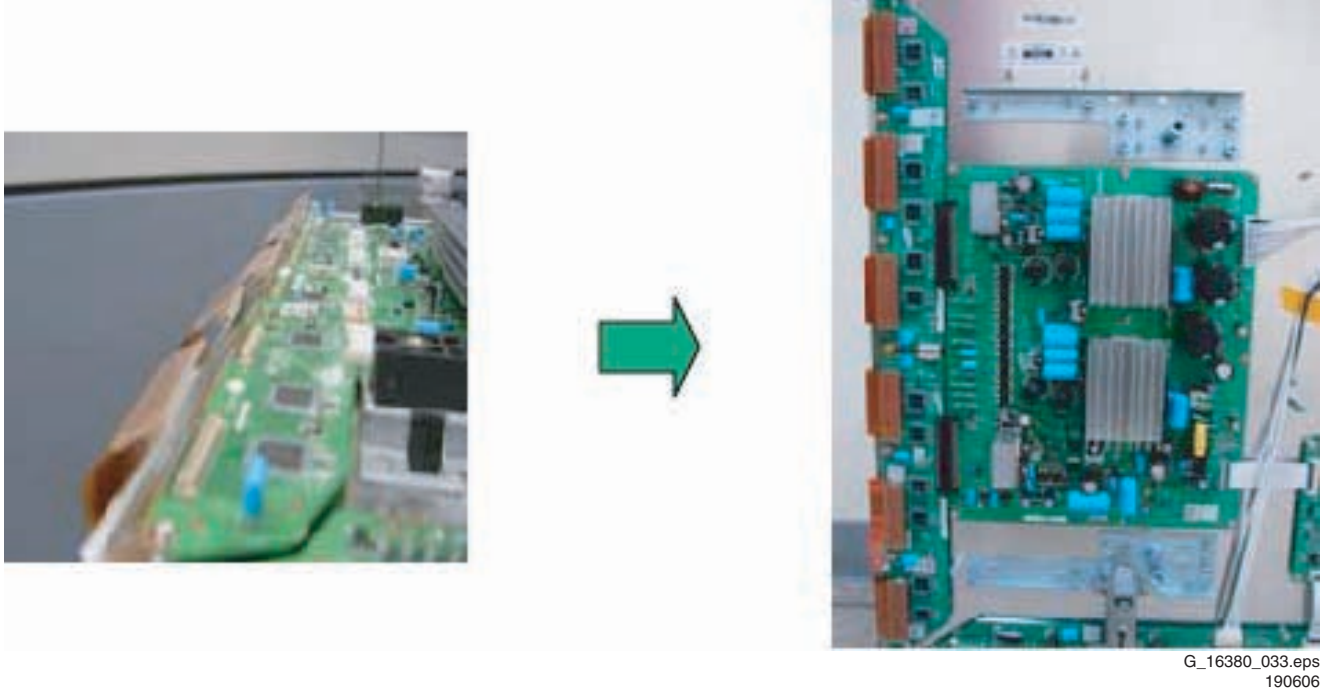
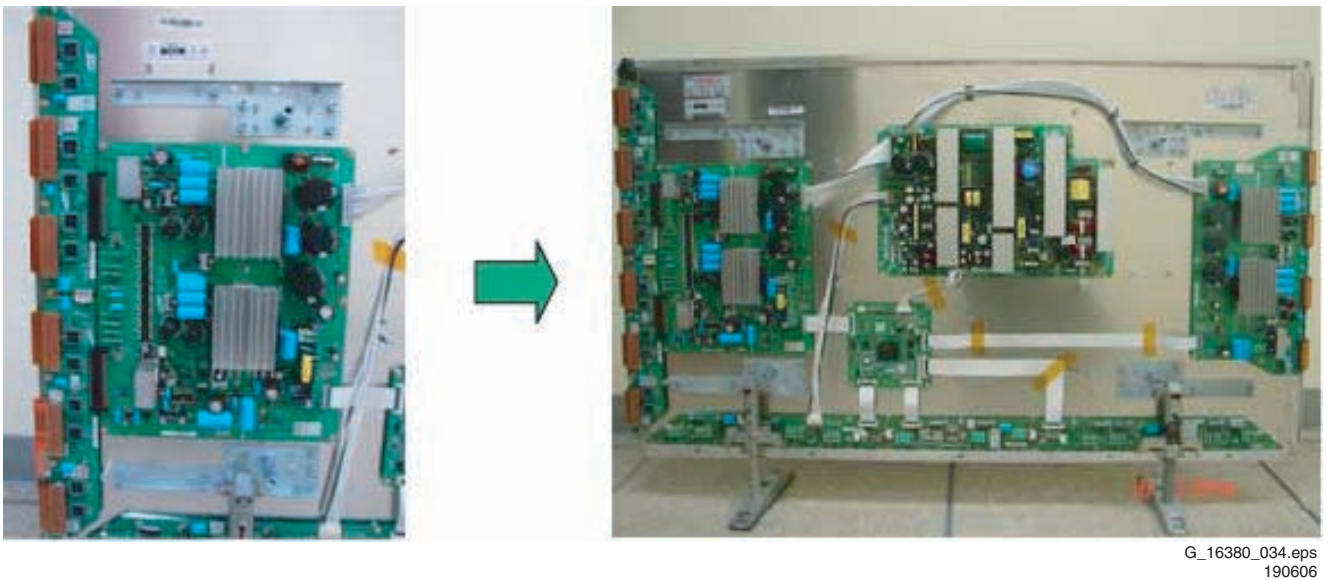


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Figure 4-22 Photo 1 and 2: Dis-assembly of YBU, YBL, and YM - 42" HD w1

4.1.10 Exchange YBU, YBL and YM board - 50" HD w1

1. Unplug all of the FPC connectors of YBU (Y-Buffer upper) and YBL (Y-Buffer lower). See "Photo 1".
2. Unplug the connector CN5412 between YBU and YBL.
3. Loosen all the screws of YBU, YBL, and Y-Main.
4. Remove the board from the chassis.
5. Remove the YBL and YBU from Y-main.
6. Replace the defective board.
7. Re-assemble the YBU and YBL to the Y-Main.
8. Plug in connector CN5412 between YBU and YBL.
9. Arrange the board on the chassis and then screw to fix.
10. Connect the FPCs.
11. Supply the electric power to the module and then check the waveform of the board.
12. Turn "off" the power after the waveform is adjusted.

**Figure 4-23 Photo 1 and 2: Dis-assembly of YBU, YBL, and YM - 50" HD w1****Figure 4-24 Photo 3 and 4: Re-assembly of YBU, YBL, and YM - 50" HD w1**

4.1.11 Exchange YBU, YBL and YM board - 63" HD v4

1. Unplug power connector CN5010 and signal connector CN5002 from Y-Main. See "Photo 1".
2. Unplug all FPC connectors of YBU (Y-Buffer upper) and YBL (Y-Buffer lower). See "Photo 1".
3. Open the connectors CN5001/CN5406 between YM and YBU, and CN5000/CN5506 between YM and YBL.
4. Loosen all the screws of YBU, YBL, and Y-Main.
5. Remove the boards from the chassis.
6. Open the connectors CN5410/CN5510 between YBU and YBL.
7. Separate the YBL and YBU from Y-main.
8. Replace the defective board.
9. Re-assemble the YBU and YBL to the Y-Main.
10. Plug in the connectors between YBU, YBL and YM.
11. Arrange the board on the chassis and then screw to fix.
12. Reconnect the FPCs.
13. Supply the electric power to the module and then check the waveform of the board.
14. Turn "OFF" the power after the waveform is adjusted.

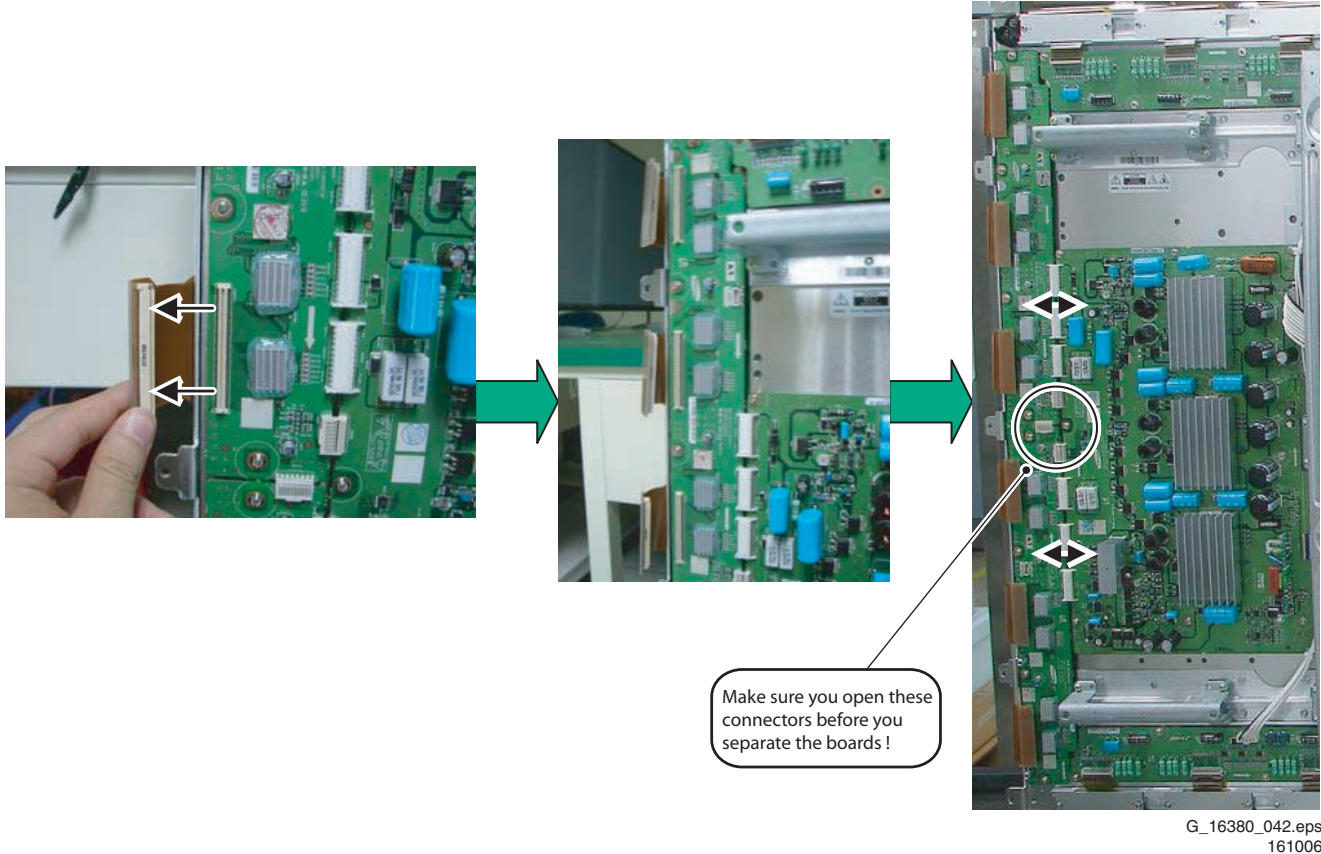


Figure 4-25 Photo 1: Dis-assembly of YBU, YBL, and YM - 63" HD v4

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

- 5.1 Repair Tools
 - 5.1.1 ComPair
 - 5.1.2 Other Service Tools
- 5.2 Fault Finding
 - 5.2.1 Possible Scenarios
 - 5.2.2 Faulty Power Supply
 - 5.2.3 No Display
 - 5.2.4 Abnormal display
 - 5.2.5 Horizontal line or block open
 - 5.2.6 Address open
 - 5.2.7 Address short
 - 5.2.8 Criteria for Panel Replacement, due to Defective Panel Cells
 - 5.2.9 Overview
- 5.3 Defect Description Form

5.1 Repair Tools

5.1.1 ComPair

For the v5 and w1 models, it will be possible to generate test patterns with ComPair. The ComPair interface must be connected to the Logic Board with the special interconnection cable (see table below for the order code).

5.1.2 Other Service Tools

Table 5-1 Overview Service tools

Service Tools	Order Code
ComPair / SDI interconnection cable	3122 785 90800
Foam buffers (2 pcs.)	3122 785 90581

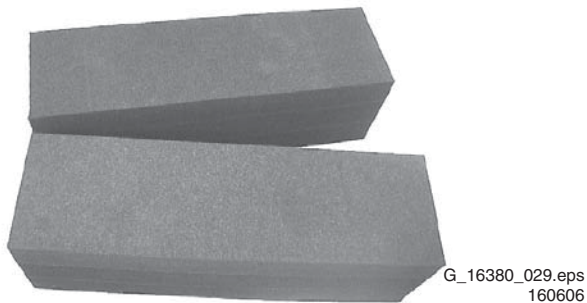


Figure 5-1 Foam buffers

5.2 Fault Finding

5.2.1 Possible Scenarios

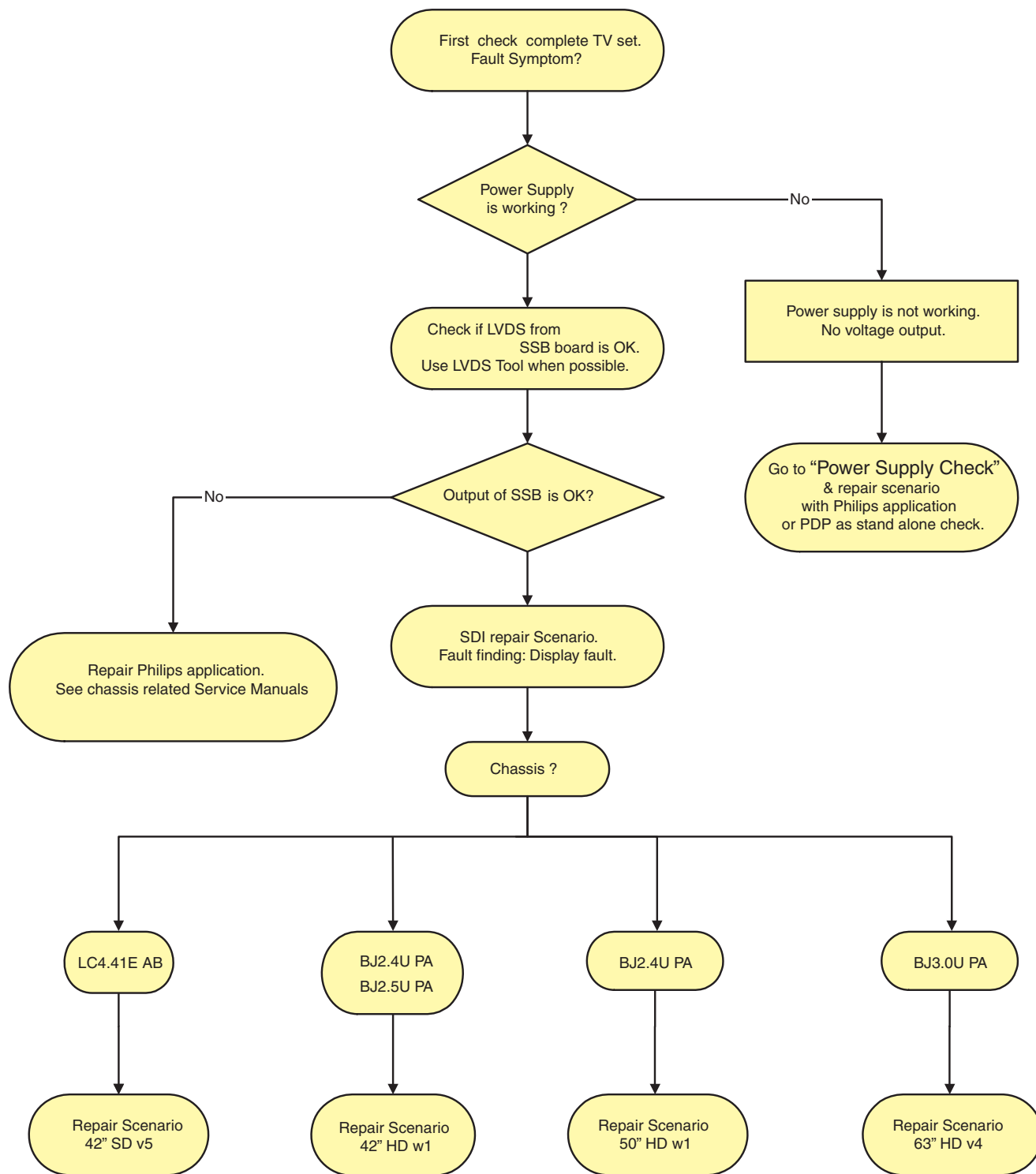


Figure 5-2 Which repair scenario?

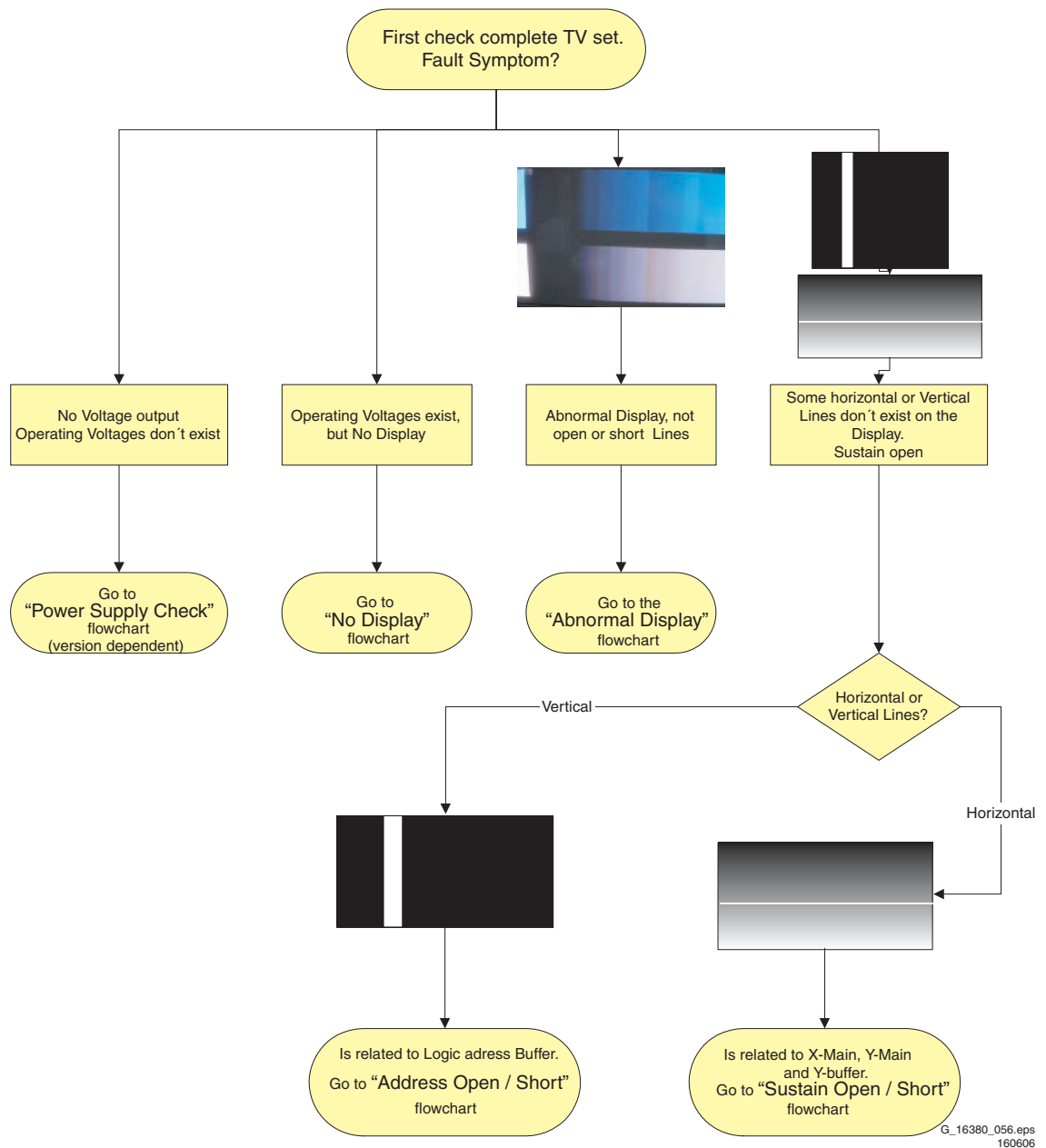


Figure 5-3 Fault symptom overview (complete TV set)

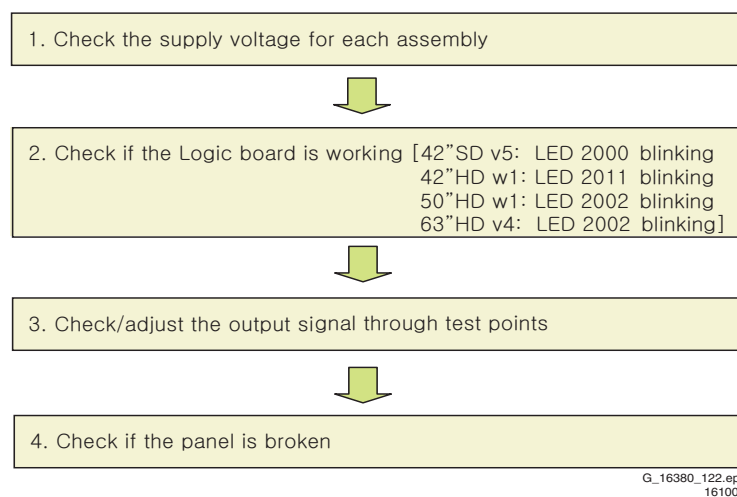


Figure 5-4 Repair scenario stand alone panels

5.2.2 Faulty Power Supply

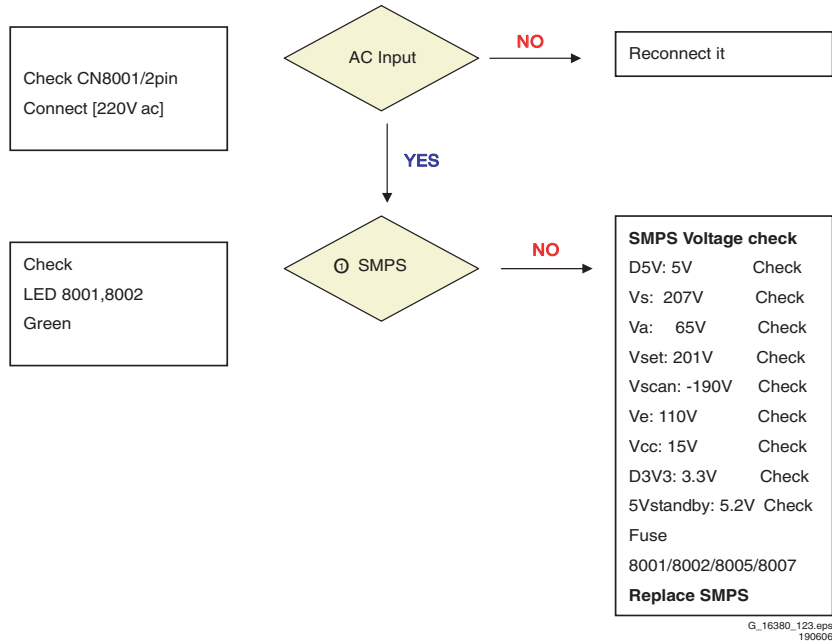


Figure 5-5 Power Supply Check for 42" SD v5 models 1/2

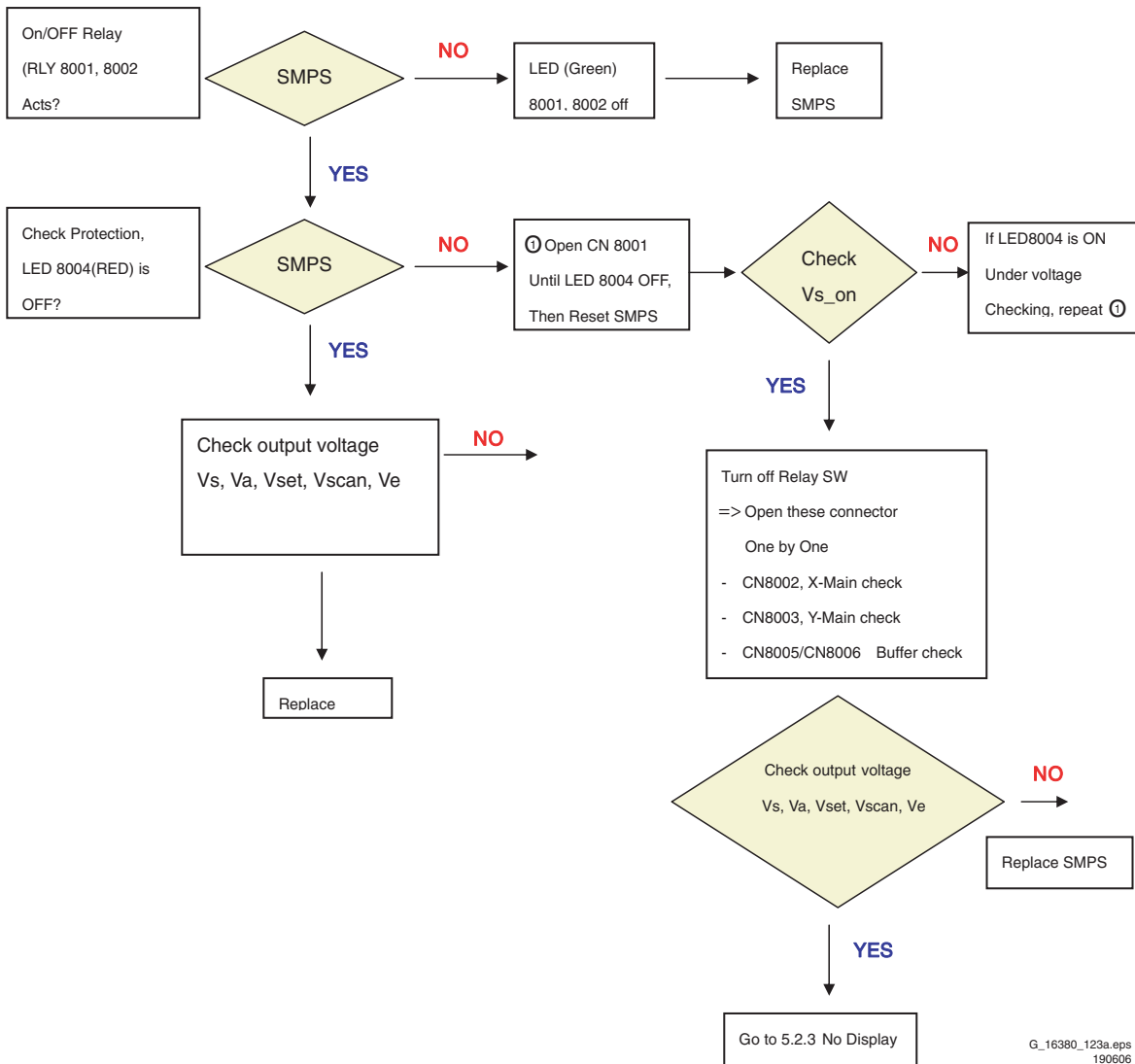


Figure 5-6 Power Supply Check for 42" SD v5 models 2/2

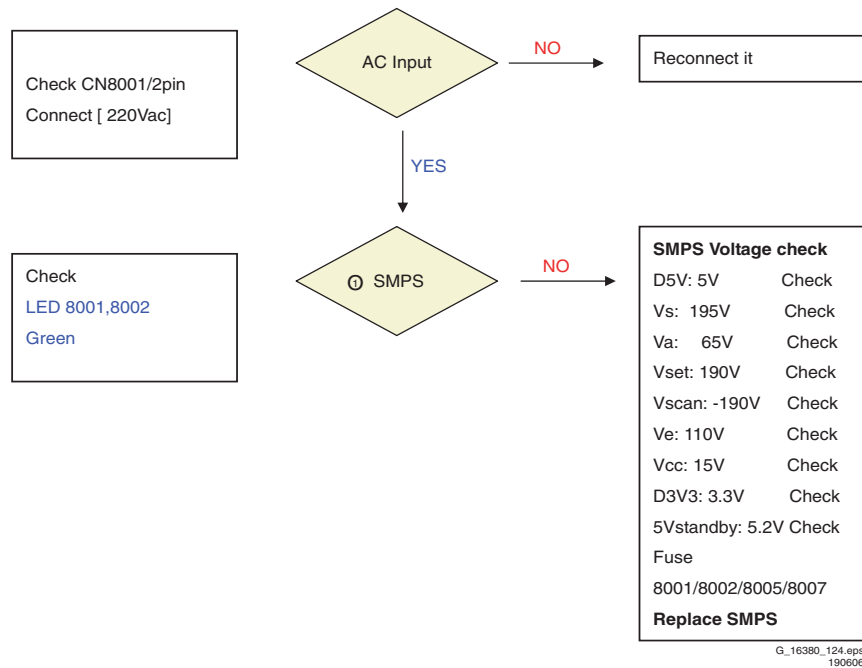


Figure 5-7 Power Supply Check for 42" HD w1 models 1/2

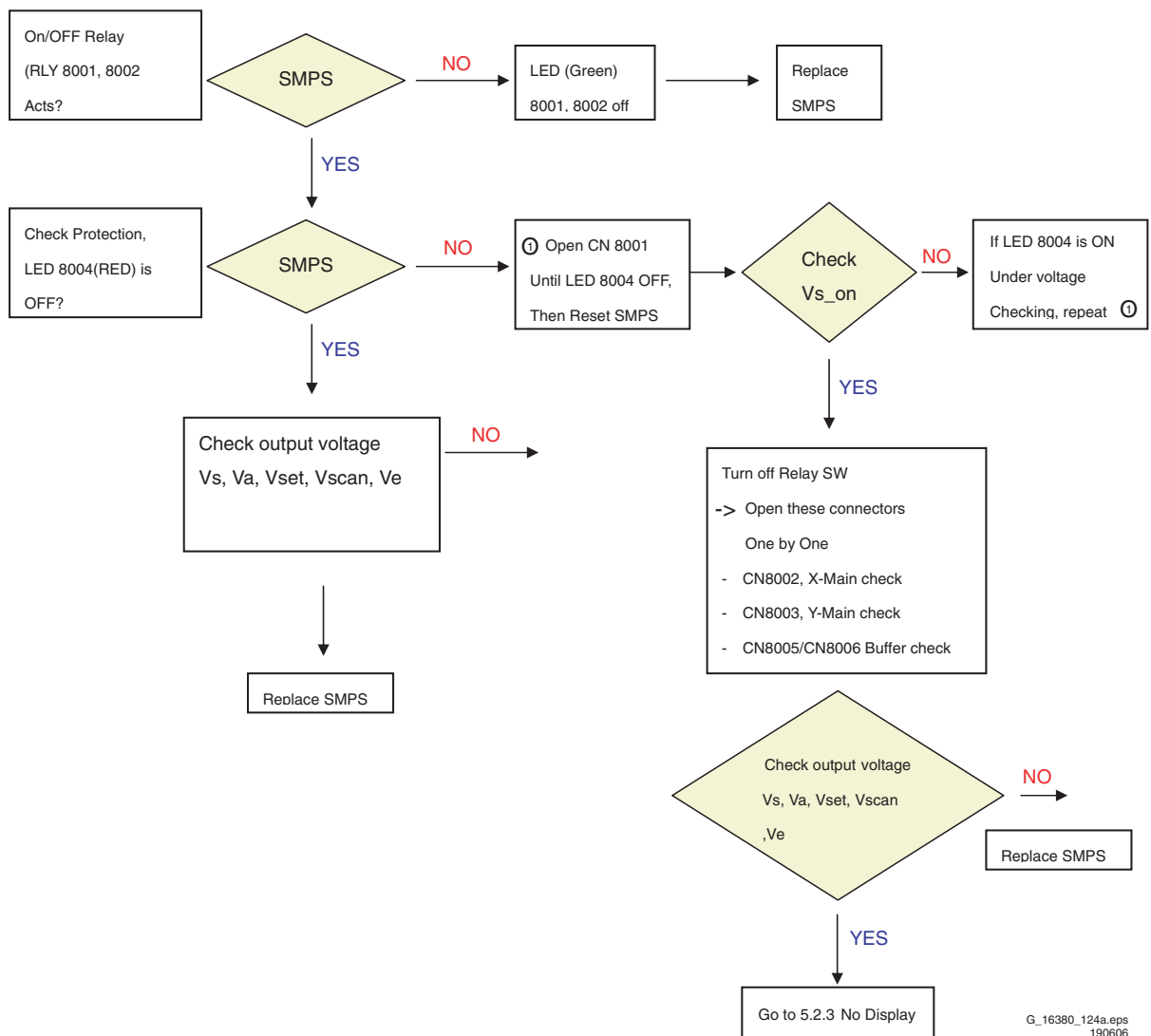


Figure 5-8 Power Supply Check for 42" HD w1 models 2/2

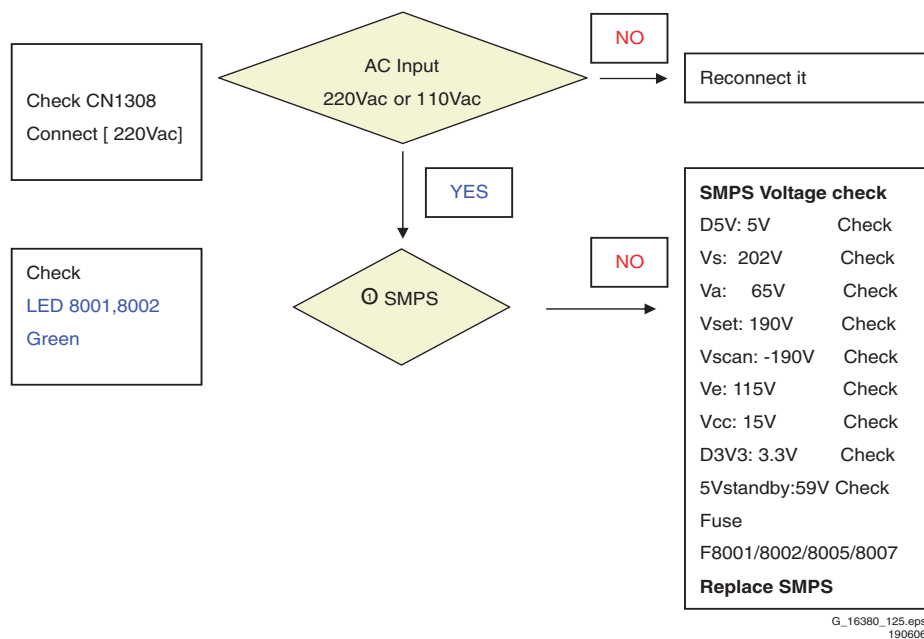


Figure 5-9 Power Supply Check for 50" HD w1 models 1/2

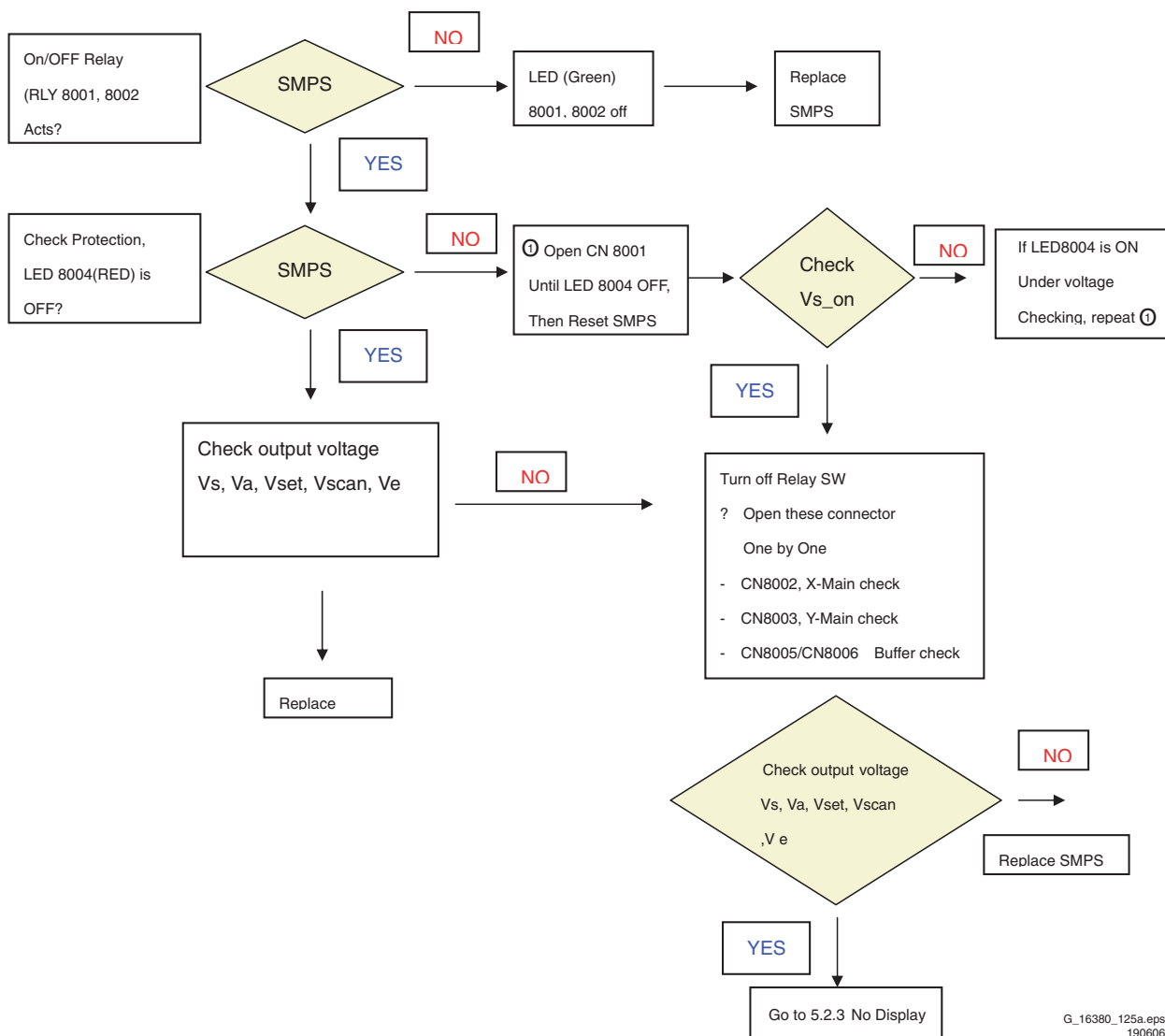


Figure 5-10 Power Supply Check for 50" HD w1 models 2/2

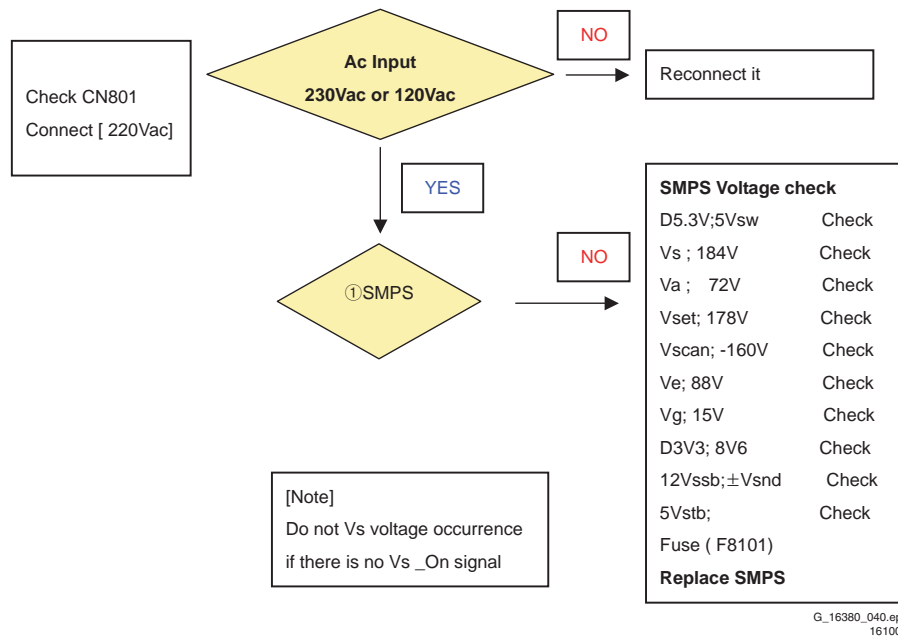


Figure 5-11 Power Supply Check for 63" HD v4 models 1/2

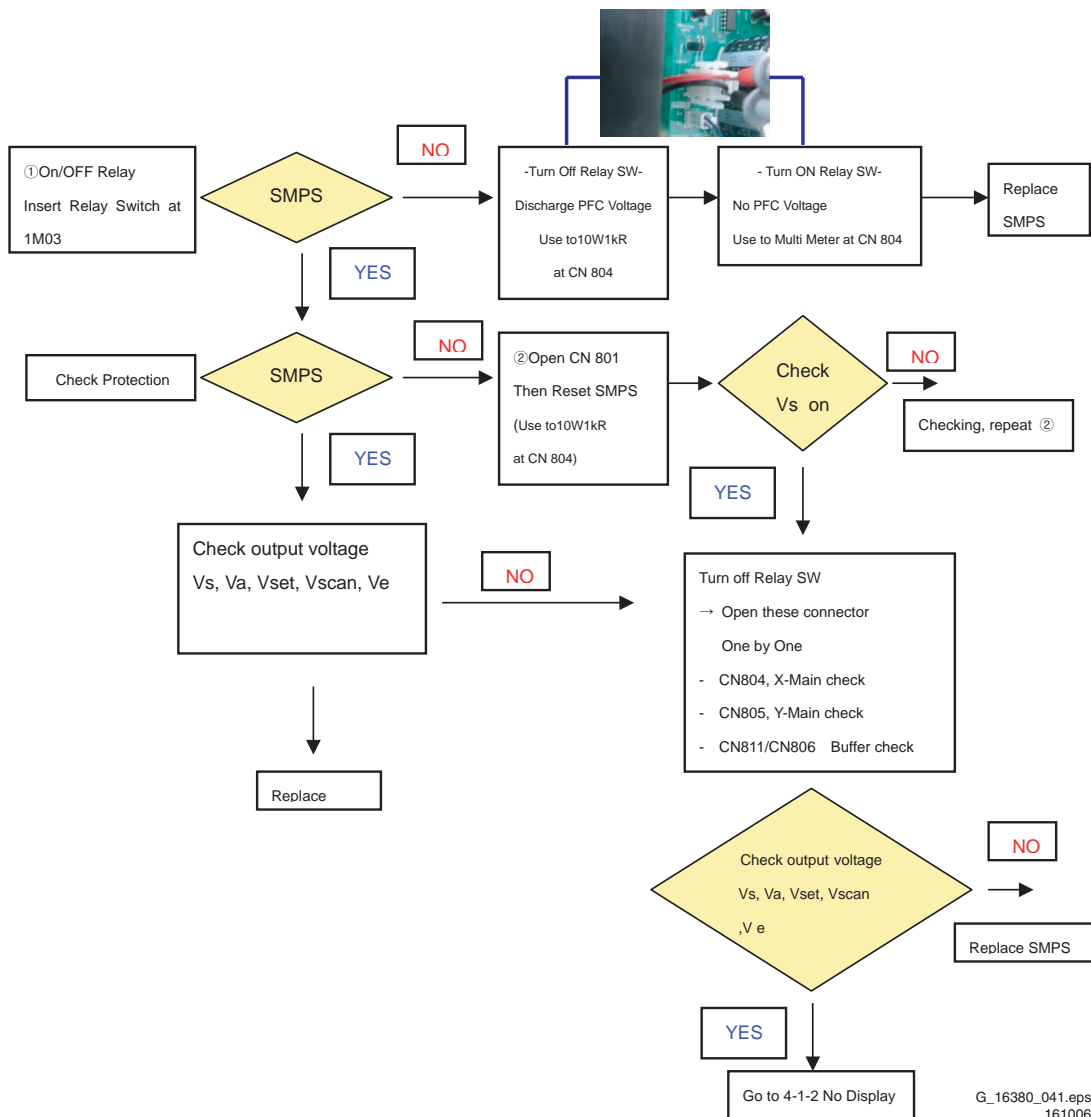


Figure 5-12 Power Supply Check for 63" HD v4 models 2/2

5.2.3 No Display

(operating voltage present, but an image doesn't exist on Screen)

No Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.

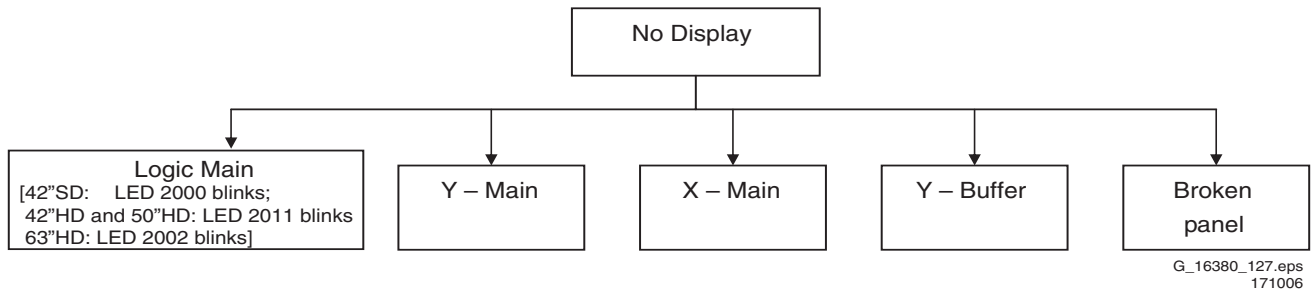


Figure 5-13 Fault symptom: "No Display", general guide line

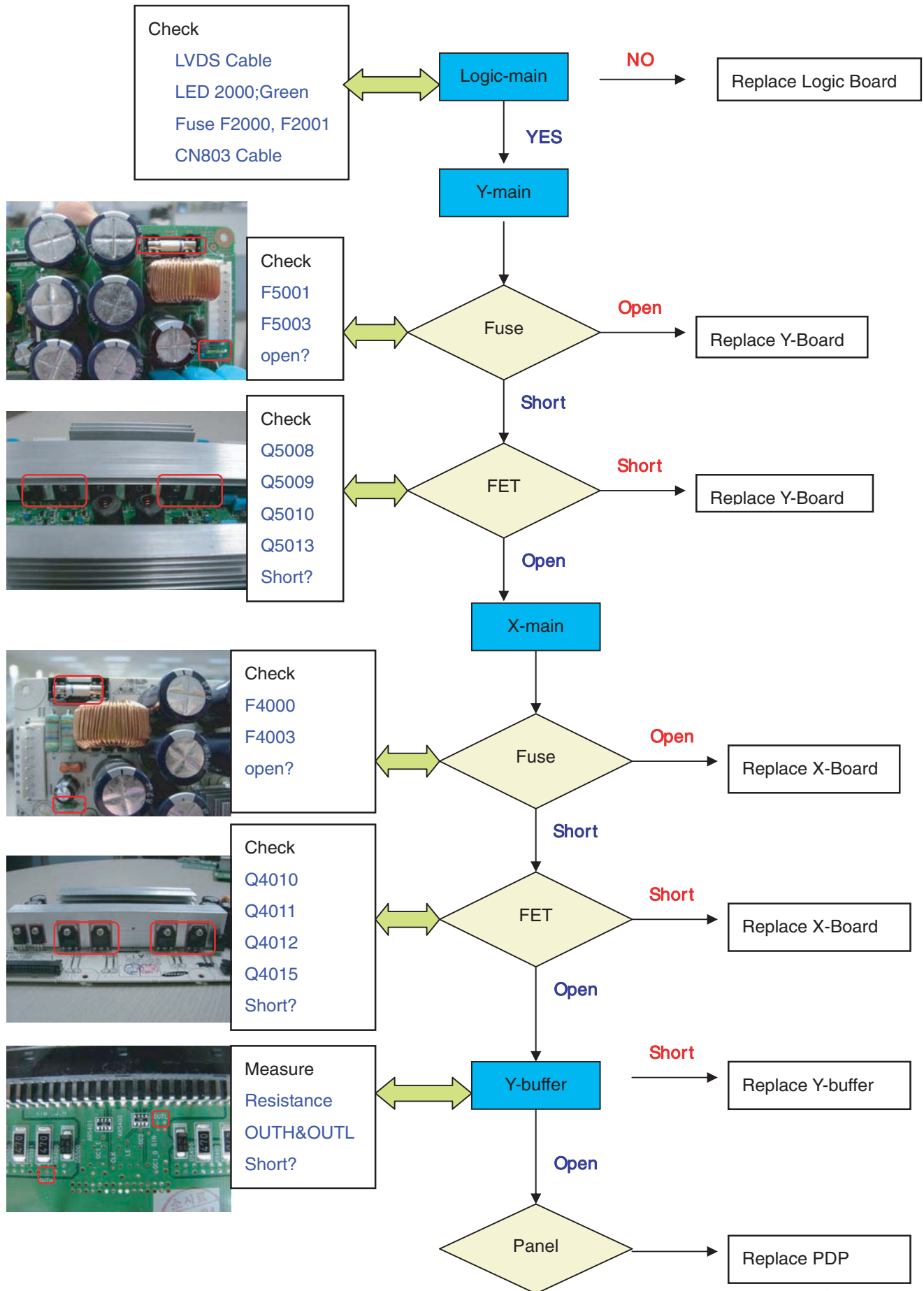


Figure 5-14 Fault symptom: "No Display", 42" SD v5

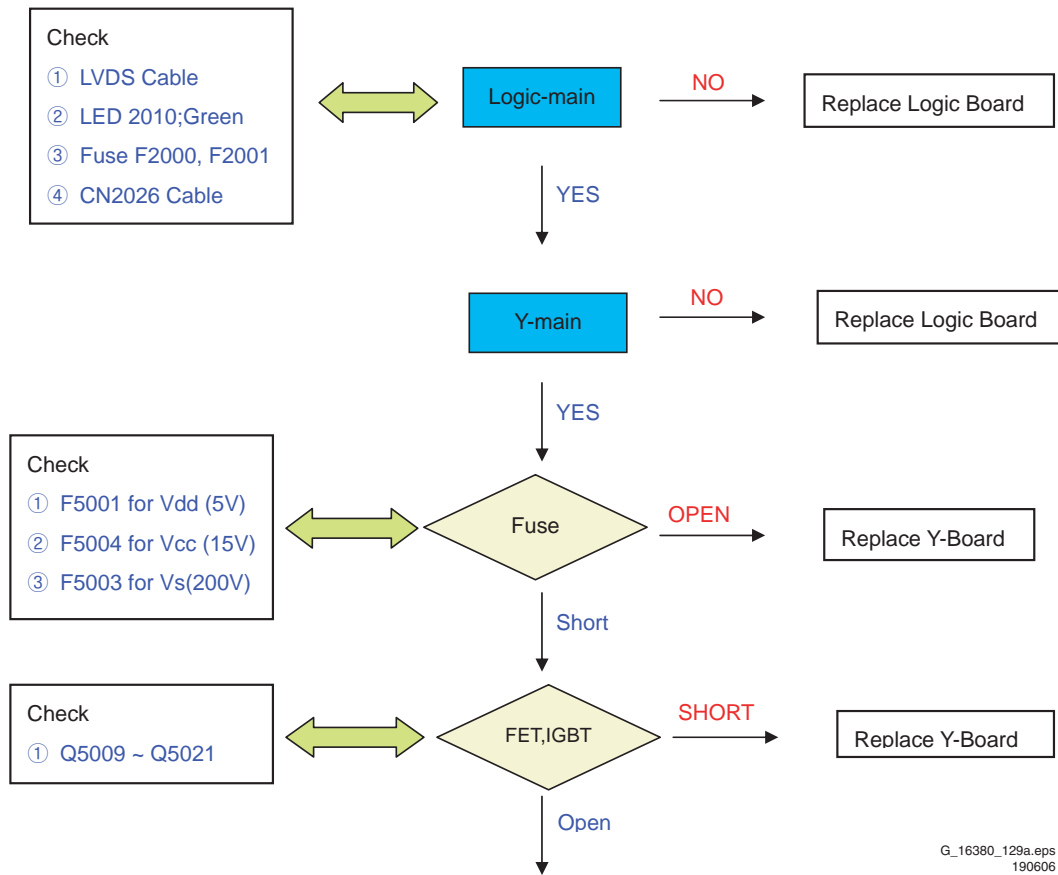


Figure 5-15 Fault symptom: "No Display", 42" HD w1 1/7

Y-main Check Point


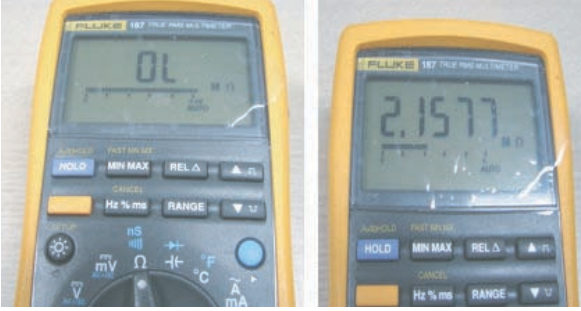
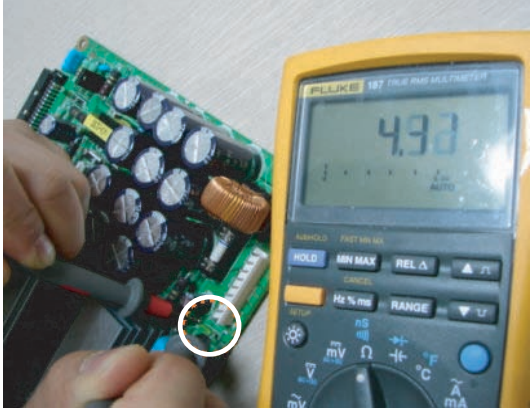
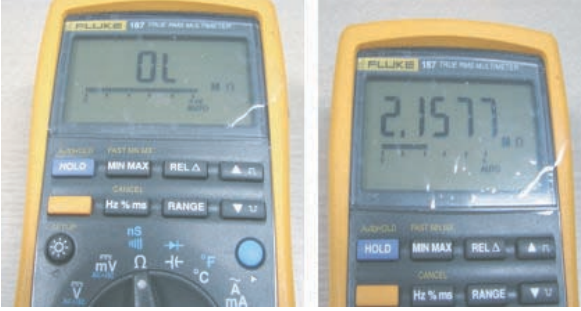
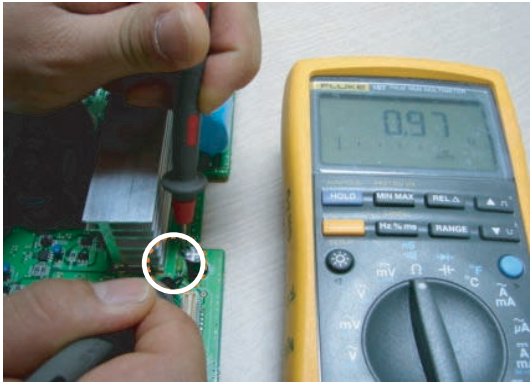
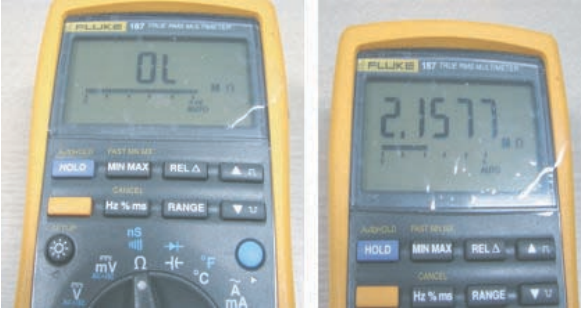

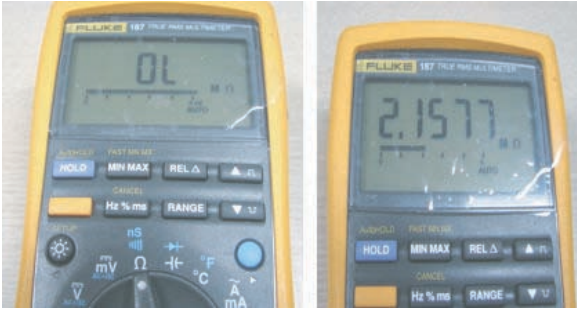
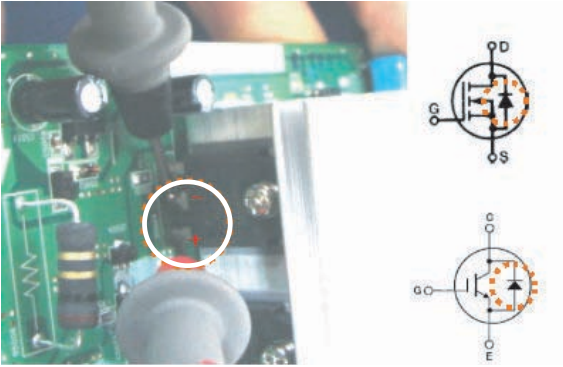

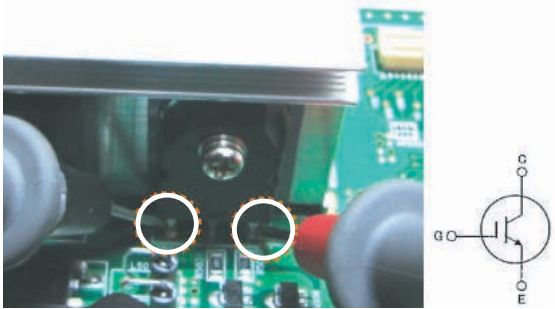

	<p>OR</p> 
<p>Vs fuse (F5003) – OK (0.x ~ x.x ohm)</p>	<p>Vs fuse (F5003) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>15V fuse (F5004) – OK (0.x ~ x.x ohm)</p>	<p>15V fuse (F5004) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>5V fuse (F5001) – OK (0.x ~ x.x ohm)</p>	<p>5V fuse (F5001) – OPEN (x.x Mohm)</p>

Figure 5-16 Fault symptom: “No Display”, 42” HD w1 2/7

	<p>OR</p> 
<p>Vscan fuse (F5006) – OK (0.x ~ x.x ohm)</p>	<p>Vscan fuse (F5006) – OPEN (x.x Mohm)</p>

IGBT, FET Check Point

	 <p>OK Short</p>
<p>FET,IGBT (contain the inner diode) [Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xe)</p>	<p>OK (0.3 ~ 0.9 V) / Short (0.000 ~ 0.00x V)</p>
	 <p>OK Short</p>
<p>IGBT (do not contain the inner diode) (Yr, Yf, Xr, Xf)</p>	<p>OK (xx.x kohm) / Short (x.x ohm)</p>

Ys(Q5013,14), Yg(Q5009,10), Ypn(Q5016,17,18), Yscan(Q5020,21), Yfr(Q5019), Yrr(Q5015),
Xs(Q4002,03), Xg(Q4011,12), Xe(Q4013,14)
Yr(Q5011), Yf(Q5012), Xr(Q4016), Xf(Q4015)

Figure 5-17 Fault symptom: “No Display”, 42” HD w1 3/7

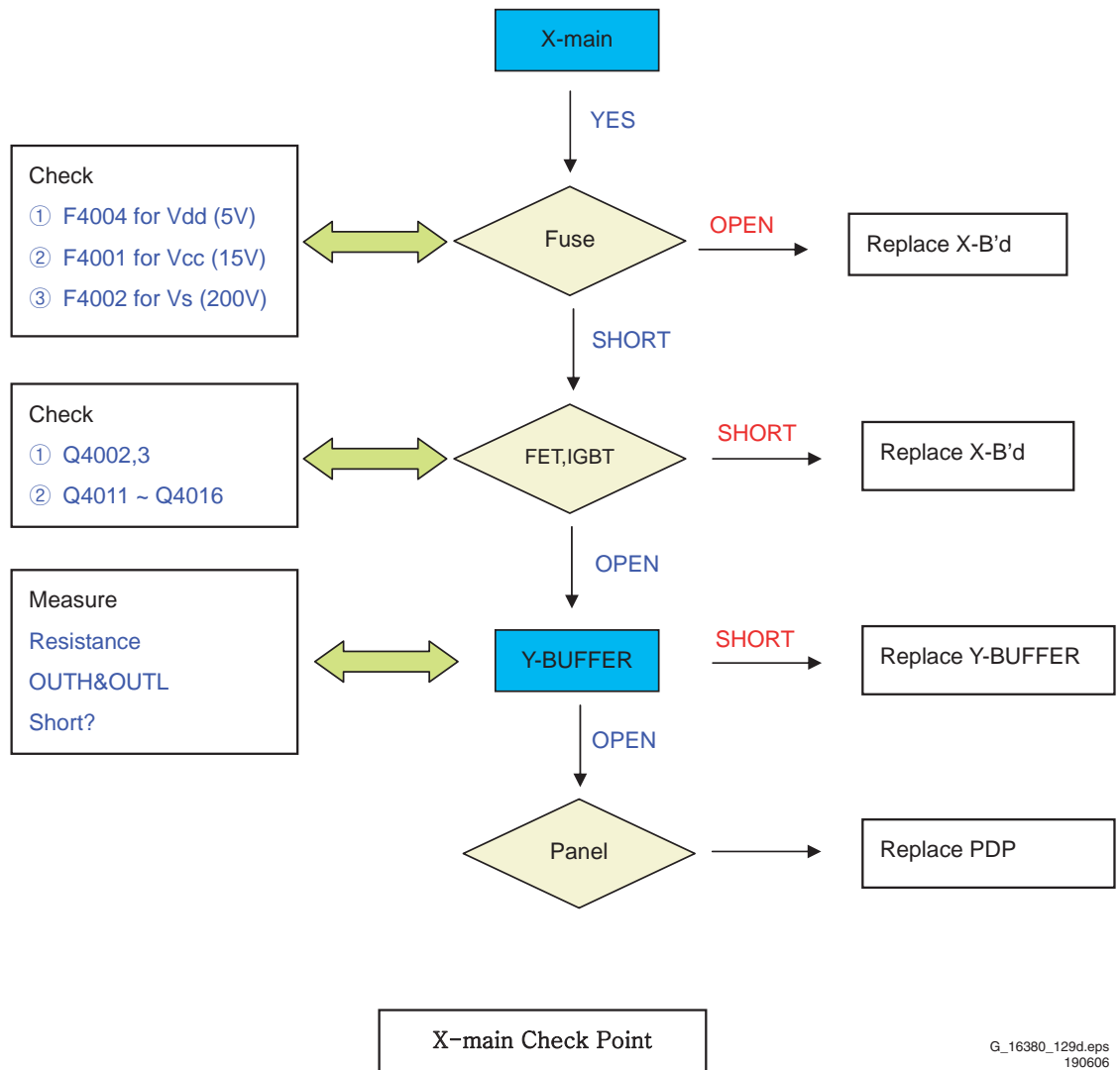


Figure 5-18 Fault symptom: "No Display", 42" HD w1 4/7

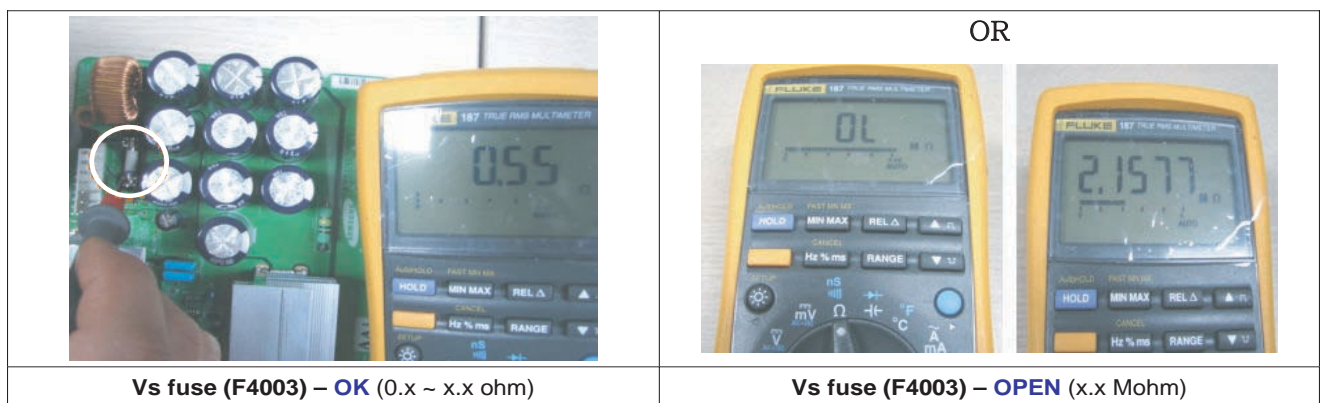
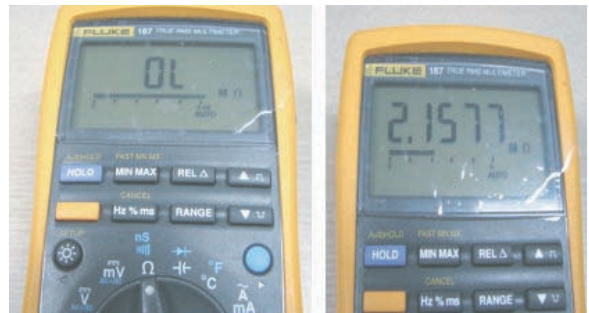


Figure 5-19 Fault symptom: "No Display", 42" HD w1 5/7

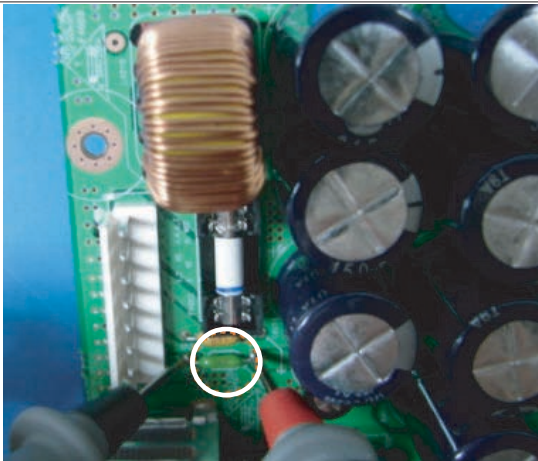


Ve fuse (F4005) – OK (0.x ~ x.x ohm)

OR

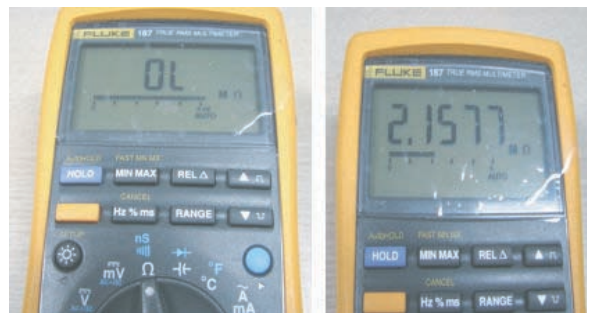


Vs fuse (F4005) – OPEN (x.x Mohm)

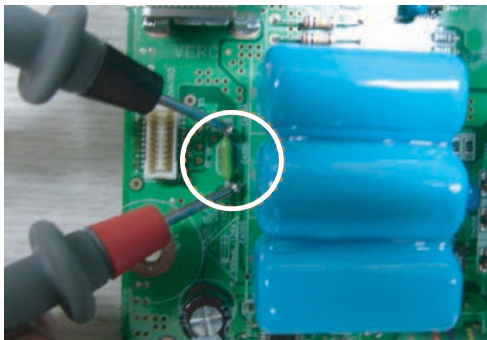


15V fuse (F4001) – OK (0.x ~ x.x ohm)

OR

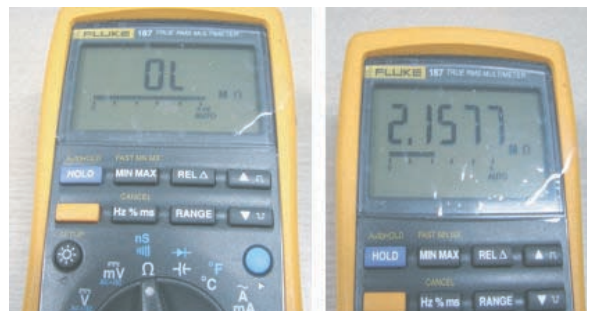


Vs fuse (F4001) – OPEN (x.x Mohm)



5V fuse (F4004) – OK (0.x ~ x.x ohm)

OR



5V fuse (F4004) – OPEN (x.x Mohm)

Figure 5-20 Fault symptom: “No Display”, 42” HD w1 6/7

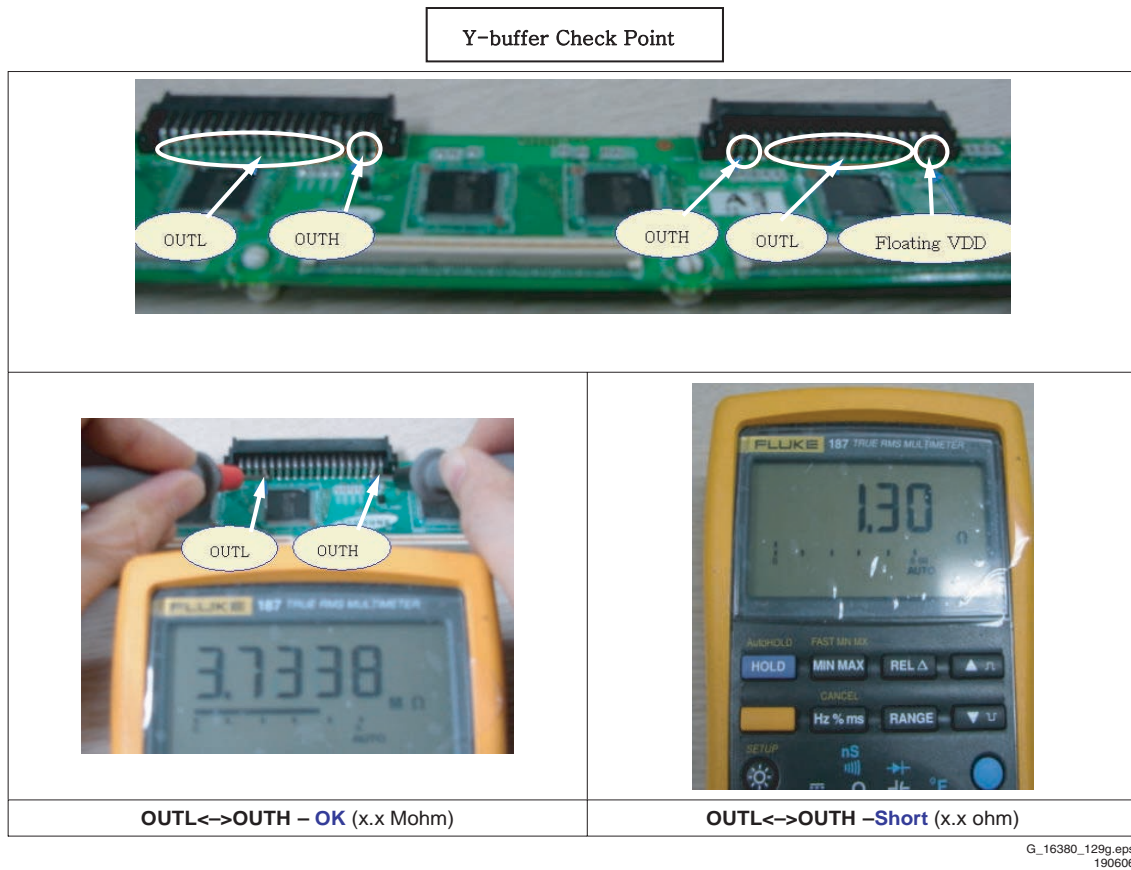


Figure 5-21 Fault symptom: “No Display”, 42” HD w1 7/7

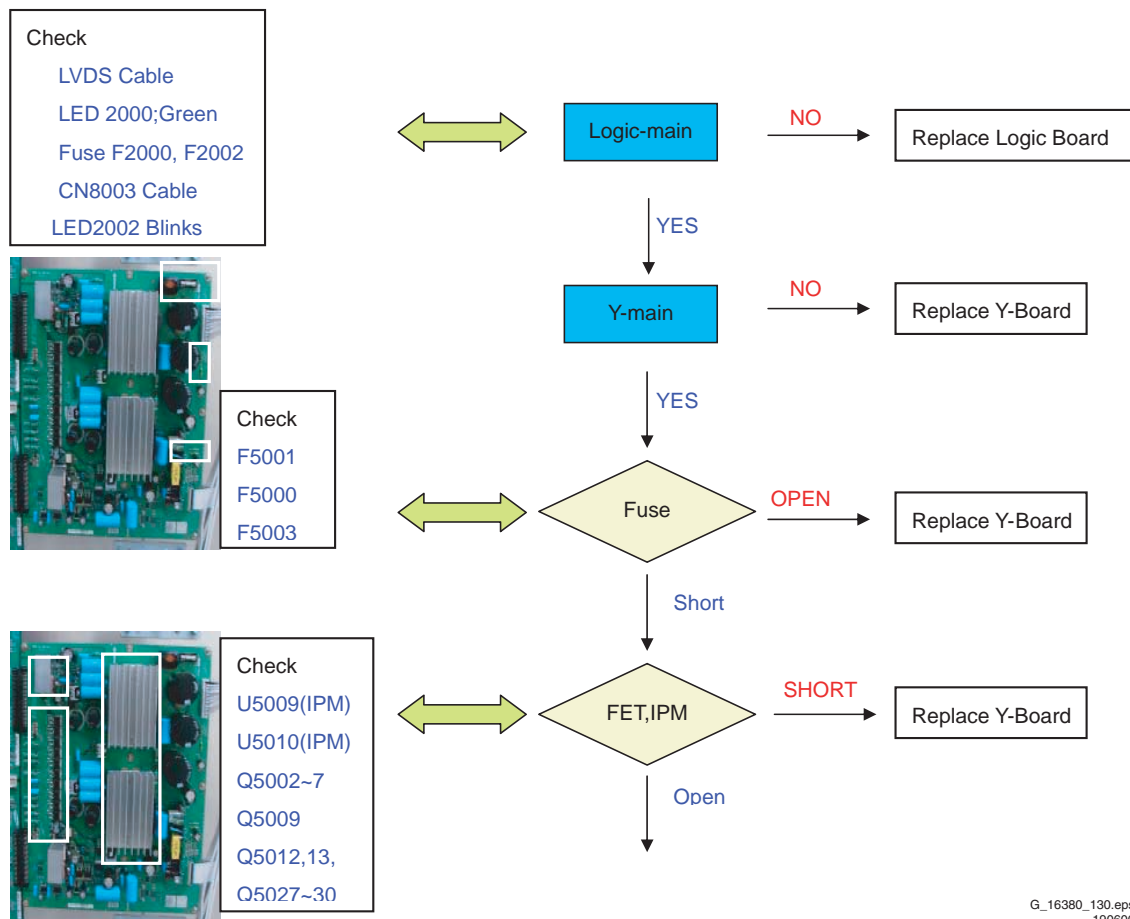

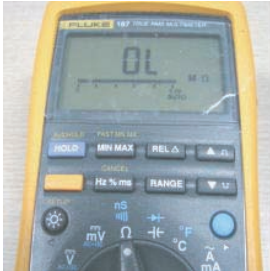









Figure 5-22 Fault symptom: “No Display”, 50” HD w1 1/6


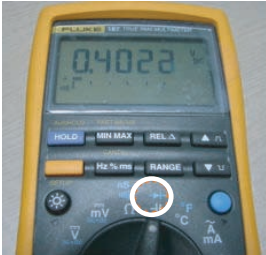

Y- main Check Point

	OR		
Vs fuse (F5003) – OK (0.x ~ x.x ohm)		Vs fuse (F5003) – OPEN (x.x Mohm)	
	OR		
15V fuse (F5000) – OK (0.x ~ x.x ohm)		15V fuse (F5000) – OPEN (x.x Mohm)	
	OR		
5V fuse (F5001) – OK (0.x ~ x.x ohm)		5V fuse (F5001) – OPEN (x.x Mohm)	

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Figure 5-23 Fault symptom: “No Display”, 50” HD w1 2/6

IGBT, FET Check Point

		
FET [Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xe)	OK	Short
	OK (0.3 ~ 0.9 V)	Short (0.000 ~ 0.00x V)

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Figure 5-24 Fault symptom: “No Display”, 50” HD w1 3/6

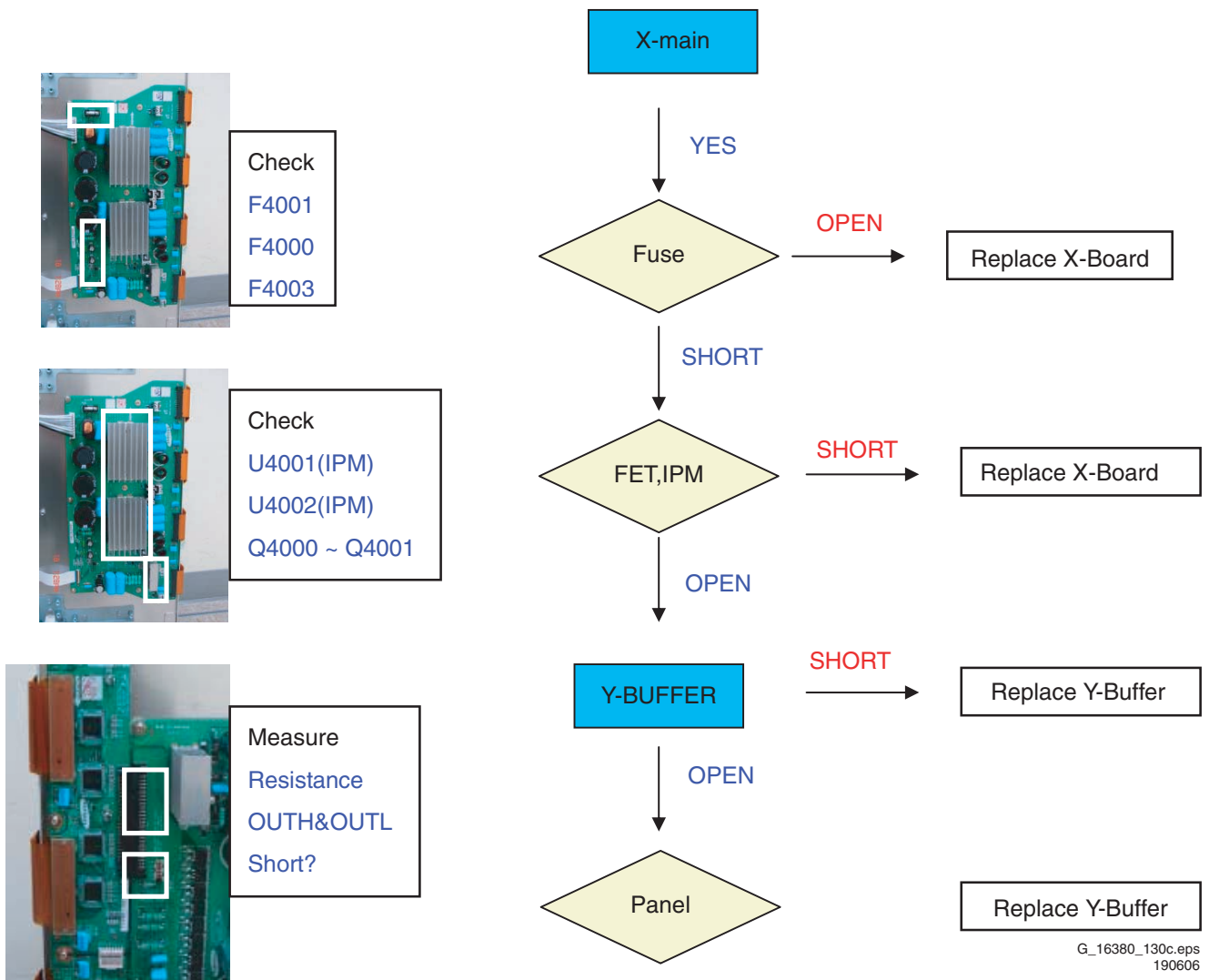


Figure 5-25 Fault symptom: "No Display", 50" HD w1 4/6

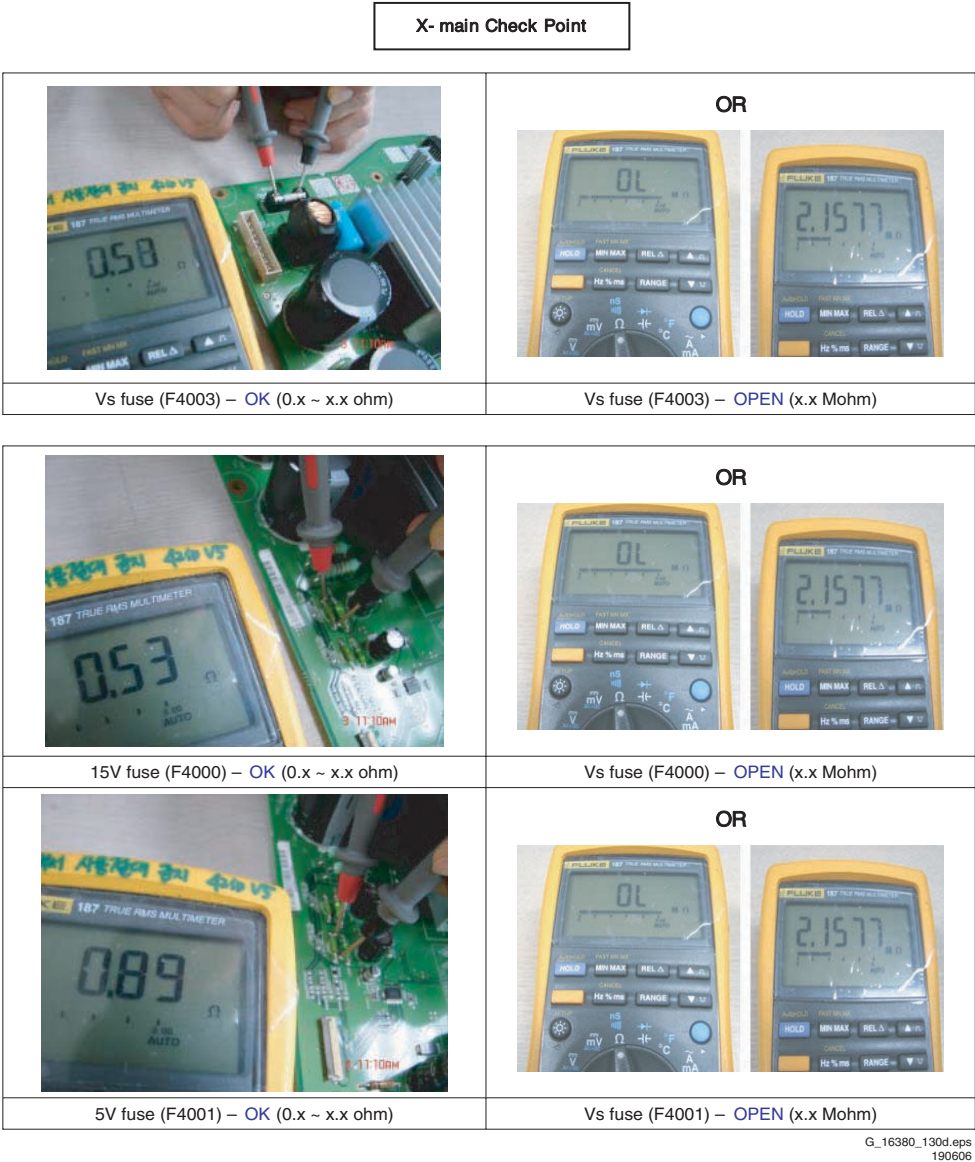


Figure 5-26 Fault symptom: “No Display”, 50” HD w1 5/6

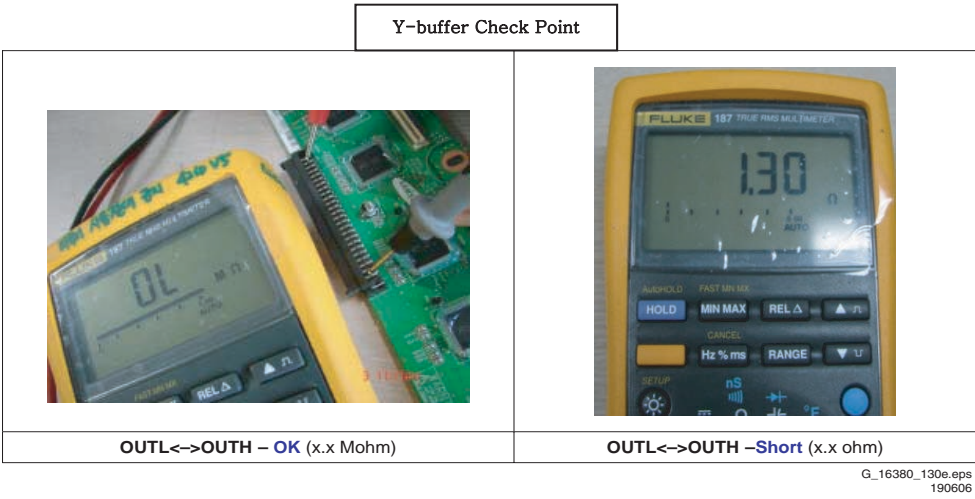


Figure 5-27 Fault symptom: “No Display”, 50” HD w1 6/6

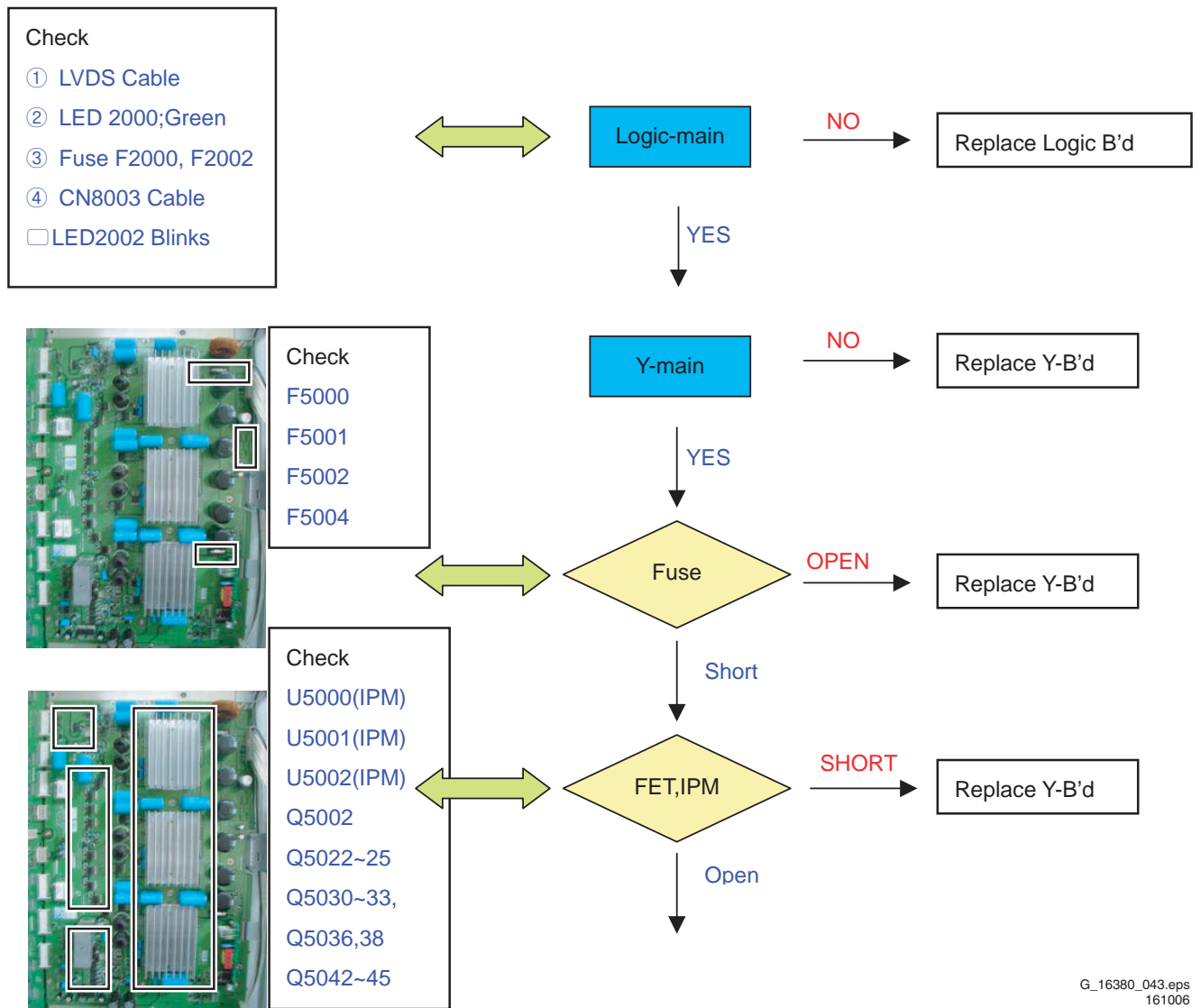
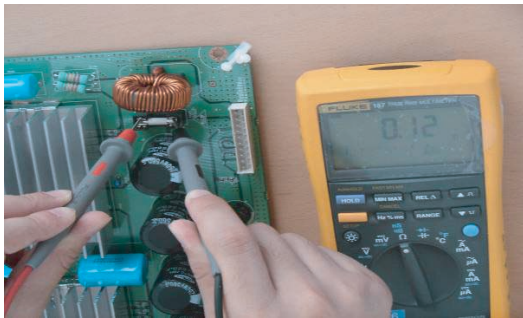


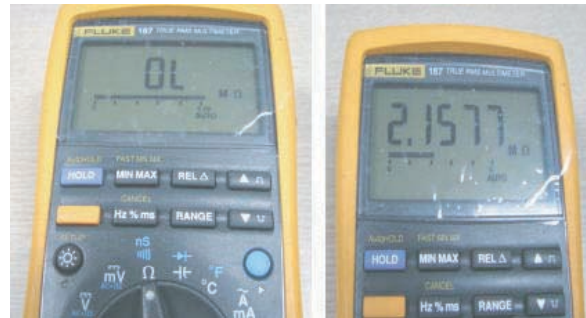
Figure 5-28 Fault symptom: "No Display", 63" HD v4 1/6

Y-main Check Point

OR

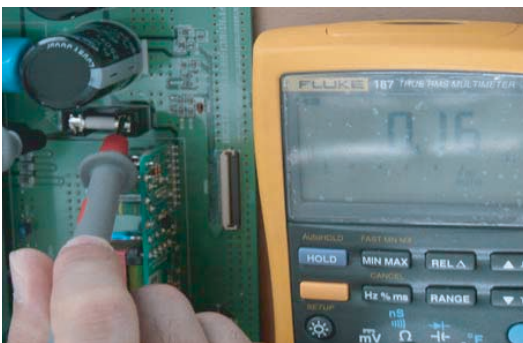


Vs fuse (F5002) – OK (0.x ~ x.x ohm)



Vs fuse (F5002) – OPEN (x.x Mohm)

OR

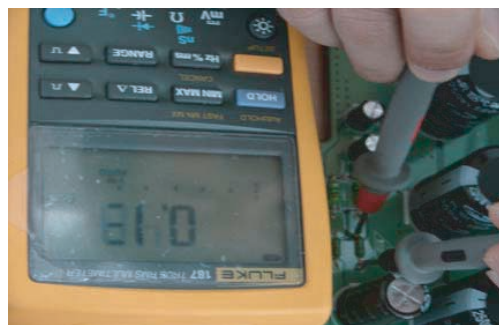


Vs fuse (F5004) – OK (0.x ~ x.x ohm)



Vs fuse (F5004) – OPEN (x.x Mohm)

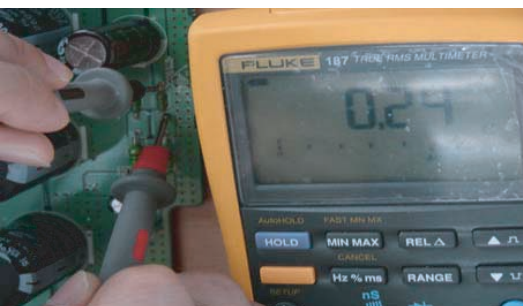
OR



15V fuse (F5001) – OK (0.x ~ x.x ohm)



15V fuse (F5001) – OPEN (x.x Mohm)



5V fuse (F5000) – OK (0.x ~ x.x ohm)




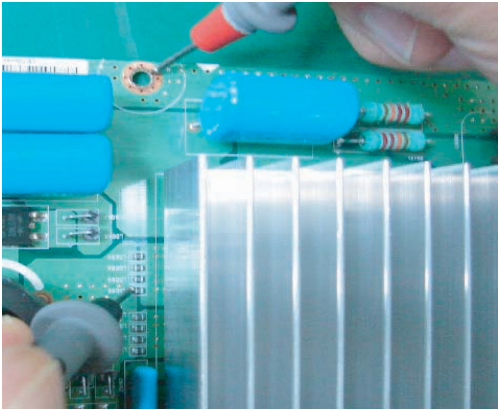
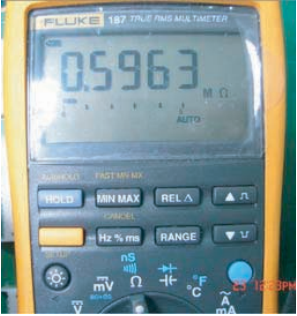



5V fuse (F5000) – OPEN (x.x Mohm)

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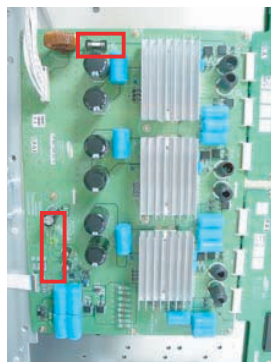
Figure 5-29 Fault symptom: “No Display”, 63” HD v4 2/6

FET,IPM Check Point

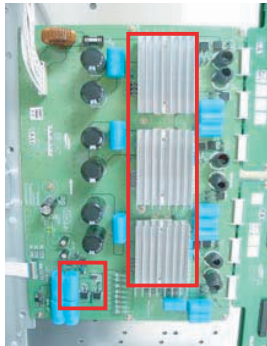
	 
FET [Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xe)	OK Short
	OK (0.3 ~ 0.9 V) / Short (0.000 ~ 0.00x V)
	 
IPM	OK Short
	OK (X.X Mohm) / Short (0.000 ~ 0.00x ohm)

G_16380_045.eps
161006

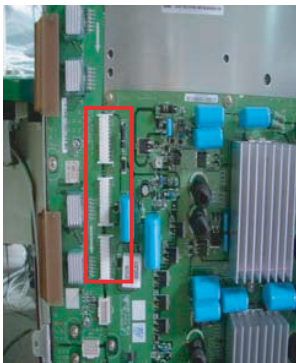
Figure 5-30 Fault symptom: “No Display”, 63” HD v4 3/6



Check
F4000
F4001
F4003



Check
U4003(IPM)
U4005(IPM)
U4006(IPM)
Q4002, Q4003



Measure
Resistance
OUTH&OUTL
Short?

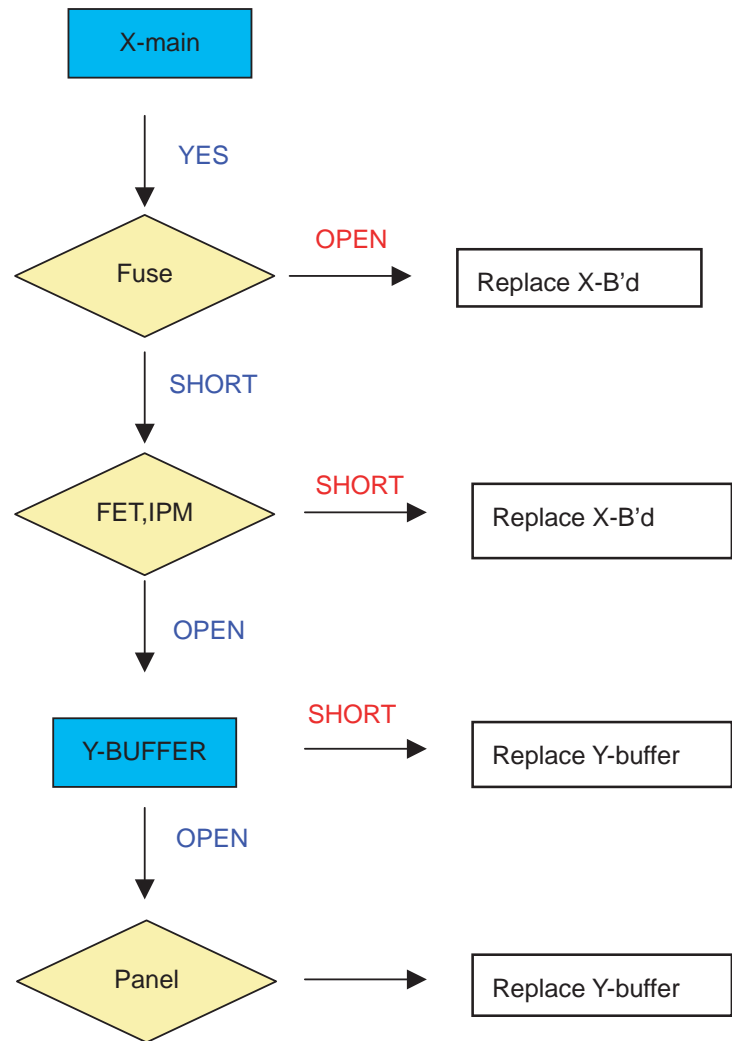



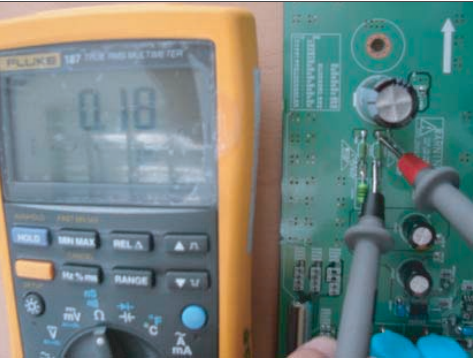


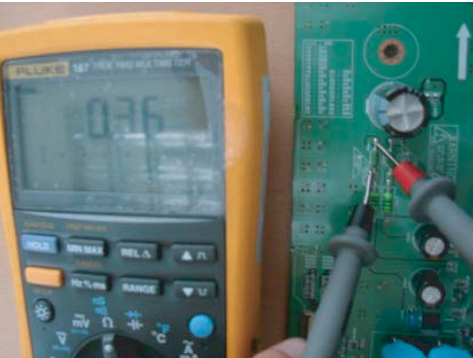




Figure 5-31 Fault symptom: "No Display", 63" HD v4 4/6

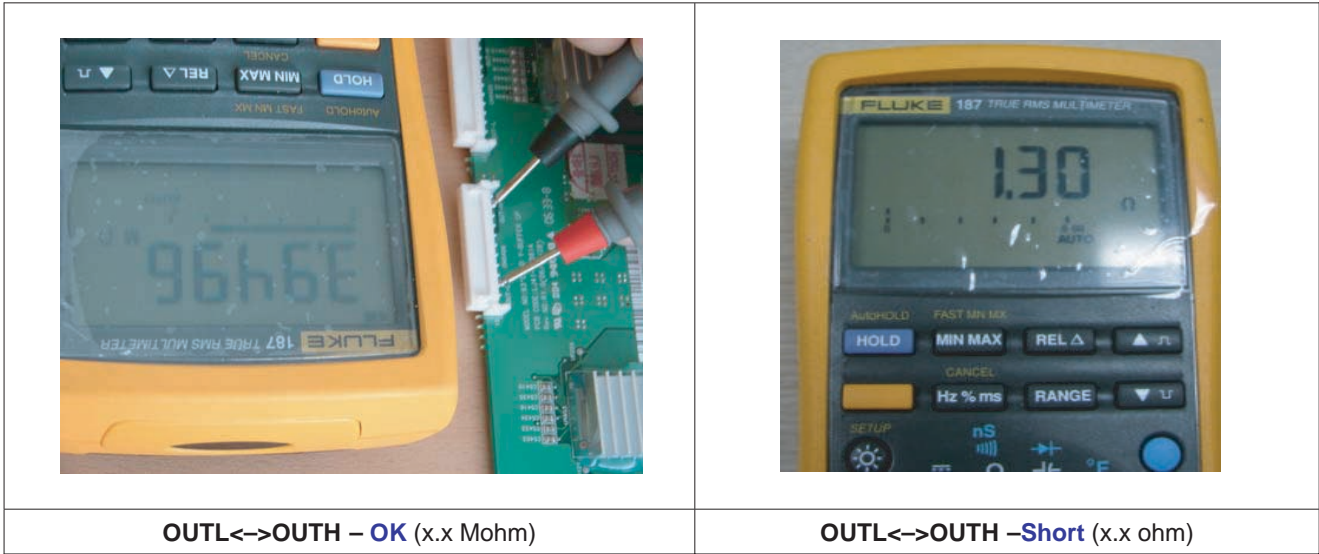
X-main Check Point

	OR  
Vs fuse (F4003) – OK (0.x ~ x.x ohm)	Vs fuse (F4003) – OPEN (x.x Mohm)
	OR  
15V fuse (F4001) – OK (0.x ~ x.x ohm)	15V fuse (F4001) – OPEN (x.x Mohm)
	OR  
5V fuse (F4000) – OK (0.x ~ x.x ohm)	Vs fuse (F4000) – OPEN (x.x Mohm)

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Figure 5-32 Fault symptom: “No Display”, 63” HD v4 5/6

Y-buffer Check Point



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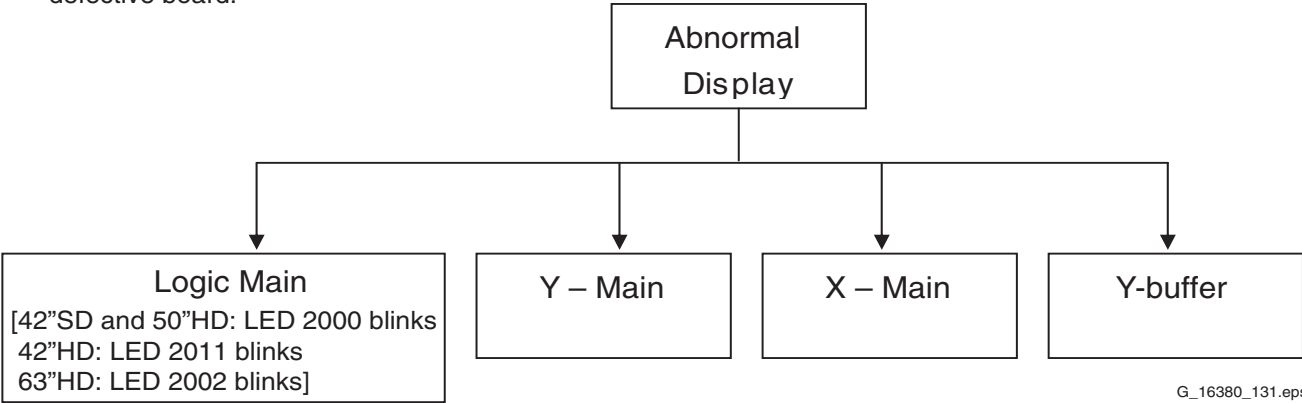
Figure 5-33 Fault symptom: “No Display”, 63” HD v4 6/6

5.2.4 Abnormal display

(Abnormal Image is on Screen (except abnormality in Sustain or Address))

-> Abnormal Display is related with Y-MAIN, X-MAIN, Logic Main, Y-buffer and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.



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Figure 5-34 Fault symptom: “Abnormal Display”, general guide line

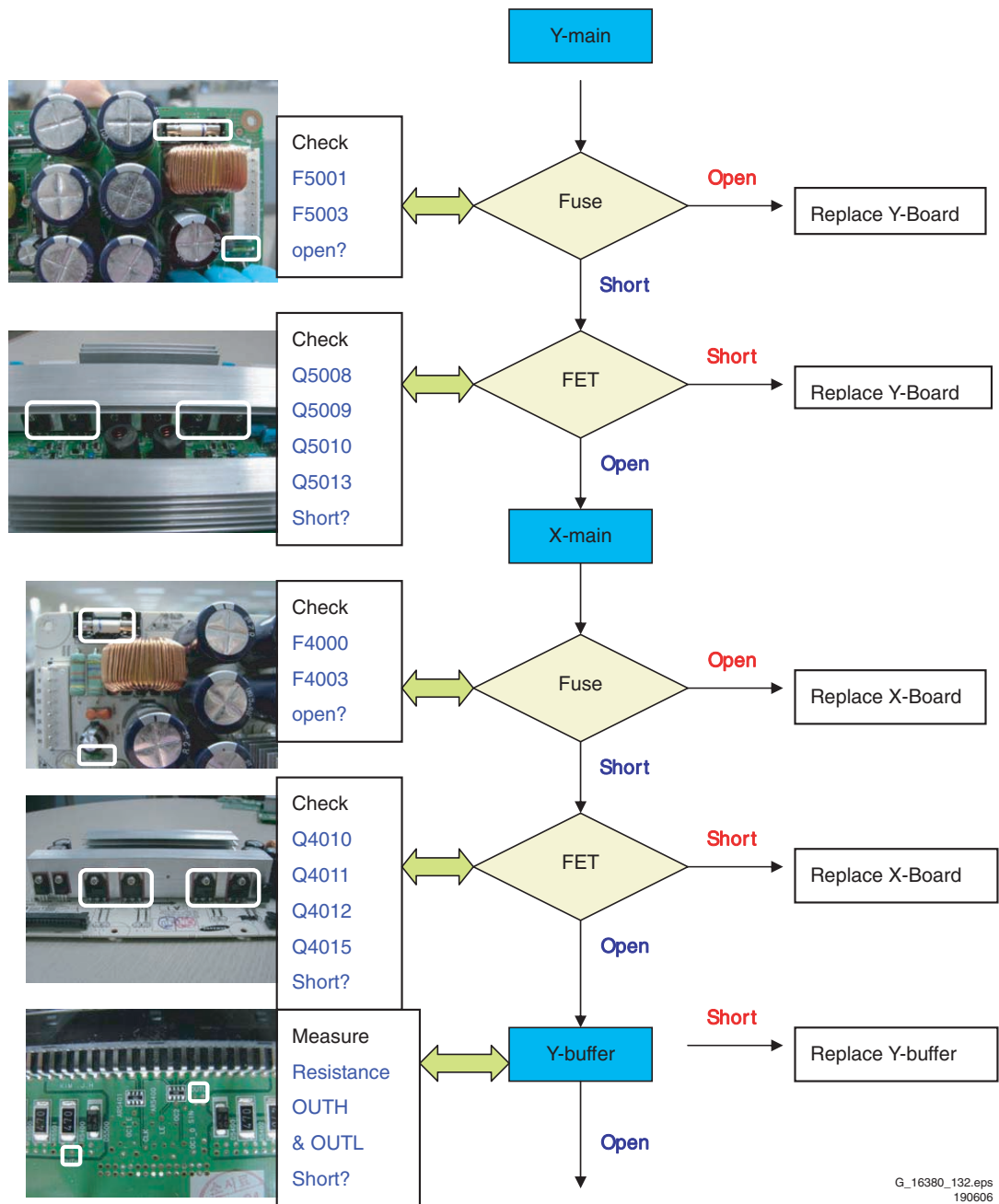


Figure 5-35 Fault symptom: "Abnormal Display" 42" SD v5 1/2

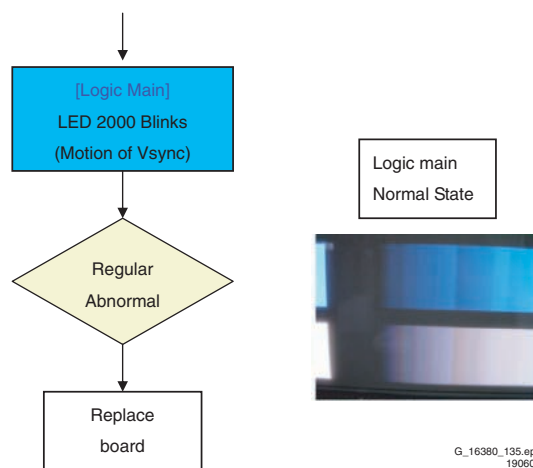


Figure 5-36 Fault symptom: "Abnormal Display" 42" SD v5 2/2

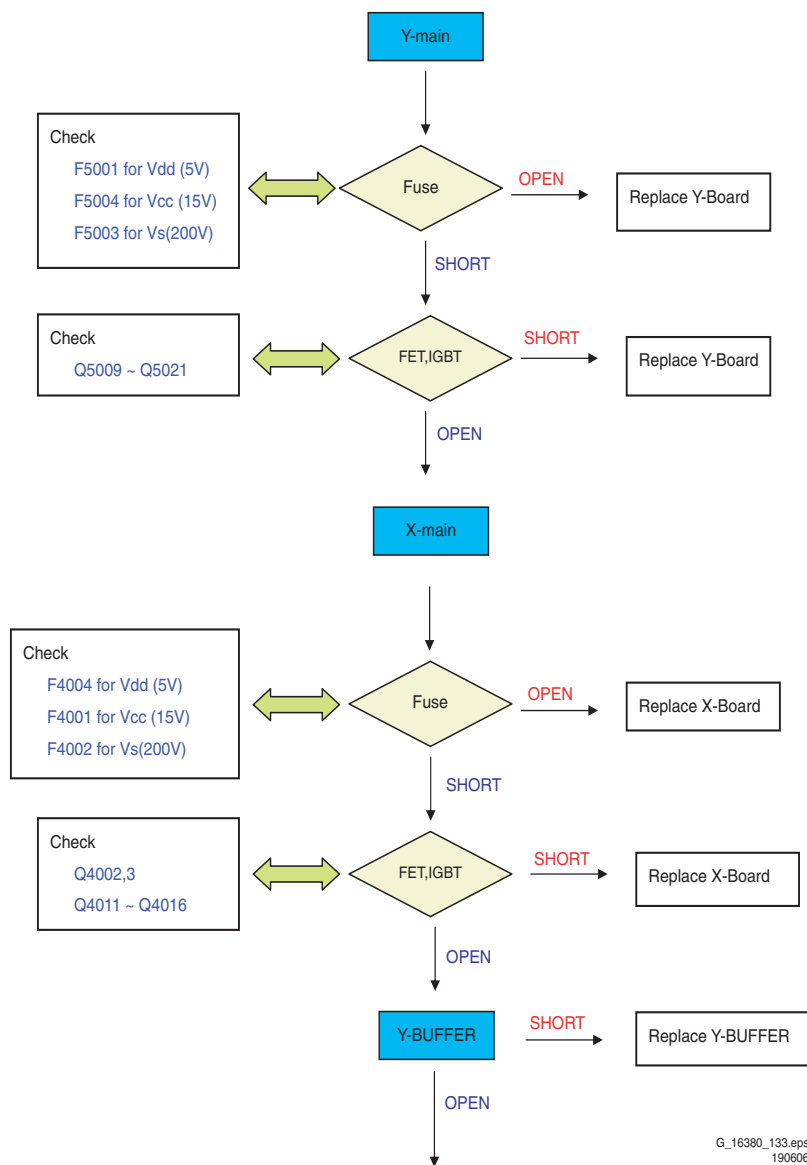


Figure 5-37 Fault symptom: “Abnormal Display” 42” HD w1 1/2

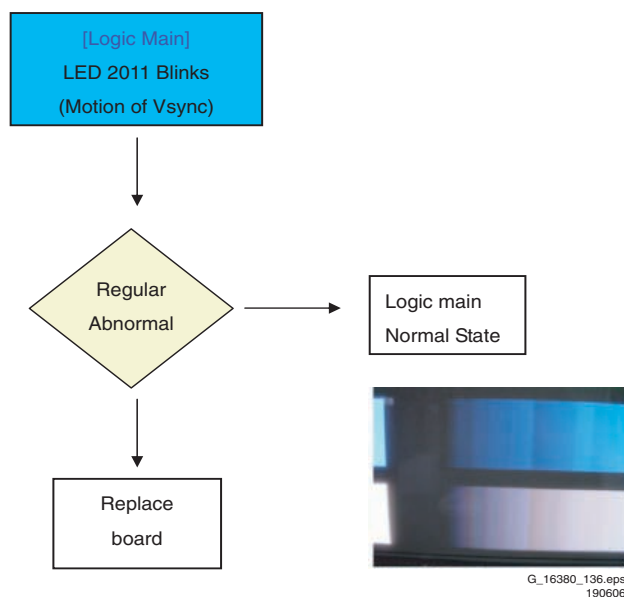


Figure 5-38 Fault symptom: “Abnormal Display” 42” HD w1 2/2

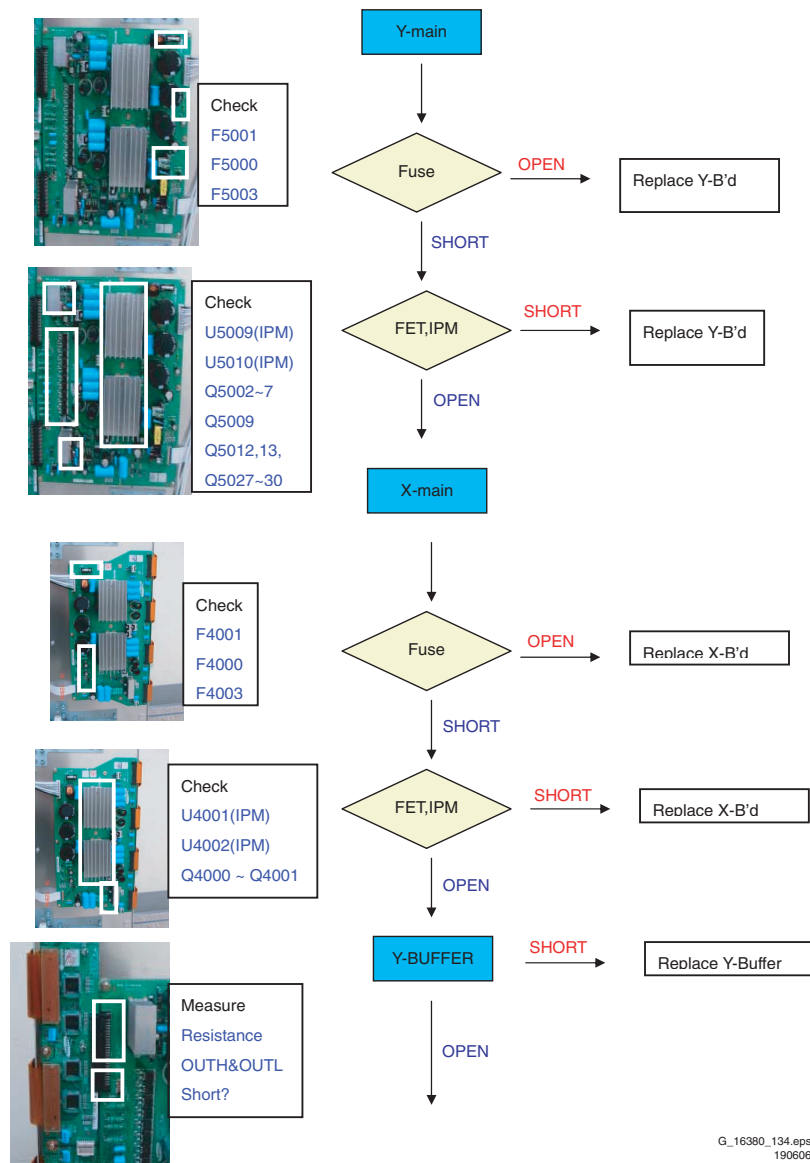


Figure 5-39 Fault symptom: "Abnormal Display" 50" HD w1 1/2

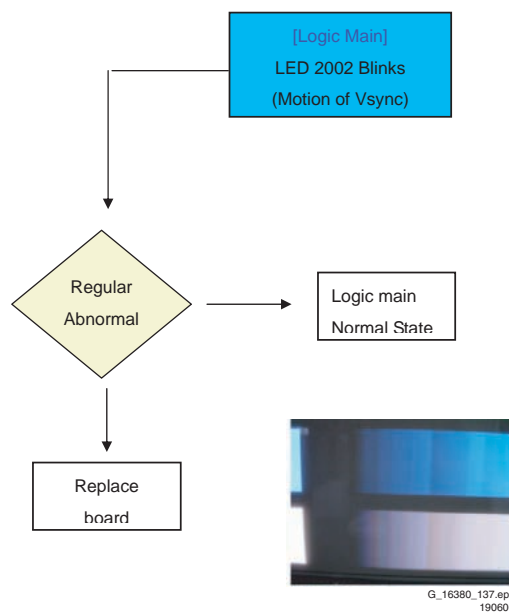
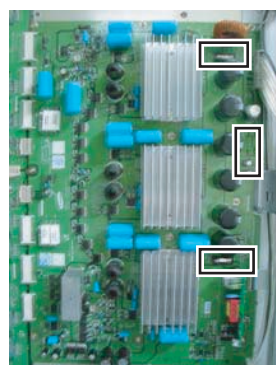
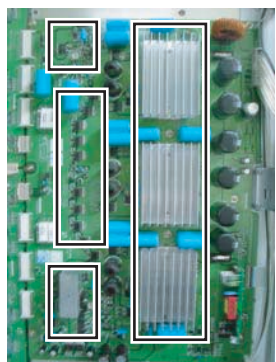


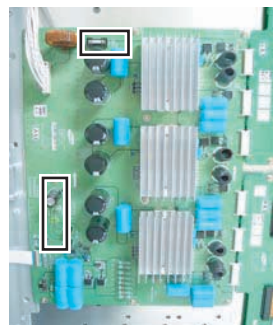
Figure 5-40 Fault symptom: "Abnormal Display" 50" HD w1 2/2



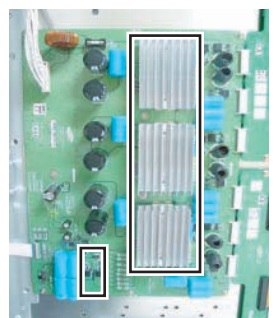
Check
F5000
F5001
F5002
F5004



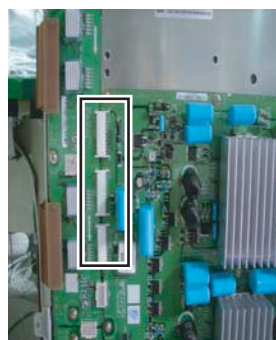
Check
U5000(IPM)
U5001(IPM)
U5002(IPM)
Q5002
Q5022~25
Q5030~33,
Q5036,38
Q5042~45



Check
F4000
F4001
F4003



Check
U4003(IPM)
U4005(IPM)
U4006(IPM)
Q4002, Q4003



Measure
Resistance
OUTH&OUTL
Short?

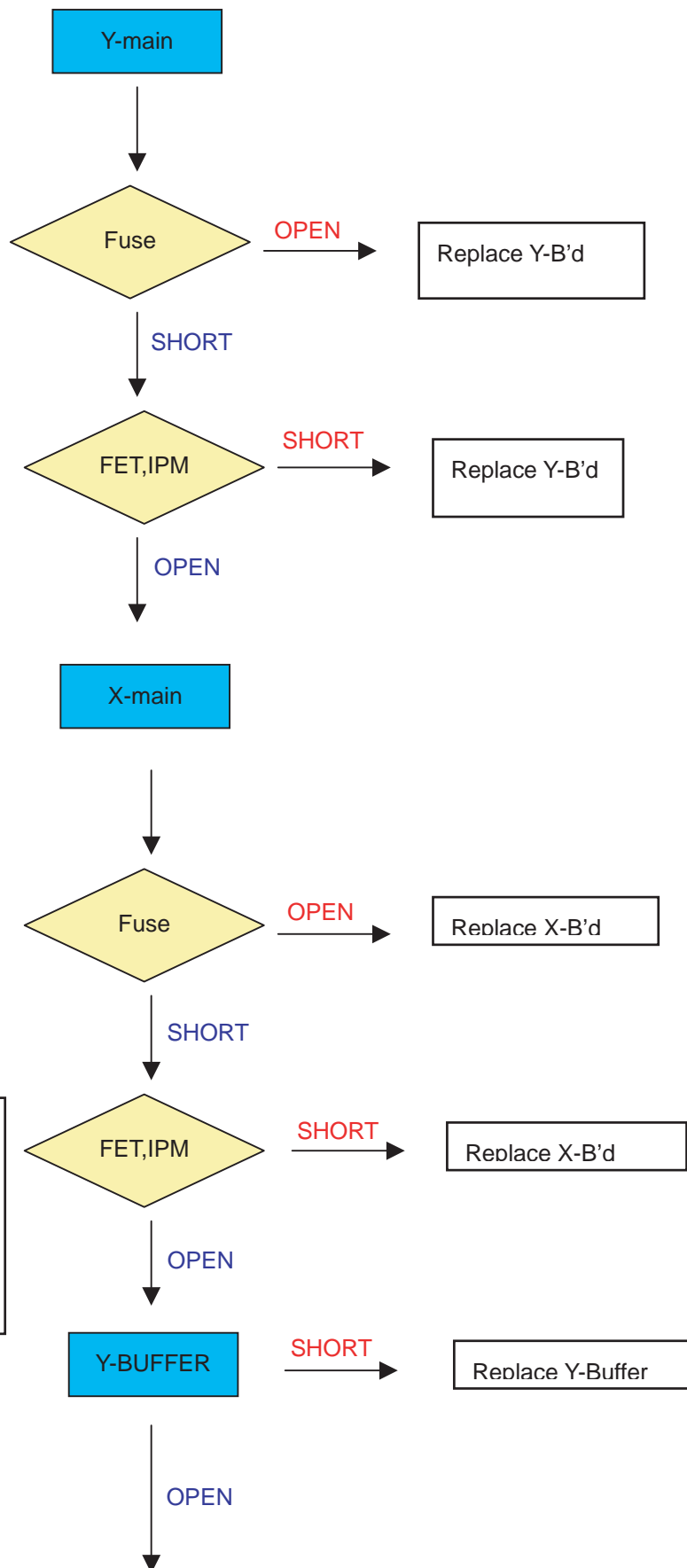


Figure 5-41 Fault symptom: "Abnormal Display" 63" HD v4 1/2

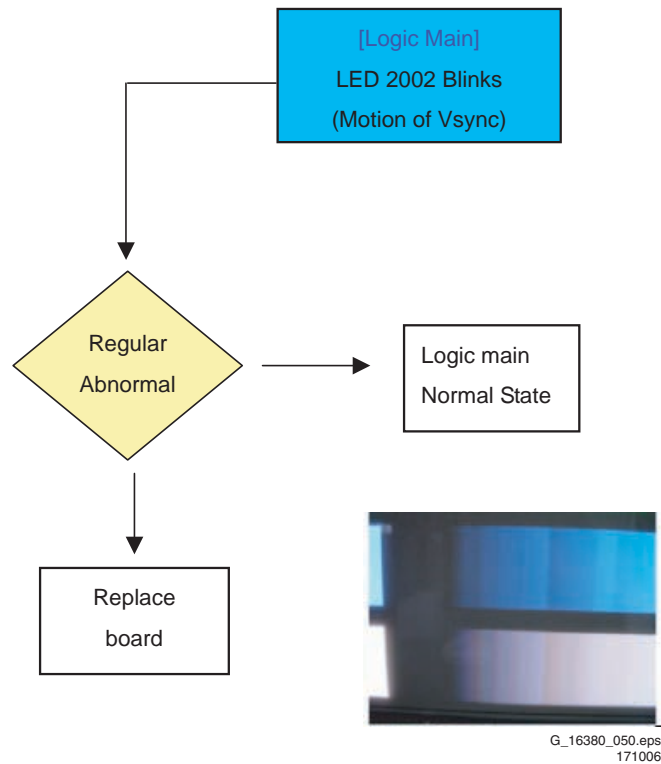


Figure 5-42 Fault symptom: "Abnormal Display" 63" HD v4 2/2

5.2.5 Horizontal line or block open

(some horizontal lines don't exist on screen)

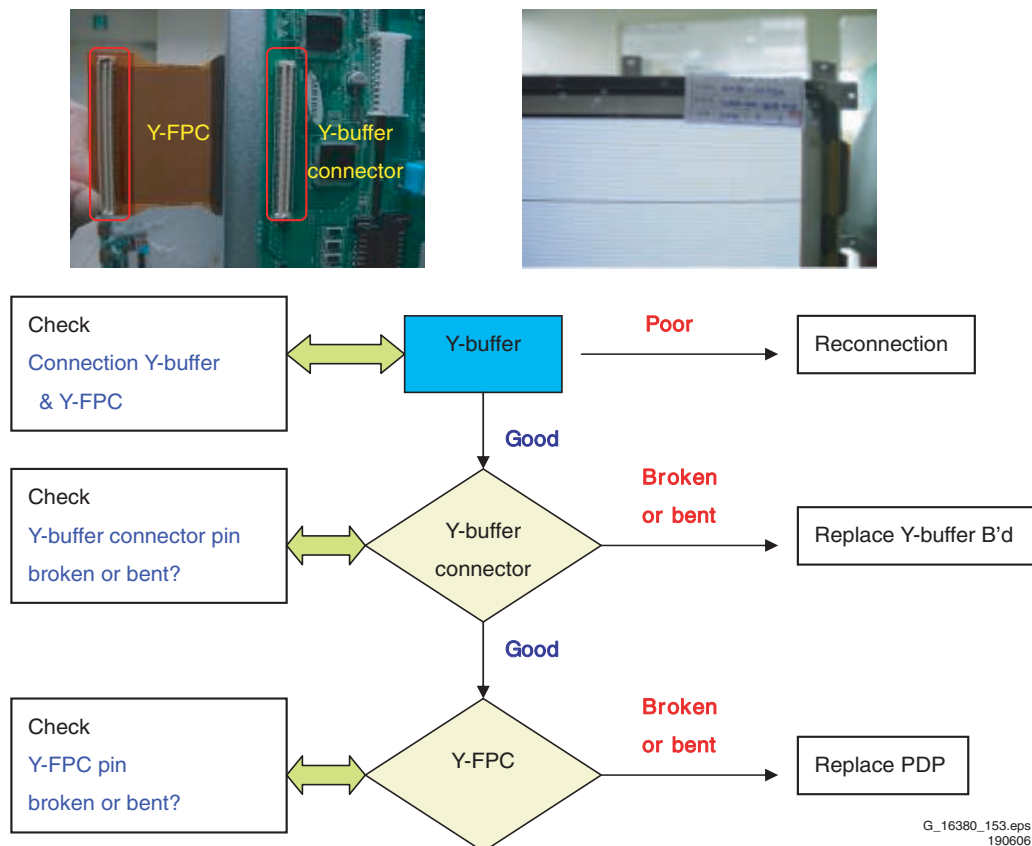


Figure 5-43 Fault symptom: "Horizontal line or block open"

5.2.6 Address open

(some vertical lines don't exist on screen)

-> Address Open is related with Logic Main, Logic Buffer, FFC, TCP and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.

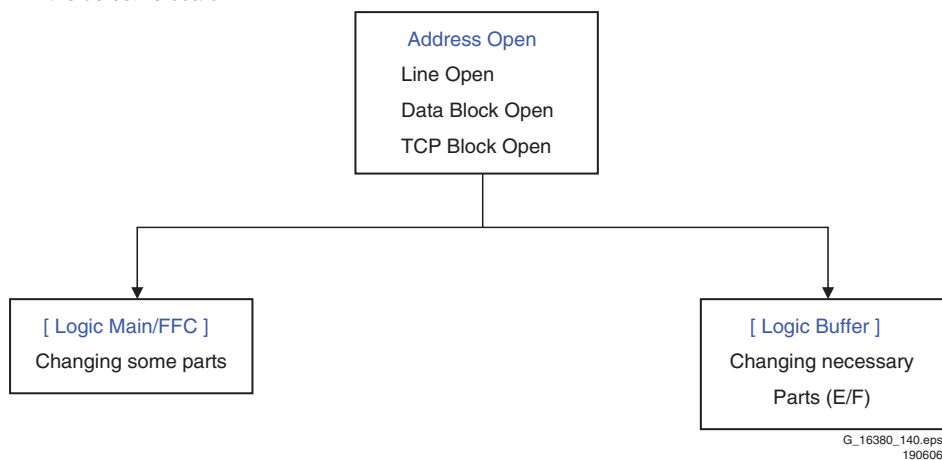


Figure 5-44 Fault symptom: "Address open" 1/2

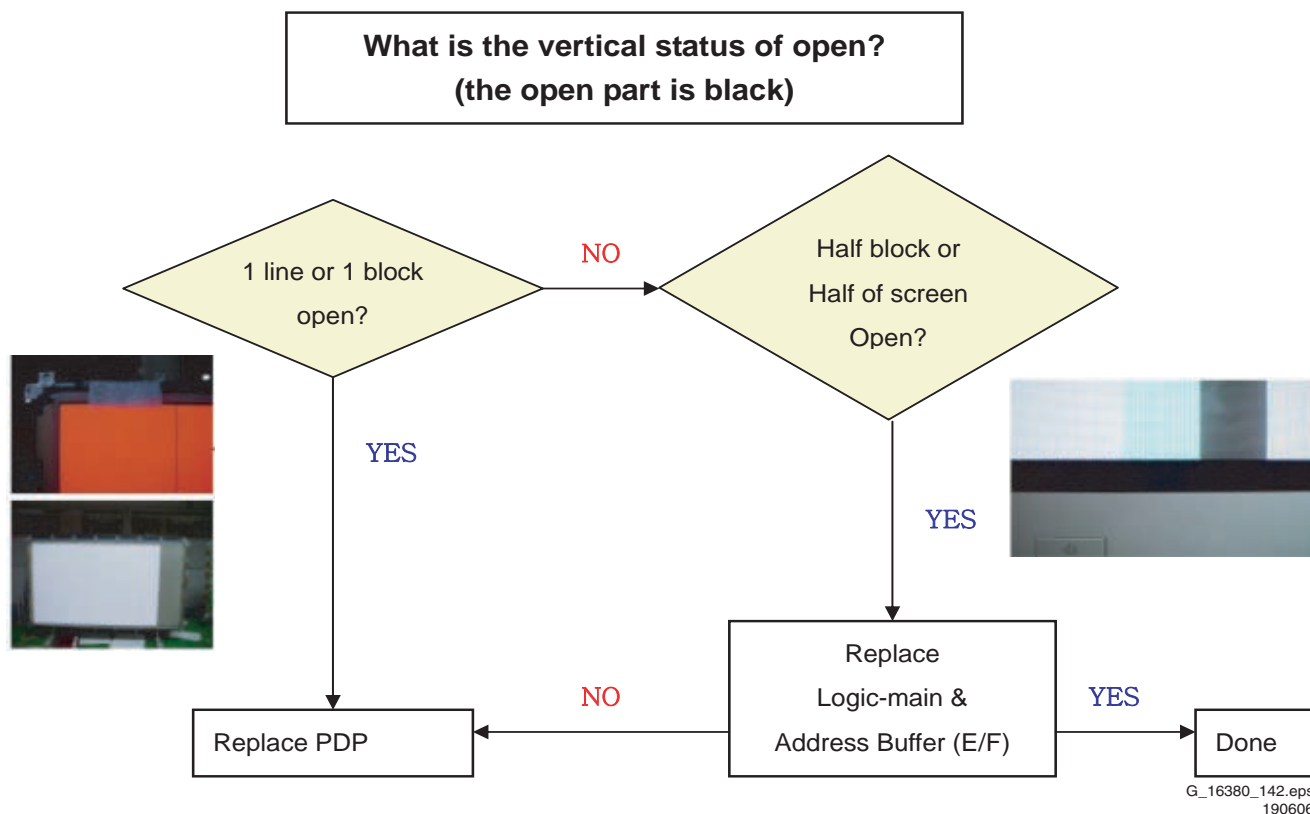


Figure 5-45 Fault symptom: "Address open" 2/2

5.2.7 Address short

(some vertical lines appear to be linked on screen)

-> Address Short is related with Logic Main, Logic Buffer, FFC, TCP and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.

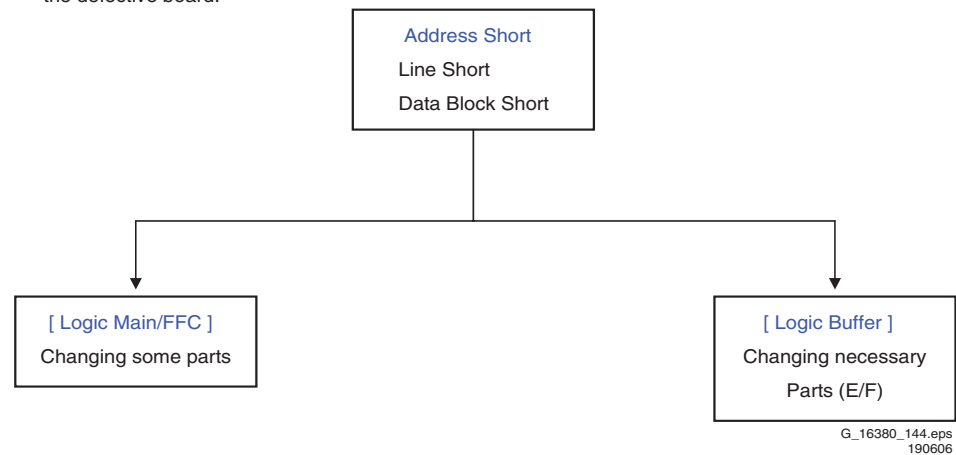


Figure 5-46 Fault symptom: "Address short" 1/2

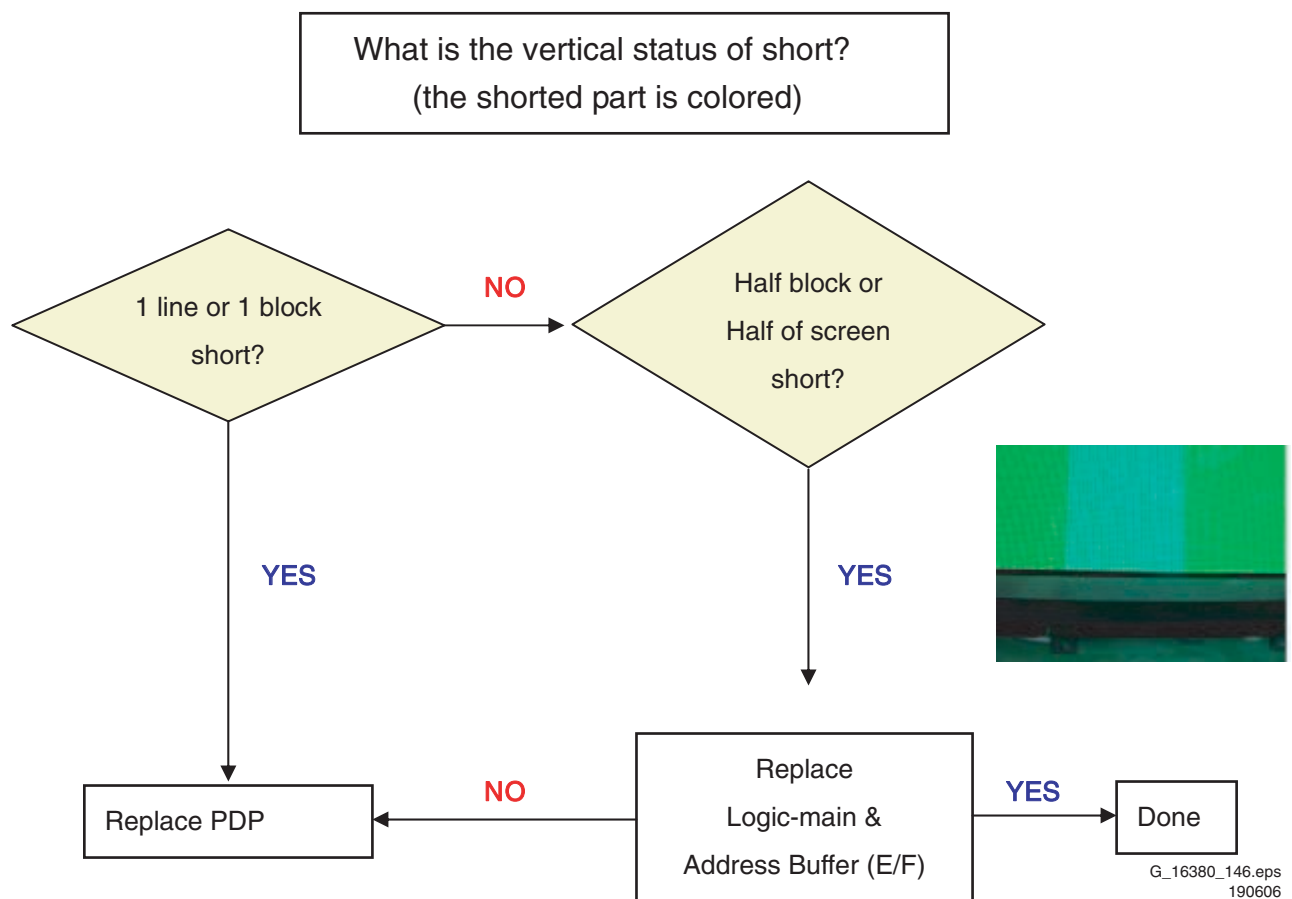


Figure 5-47 Fault symptom: "Address short" 2/2

5.2.8 Criteria for Panel Replacement, due to Defective Panel Cells

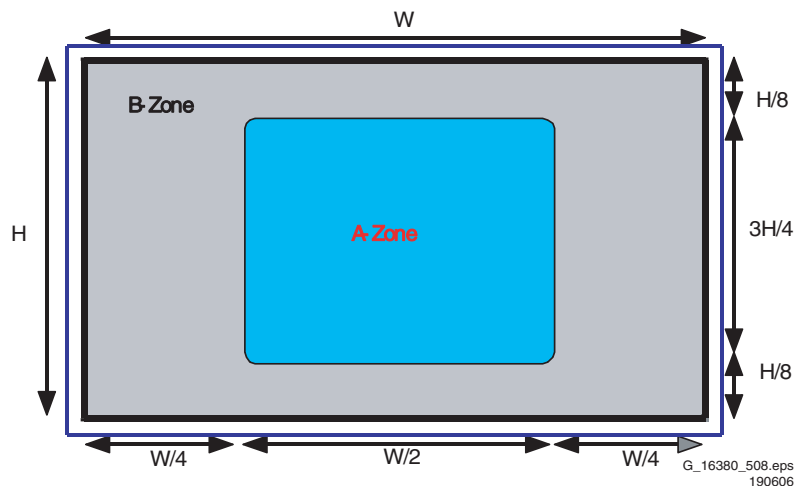


Figure 5-48 Panel zones 42" SD v5

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 0 and less Zone B: 4 and less	Regardless of A and B zone 1 Cell Defect in an area of 50 * 50 mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1	
Flickering cell defect	Zone A: 0 Zone B: 1	
High Intensity Cell defect	Zone A: 0 Zone B: 0	
Adjacent cell defect	Zone A: 0 Zone B: 0	
Total cell defects	6 and less	

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Figure 5-49 Criteria for panel replacement 42" SD v5

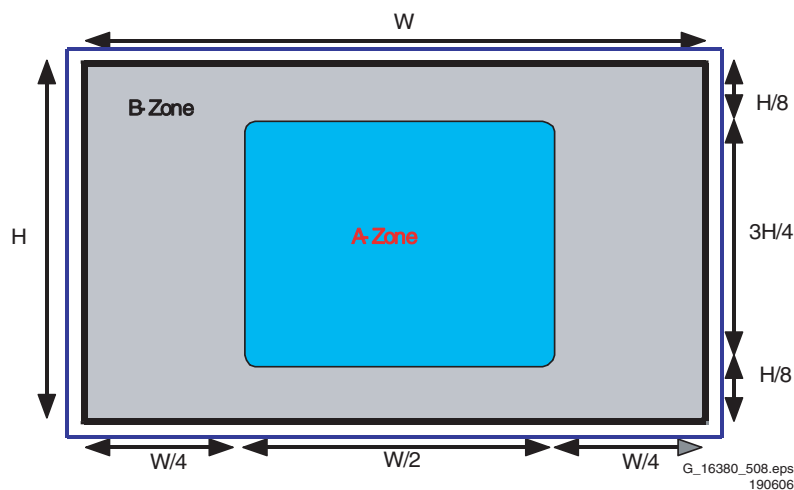


Figure 5-50 Panel zones 42" HD w1

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 4 and less Zone B: 8 and less	Regardless of A and B zone, 1 Cell Defect in an area of 50mm*50mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1 and less	
Flickering cell defect	Zone A: 0 Zone B: 1 and less	
High Intensity Cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Adjacent cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Total cell defects	12 and less	

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Figure 5-51 Criteria for panel replacement 42" HD w1

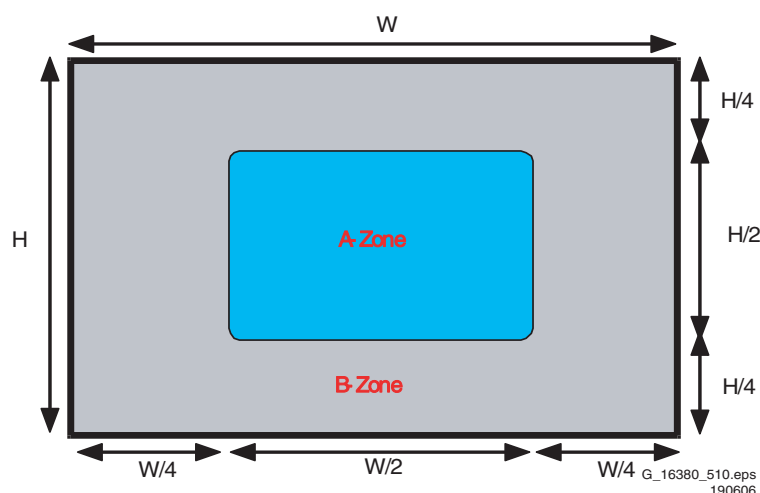
G_16380_510.eps
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Figure 5-52 Panel zones 50" HD w1

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 4 and less Zone B: 8 and less	Regardless of A and B zone, 1 Cell Defect in an area of 50mm*50mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1 and less	
Flickering cell defect	Zone A: 0 Zone B: 1 and less	
High Intensity Cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Adjacent cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Total cell defects	12 and less	

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Figure 5-53 Criteria for panel replacement 50" HD w1

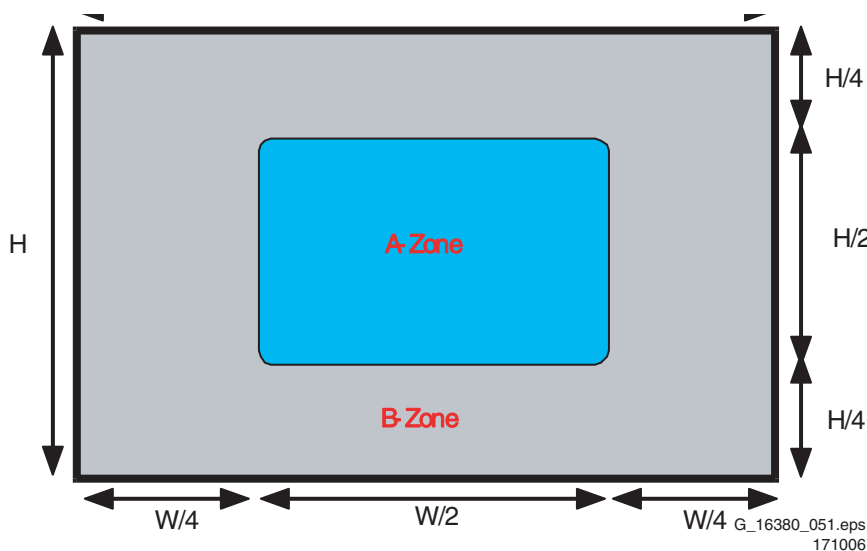


Figure 5-54 Panel zones 63” HD v4

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 2 and less Zone B: 8 and less	Regardless of A and B zone, 1 Cell Defect in an area of 50mm*50mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1 and less	
Flickering cell defect	Zone A: 0 Zone B: 1 and less	
High Intensity Cell defect	Zone A: 0 Zone B: 1 and less (No green cell)	
Adjacent cell defect	Zone A: 0 Zone B: 1 and less (No green cell)	
Total cell defects	10 and less	

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Figure 5-55 Criteria for panel replacement 63” HD v4

5.2.9 Overview

Table 5-2 Overview of faults and cures

Condition Name	Description	Related Board
No output voltage	Operating voltages don't exist.	SMPS
No display	Operating voltages exist, but no image on screen	Y-MAIN, X-MAIN, Logic Main, Cables
Abnormal display	Abnormal Image (not open or short) is on screen.	Y-MAIN, X-MAIN, Logic Main
Sustain open	Some horizontal lines are missing on screen	Scan Buffer, FPC of X / Y
Sustain short	Some horizontal lines appear to be linked on screen	Scan Buffer, FPC of X / Y
Address open	Some vertical lines are missing on screen	Logic Main, Logic Buffer, FFC,TCP
Address short	Some vertical lines appear to be linked on screen	Logic Main, Logic Buffer, FFC,TCP
Defective panel cells	Some cells seem to be defective	Check criteria for replacement of the panel

5.3 Defect Description Form

This form must be used by the workshops for warranty claims:

DDF FLAT TV (panels & boards) version 1.1				Date last modified: 08/03/2005		
To be filled in by <u>WORKSHOP / WORK CENTER</u>						
Country:		<div style="font-size: 24px; font-weight: bold;">Philips</div> <div style="font-size: 18px; font-weight: bold;">LCD & Plasma</div> <div style="border: 1px solid black; padding: 5px; font-weight: bold;">DEFECT DESCRIPTION</div> <div style="border: 1px solid black; padding: 5px; font-weight: bold;">FORM</div>		Type nr./Model nr. set		
Customer Account nr.:				Serial nr. set		
Job sheet nr.:				Type nr. display		
				Serial nr. display		
				Part nr display (12nc)		
				Return number		0170 _ _ _ _ _
GENERAL REPAIR DATA	Condition	<input type="checkbox"/> Constantly <input type="checkbox"/> Intermittently <input type="checkbox"/> After a while <input type="checkbox"/> In a hot environment <input type="checkbox"/> In a cold environment <input type="checkbox"/> Other :				
	Symptom(s)	<input type="checkbox"/> No backlight <input type="checkbox"/> No picture <input type="checkbox"/> Picture too bright <input type="checkbox"/> Shading / smearing on picture <input type="checkbox"/> Only partial picture <input type="checkbox"/> Unstabel picture <input type="checkbox"/> Flickering / flashing picture <input type="checkbox"/> Lines across/down image <input type="checkbox"/> Inactive row(s) <input type="checkbox"/> Inactive column(s) <input type="checkbox"/> Missing colour(s) <input type="checkbox"/> Other:				
PANEL REPAIR	Pixel Defect(s):	<input type="checkbox"/> Dark dots <input type="checkbox"/> Bright dots	Qty of dots :	Mark Defect(s)	<div style="color: red; font-weight: bold; font-size: 1.2em;">----- Picture -----</div> <p>Insert picture or mark defect !</p>	
	Symptoms	Following defect symptoms are out of warranty: <div style="display: flex; justify-content: space-between;"> <div> <ul style="list-style-type: none"> Broken glass Scratch(es) on display </div> <div> <ul style="list-style-type: none"> Number of dark/bright pixels within spec. Burn in (only for Plasma TV) </div> </div>				These symptoms are not claimable.
BOARD REPAIR	For Plasma TV repair only		Spare Part Nr. New Board	Barcode Nr. Defect Board	Barcode Nr. Replaced Board	
	1.					
	2.					
	3.					
	4.					
To be filled in by <u>EUROSERVICE</u>			RMA number:		Date of receipt:	
<p>Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected.</p> <p>Note 2: Please fill out this form <u>completely</u> and correctly, otherwise Euroservice is unable to fulfil the repair request!</p>						
Owner: PHILIPS CE EUROSERVICE DE10WEG						

Figure 5-56 Defect Description Form (DDF)

6. Block Diagrams, Test Point Overview, and Waveforms

Index of this chapter:

- 6.1 Block Diagram for Drive Circuits

6.2 Block Diagram for Logic Circuit

6.3 PSU

6.3.1 PSU Layout, Display Types 42" SD v5, 42" HD w1, and 50" HD w1
- 6.3.2 PSU Layout, Display Type 63" HD v4

6.3.3 Voltage Level Overview 42" SD v5

6.3.4 Voltage Level Overview 42" HD w1

6.3.5 Voltage Level Overview 50" HD w1

6.3.6 Voltage Level Overview 63" HD v4

6.1 Block Diagram for Drive Circuits

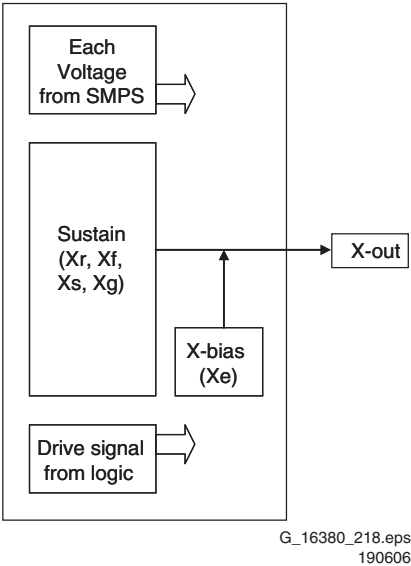


Figure 6-1 Block diagram X-Main Board

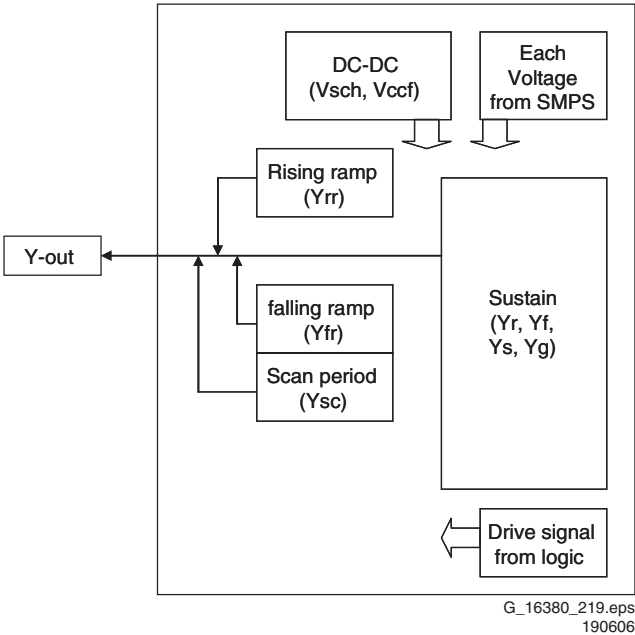


Figure 6-2 Block diagram Y-Main Board

6.2 Block Diagram for Logic Circuit

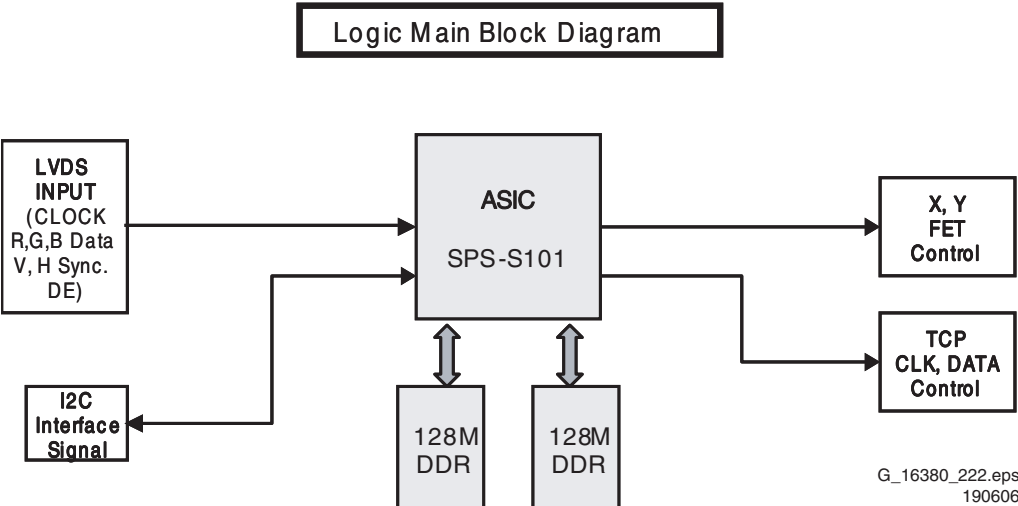


Figure 6-3 Block diagram (42" SD v5)

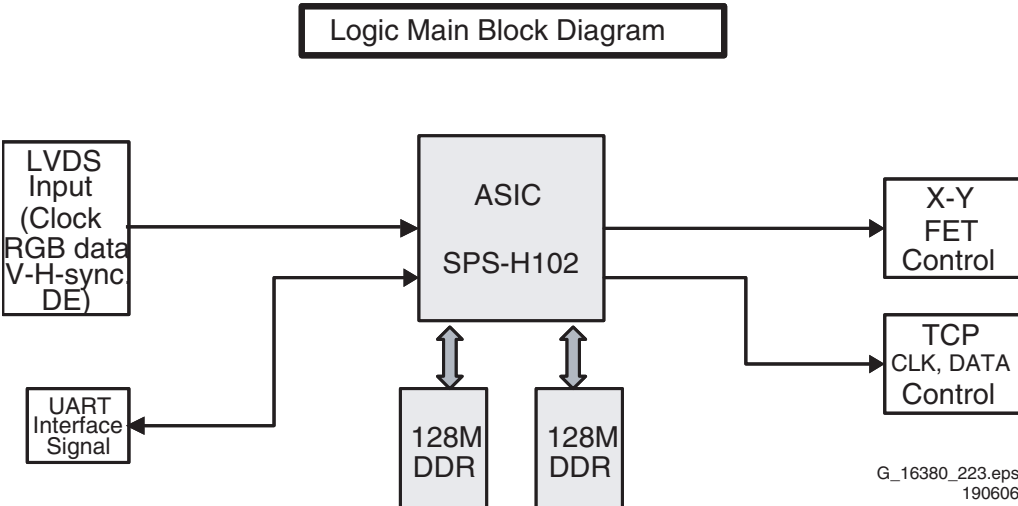


Figure 6-4 Block diagram (42" HD w1)

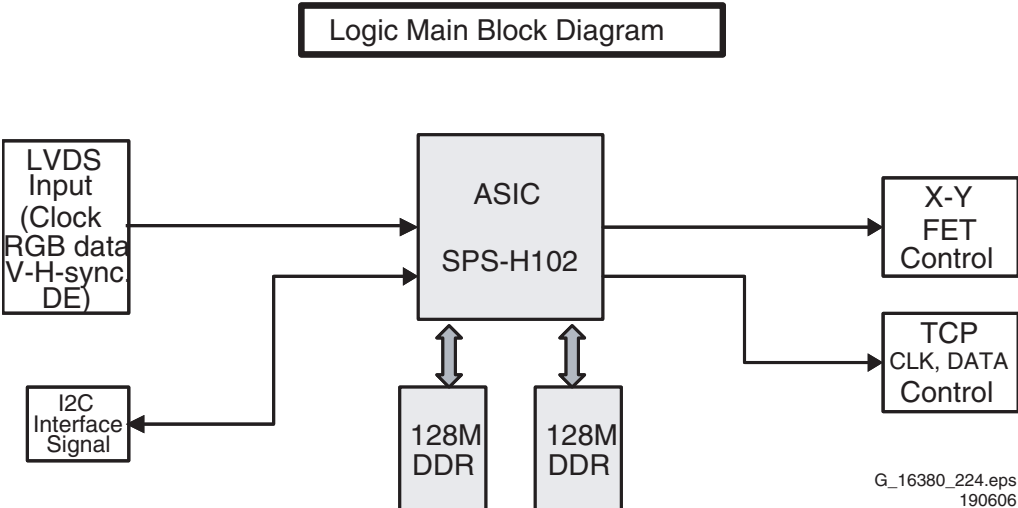


Figure 6-5 Block diagram (50" HD w1 and 63" HD v4)

6.3 PSU

6.3.1 PSU Layout, Display Types 42" SD v5, 42" HD w1, and 50" HD w1

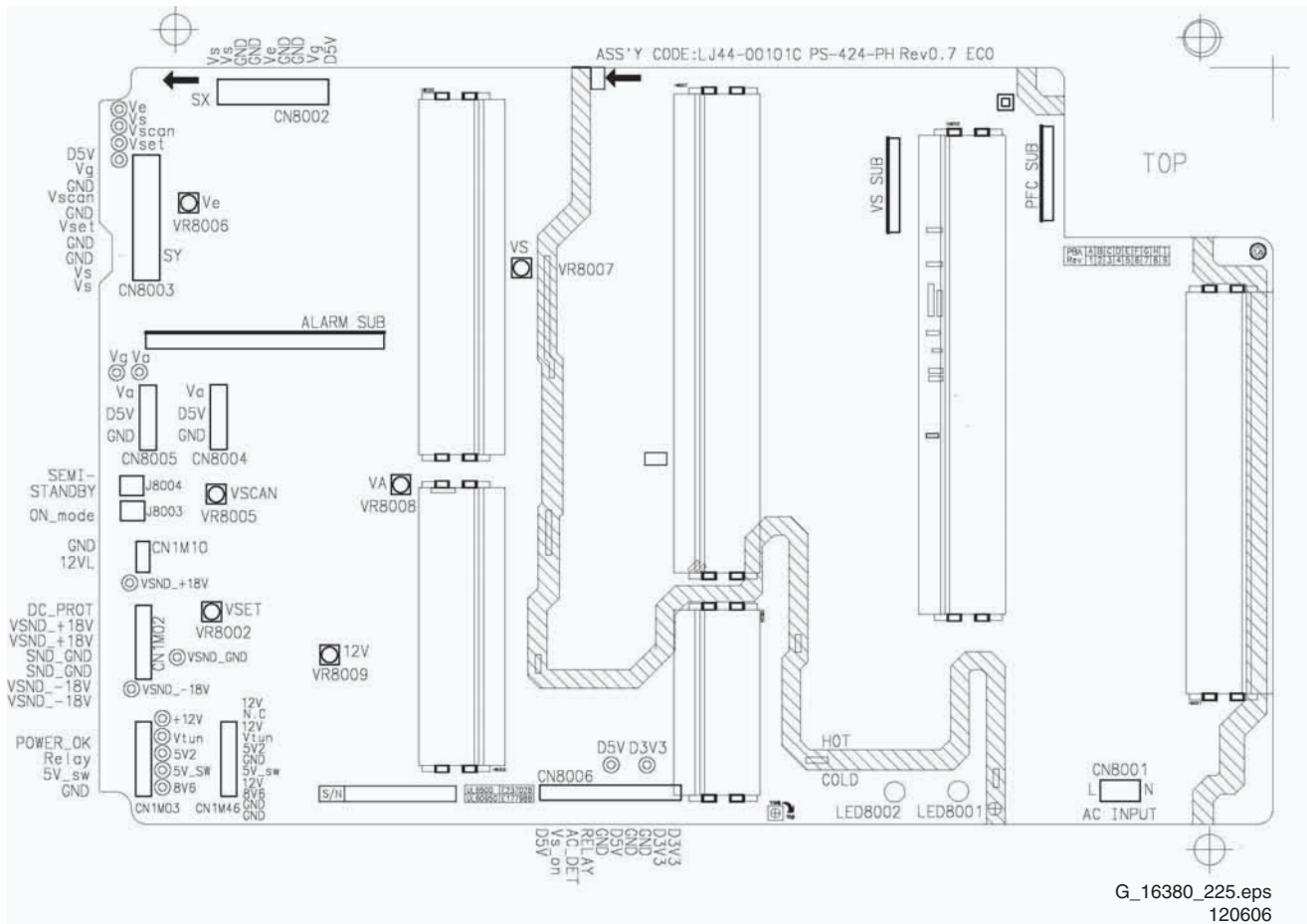


Figure 6-6 PSU layout (42" SD v5, 42" HD w1, and 50" HD w1)

6.3.2 PSU Layout, Display Type 63" HD v4

Package 1, Main Supply

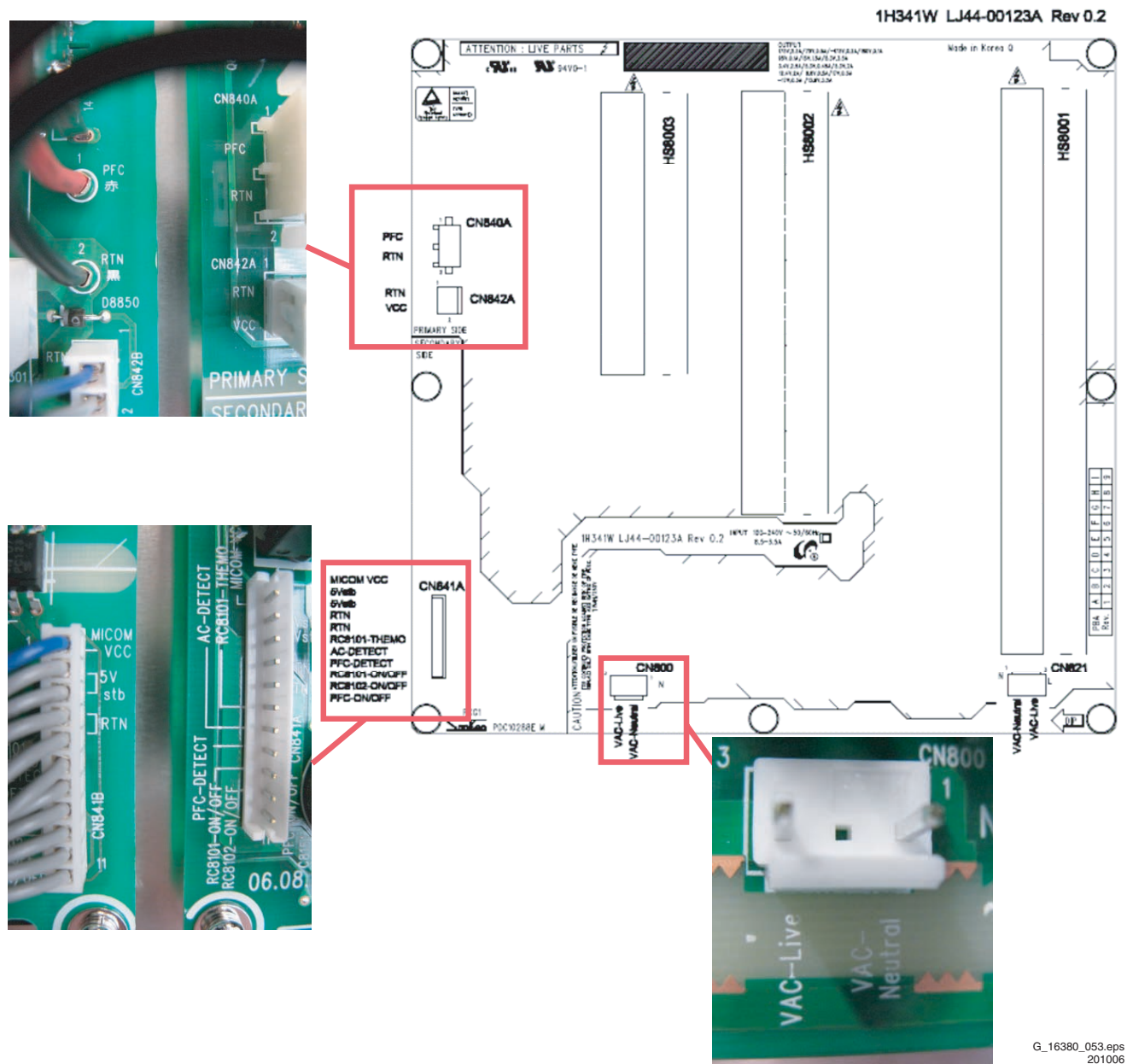


Figure 6-7 PSU layout (63" HD v4, Main PSU)

Package 2, Sub Supply

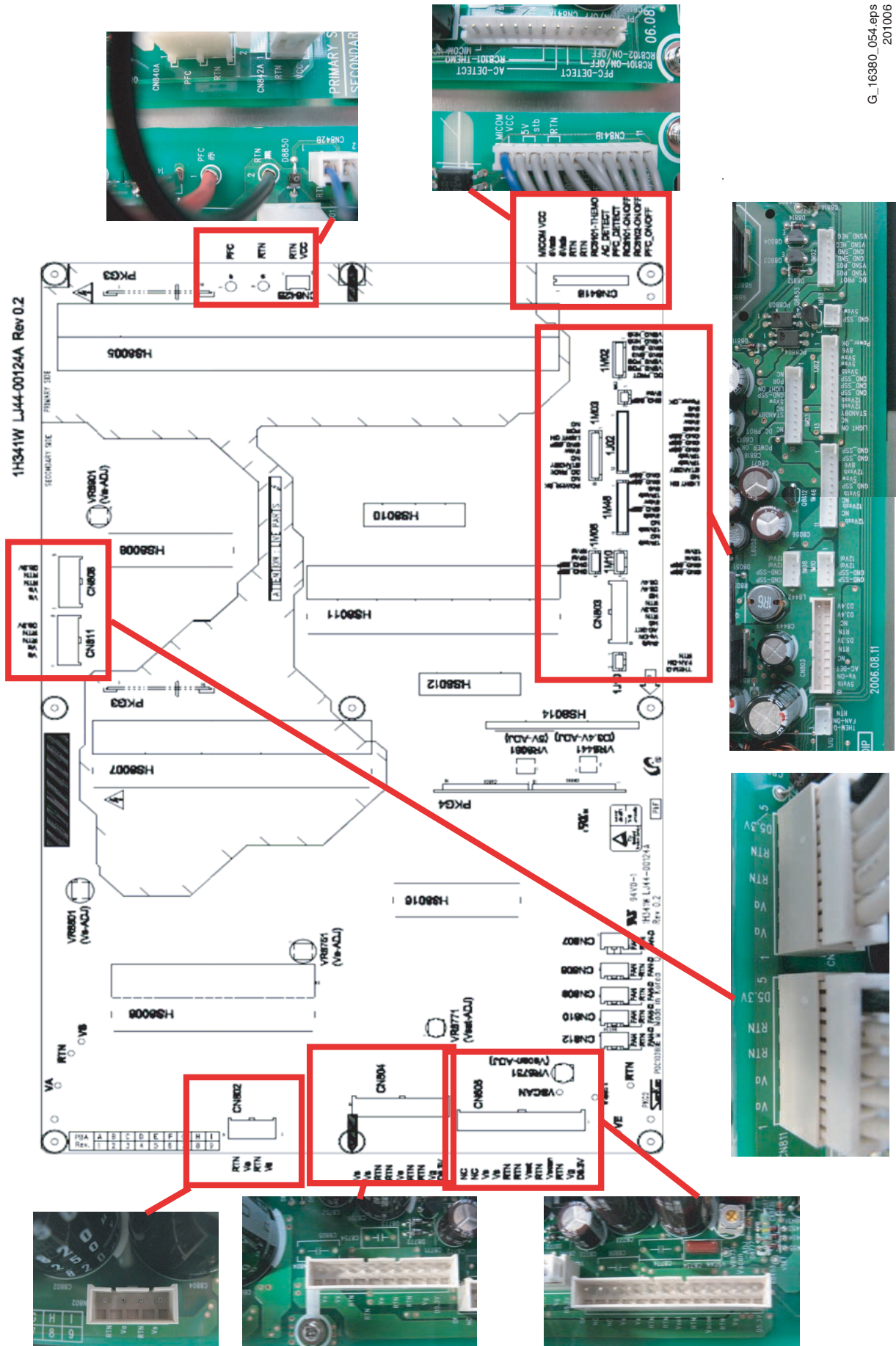


Figure 6-8 PSU layout (63" HD v4, Sub PSU))

6.3.3 Voltage Level Overview 42" SD v5

Table 6-1 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	207 V \pm 1 %	195 V ~ 215 V
2	VA	65 V \pm 1.5 %	50 V ~ 70 V
3	VE	110 V \pm 1.5 %	70 V ~ 110 V
4	VSET	201 V \pm 1.5 %	180 V ~ 210 V
5	VSCAN	-190 V \pm 1.5 %	-190 V ~ -170 V
6	VSB	5 V \pm 5 %	Fixed
7	VG	15 V \pm 5 %	Fixed
8	D5VL	5.2 V \pm 5 %	Fixed
9	D3V3	3.3 V \pm 5 %	Fixed
Check voltage label on the PDP for correct values.			

6.3.4 Voltage Level Overview 42" HD w1

Table 6-2 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	200 V \pm 1.5 %	198 V ~ 202 V
2	VA	65 V \pm 1.5 %	63 V ~ 67 V
3	VE	110 V \pm 1.5 %	105 V ~ 115 V
4	VSET	195 V \pm 1.5 %	193 V ~ 197 V
5	VSCAN	-190 V \pm 1.5 %	-192 V ~ -188 V
6	VG	15 V \pm 5 %	Fixed
7	D5VL	5.2 V \pm 5 %	Fixed
8	D3V3	3.3 V \pm 5 %	Fixed
Check voltage label on the PDP for correct values.			

6.3.5 Voltage Level Overview 50" HD w1

Table 6-3 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	202 V \pm 1 %	190 V ~ 210 V
2	VA	65 V \pm 1.5 %	55 V ~ 75 V
3	VE	115 V \pm 1.5 %	110 V ~ 130 V
4	VSET	190 V \pm 1.5 %	170 V ~ 200 V
5	VSCAN	-190 V \pm 1.5 %	-210 V ~ -180 V
6	VSB	5 V \pm 5 %	Fixed
7	VG	15 V \pm 5 %	Fixed
8	D5VL	5.2 V \pm 5 %	Fixed
9	D3V3	3.3 V \pm 5 %	Fixed
Check voltage label on the PDP for correct values.			

6.3.6 Voltage Level Overview 63" HD v4

Table 6-4 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	184 V \pm 1 %	165 V ~ 190 V
2	VA	72 V \pm 1.5 %	60 V ~ 85 V
3	VE	88 V \pm 1.5 %	80 V ~ 110 V
4	VSET	178 V \pm 1.5 %	160 V ~ 200 V
5	VSCAN	-160 V \pm 1.5 %	-190 V ~ -155 V
6	VSB	5 V \pm 5 %	Fixed
7	VG	15 V \pm 5 %	Fixed
8	D5VL	5.3 V \pm 5 %	Fixed
9	D3V3	3.4 V \pm 5 %	Fixed
Check voltage label on the PDP for correct values.			

7. Circuit Diagrams and PWB Layouts

Not applicable.

8. Alignments

Index of this chapter:

- 8.1 Power Supply Voltages
- 8.2 Waveform Alignments 42" SD v5
- 8.3 Waveform Alignments 42" HD w1
- 8.4 Waveform Alignments 50" HD w1
- 8.5 Waveform Alignments 63" HD v4

Note:

- Figures can deviate due to the different model executions.

Important: Remove all non-default jumpers and reset all DIP switches, after the repair!

8.1 Power Supply Voltages

8.1.1 Location of potentiometers and test points on the PSU of 42"SD v5, 42" HD w1, and 50" HD w1

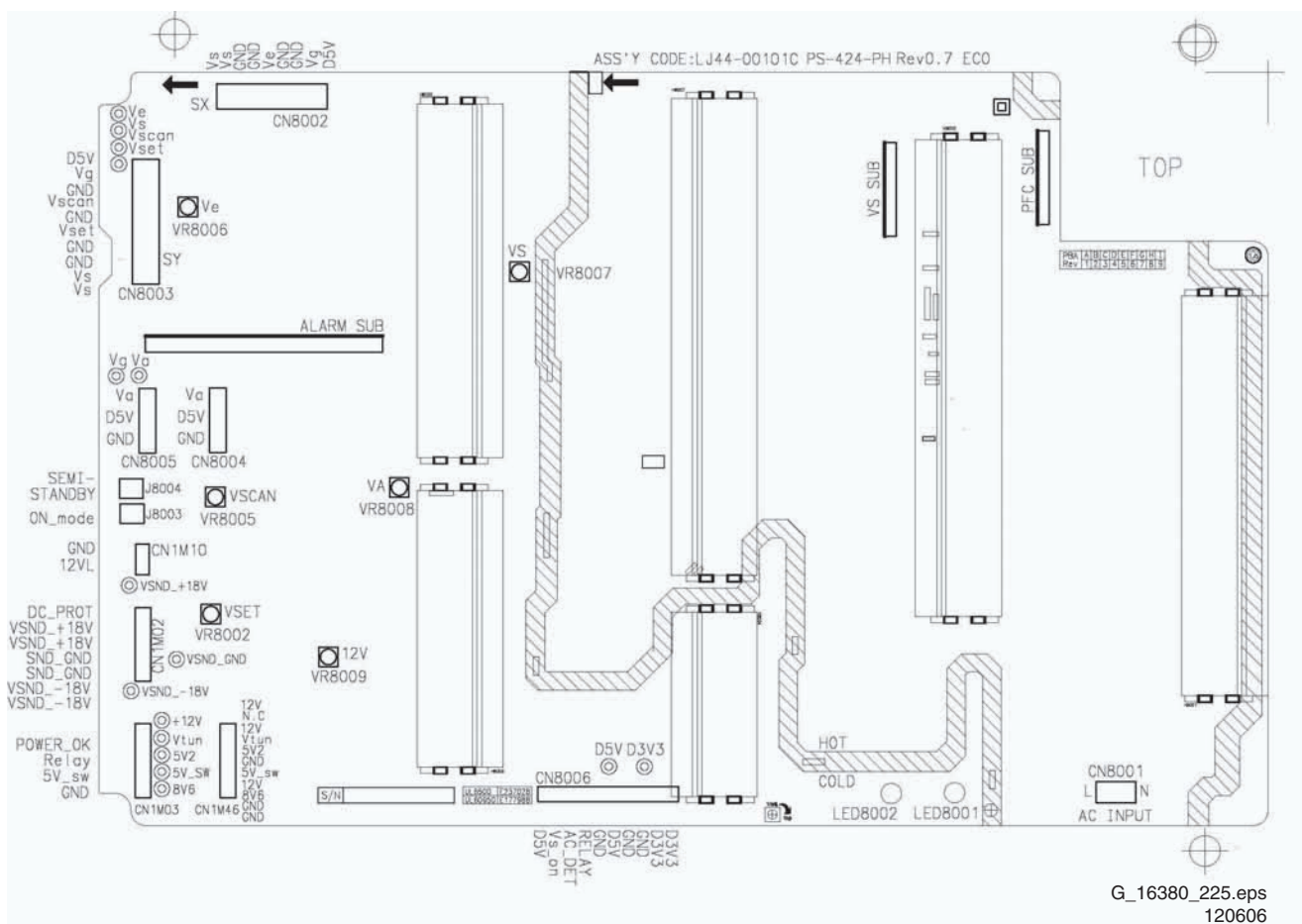


Figure 8-1 Location of potentiometers and test points on the PSU of 42"SD v5, 42" HD w1, and 50" HD w1

8.1.2 Location of potentiometers and test points on the PSU of 63" HD v4

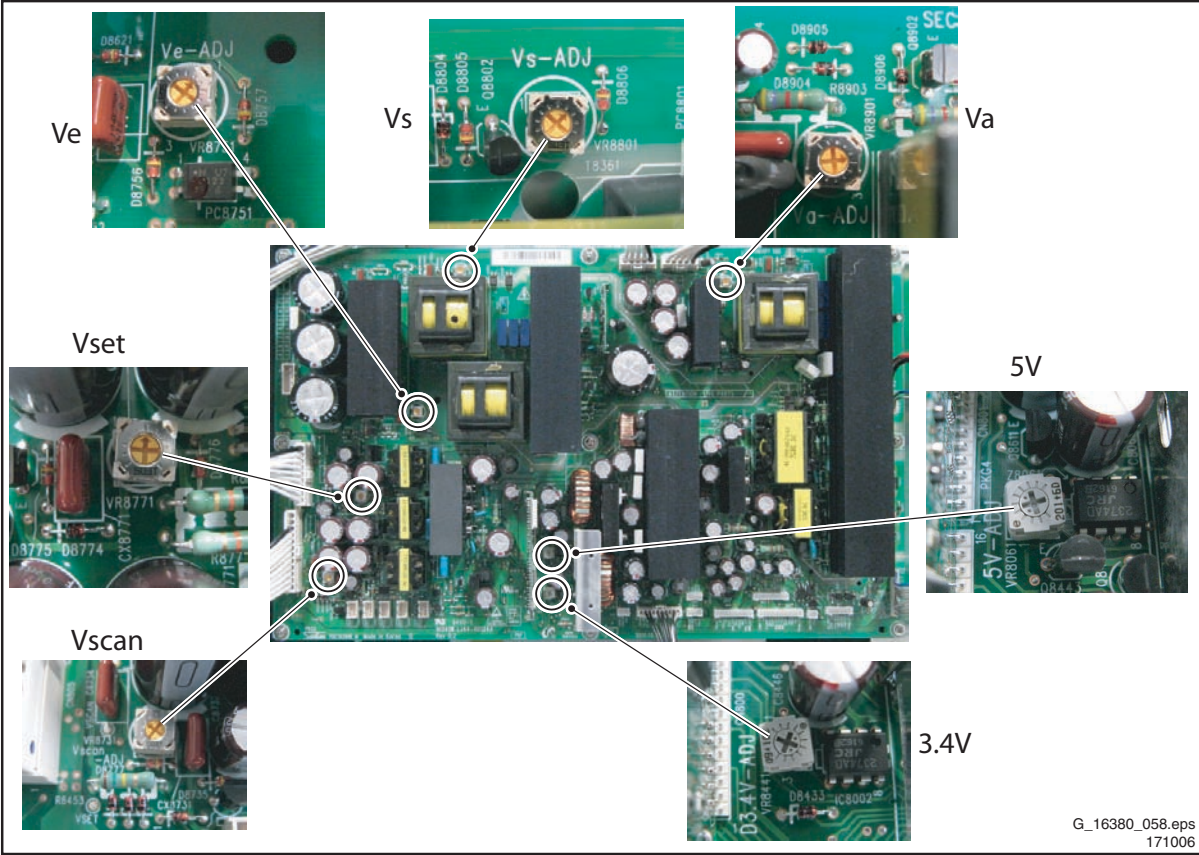


Figure 8-2 Location of potentiometers on the PSU of 63" HD v4

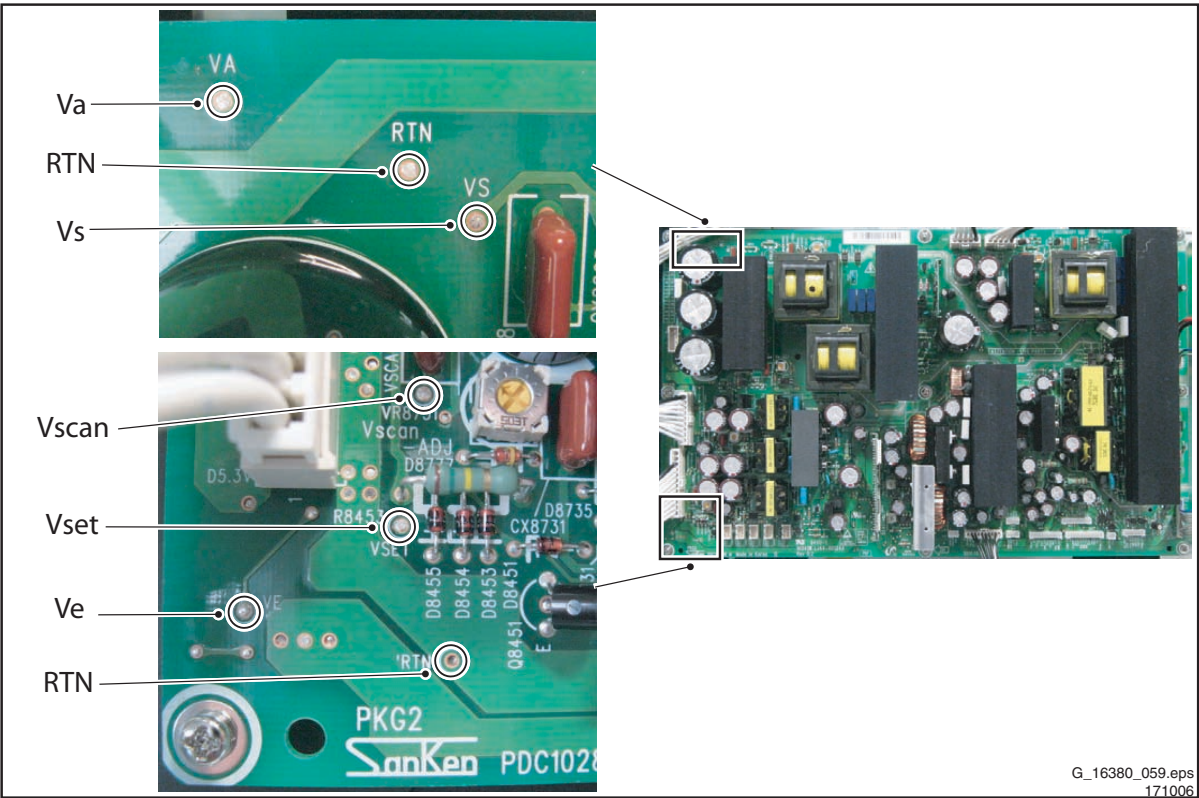


Figure 8-3 Location of test points on the PSU of 63" HD v4

8.1.3 Adjustment Power Supply Voltages 42" SD v5

Table 8-1 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	207 V ± 1 %	195 V ~ 215 V
2	VA	65 V ± 1.5 %	50 V ~ 70 V
3	VE	110 V ± 1.5 %	70 V ~ 110 V
4	VSET	201 V ± 1.5 %	180 V ~ 210 V
5	VSCAN	-190 V ± 1.5 %	-190 V ~ -170 V
6	VSB	5 V ± 5 %	Fixed
7	VG	15 V ± 5 %	Fixed
8	D5VL	5.2 V ± 5 %	Fixed
9	D3V3	3.3 V ± 5 %	Fixed

Check voltage label on the PDP for correct values.

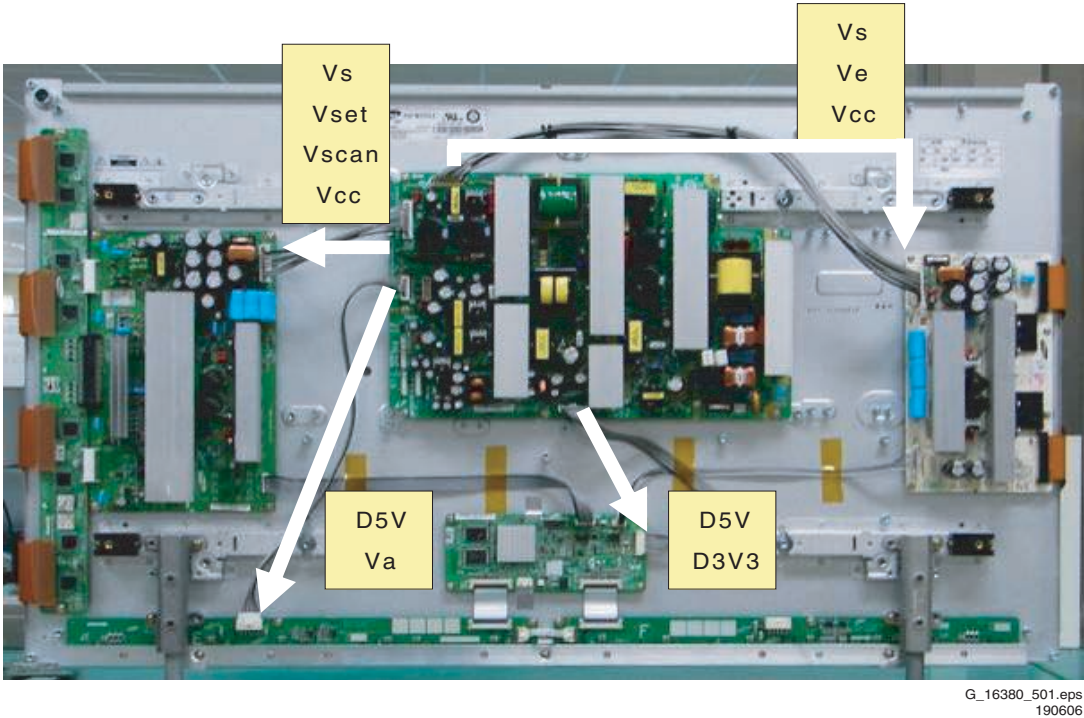


Figure 8-4 Location of the supply lines from the PSU to the boards - 42" SD v5

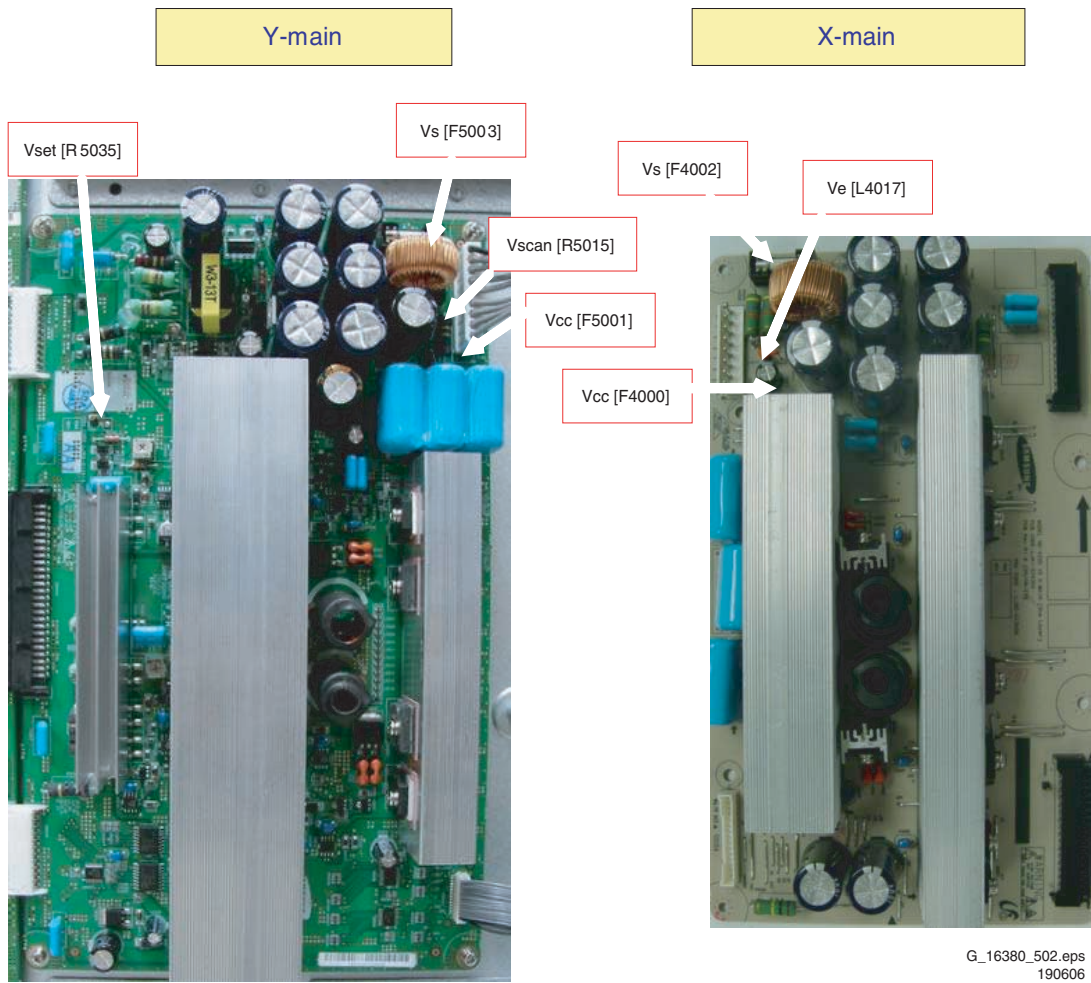


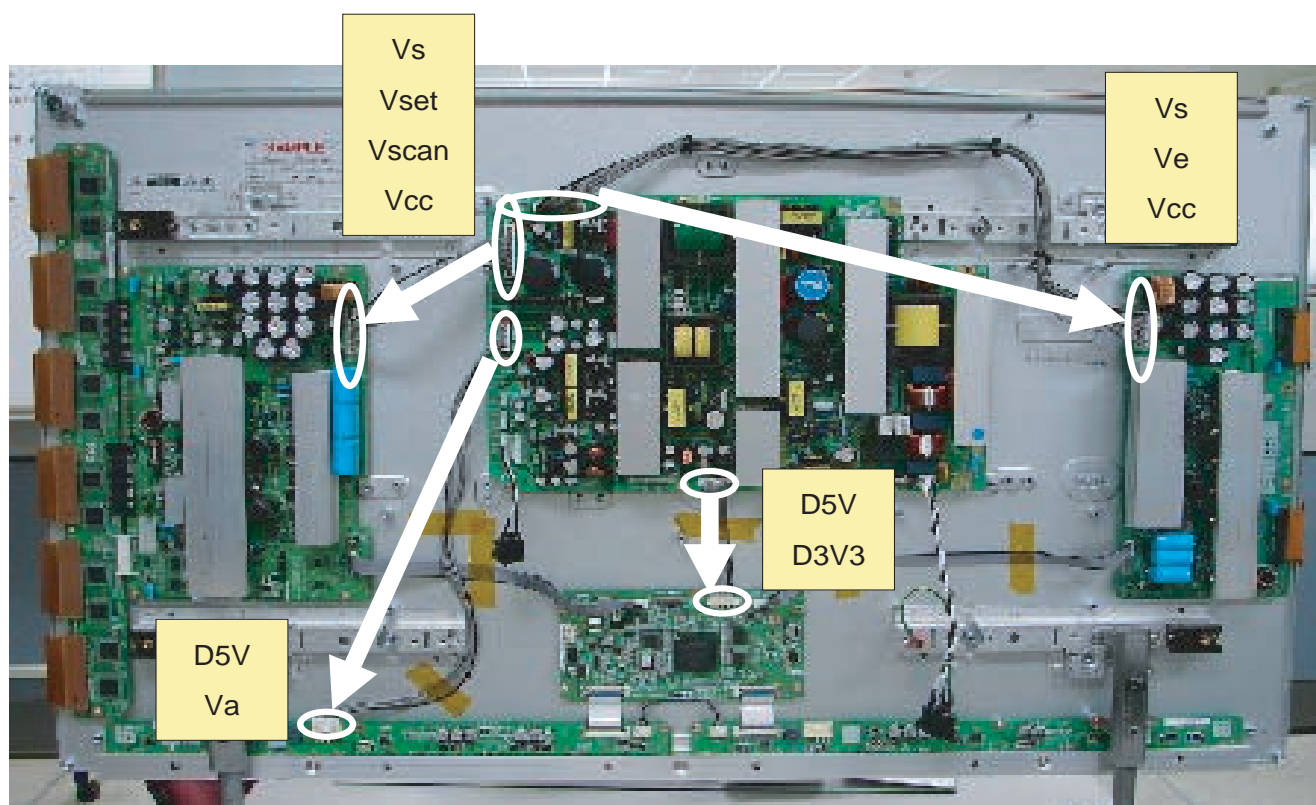
Figure 8-5 Location of the test points for the supply voltages - 42" SD v5

8.1.4 Adjustment Power Supply Voltages 42" HD w1

Table 8-2 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	200 V ± 1.5 %	198 V ~ 202 V
2	VA	65 V ± 1.5 %	63 V ~ 67 V
3	VE	110 V ± 1.5 %	105 V ~ 115 V
4	VSET	195 V ± 1.5 %	193 V ~ 197 V
5	VSCAN	-190 V ± 1.5 %	-192 V ~ -188 V
6	VG	15 V ± 5 %	Fixed
7	D5VL	5.2 V ± 5 %	Fixed
8	D3V3	3.3 V ± 5 %	Fixed

Check voltage label on the PDP for correct values.




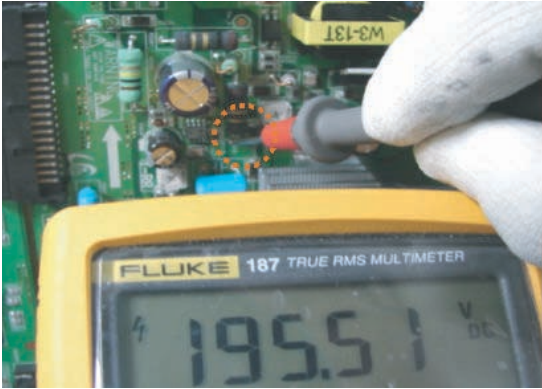





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Figure 8-6 Location of the supply lines from the PSU to the boards - 42" HD w1

Drive board's voltage check point





Y- main Voltage Check Point

	
YM Vs (200V) – F5003	YM Vscan (-190V) – R5081
	
YM Vsch (-70V) – Vsch TP	YM Vset (195V) – R5048
	
YM 5.5V (5.5V) – F5001	YM Vccf (Vscan + 15V) – Vccf TP
	
YM Vcc (15V) – F5004	

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Figure 8-7 Location of the test points for the supply voltages - Y-main - 42” HD w1

X-main Voltage Check Point

	
Vs (200V) – F4003	Ve (110V) – F4005
	
Vcc (15V) – F4001	5.5V (5.5V) – F4004

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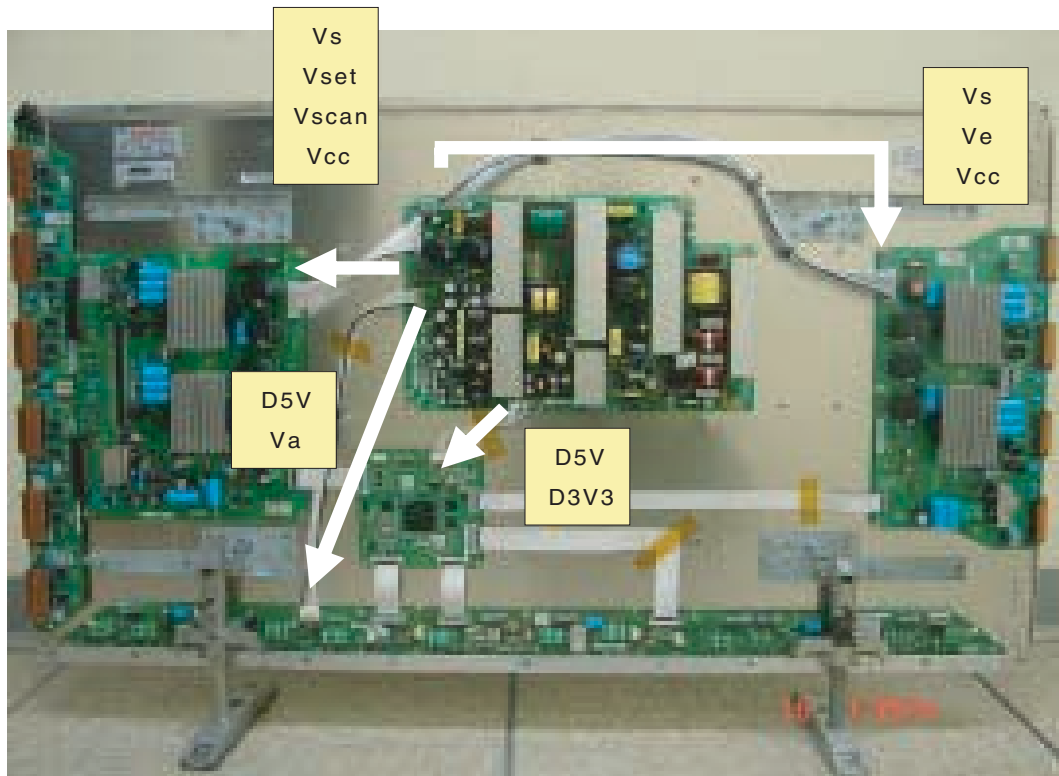
Figure 8-8 Location of the test points for the supply voltages - X-main - 42" HD w1

8.1.5 Adjustment Power Supply Voltages 50" HD w1

Table 8-3 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

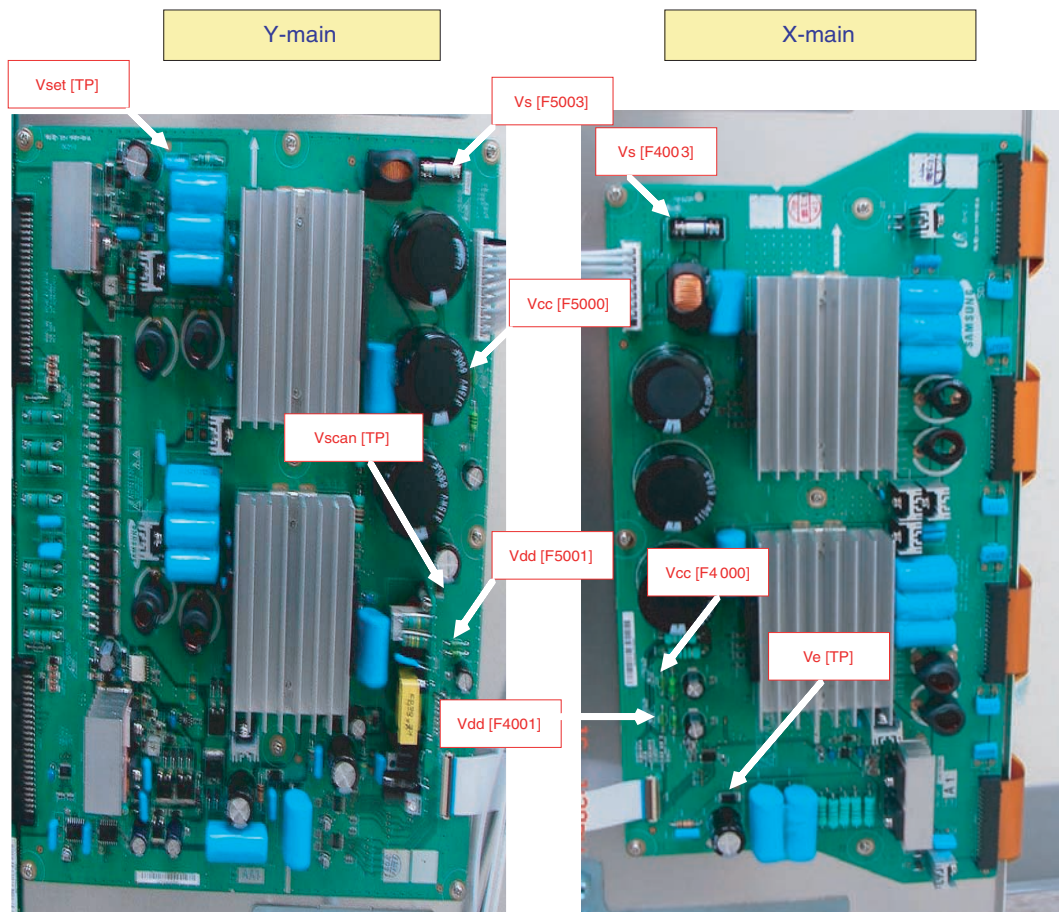
No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	202 V ± 1 %	190 V ~ 210 V
2	VA	65 V ± 1.5 %	55 V ~ 75 V
3	VE	115 V ± 1.5 %	110 V ~ 130 V
4	VSET	190 V ± 1.5 %	170 V ~ 200 V
5	VSCAN	-190 V ± 1.5 %	-210 V ~ -180 V
6	VSB	5 V ± 5 %	Fixed
7	VG	15 V ± 5 %	Fixed
8	D5VL	5.2 V ± 5 %	Fixed
9	D3V3	3.3 V ± 5 %	Fixed

Check voltage label on the PDP for correct values.



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Figure 8-9 Location of the supply lines from the PSU to the boards - 50" HD w1



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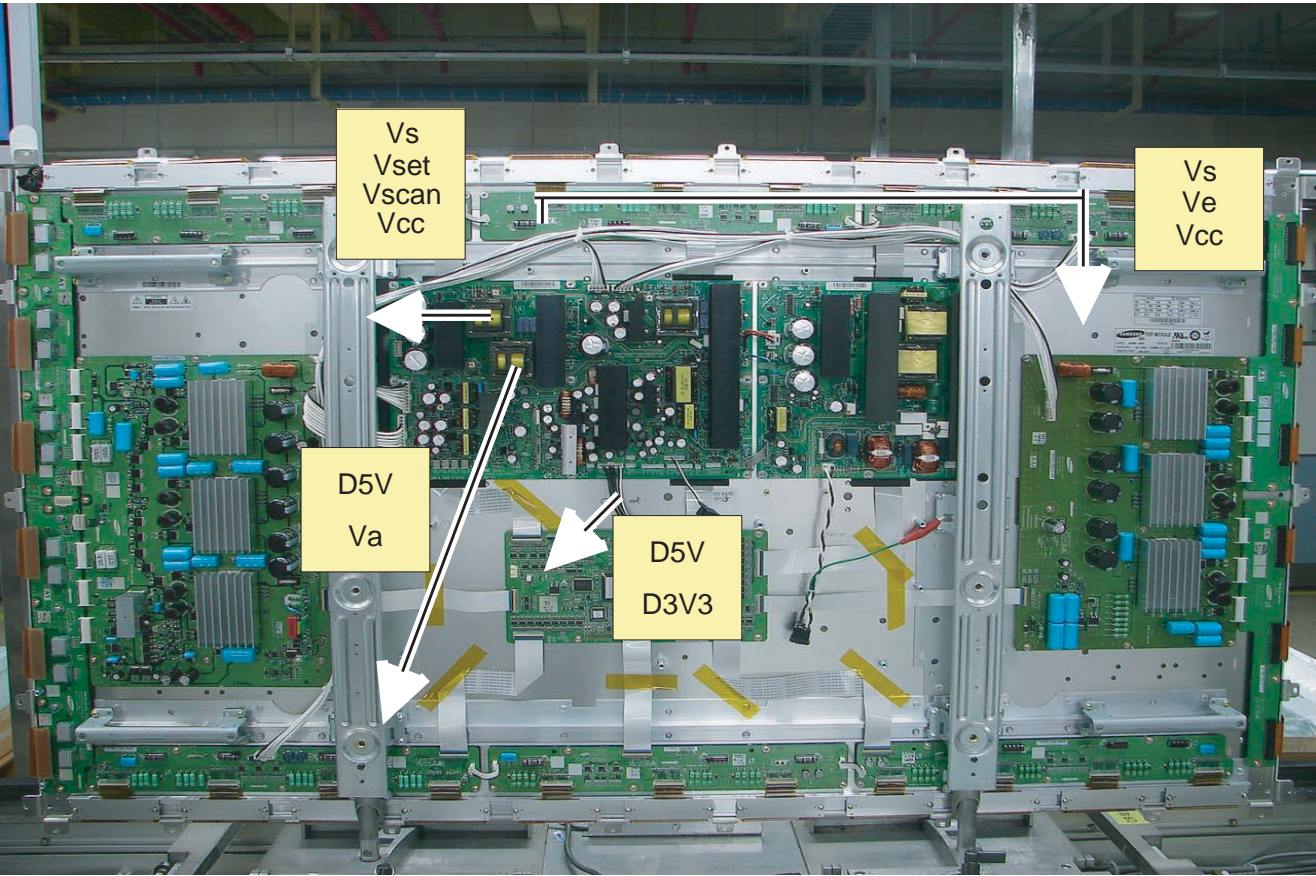
Figure 8-10 Location of the test points for the supply voltages - 50" HD w1

8.1.6 Adjustment Power Supply Voltages 63" HD v4

Table 8-4 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	Vs	184 V ± 1 %	165 V ~ 190 V
2	Va	72 V ± 1.5 %	60 V ~ 85 V
3	Ve	88 V ± 1.5 %	80 V ~ 110 V
4	Vset	178 V ± 1.5 %	160 V ~ 200 V
5	Vscan	-160 V ± 1.5 %	-190 V ~ -155 V
6	Vsb	5 V ± 5 %	Fixed
7	Vg	15 V ± 5 %	Fixed
8	D5VL	5.3 V ± 5 %	Fixed
9	D3V3	3.4 V ± 5 %	Fixed

Check voltage label on the PDP for correct values.



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Figure 8-11 Location of the supply lines from the PSU to the boards - 63" HD v4

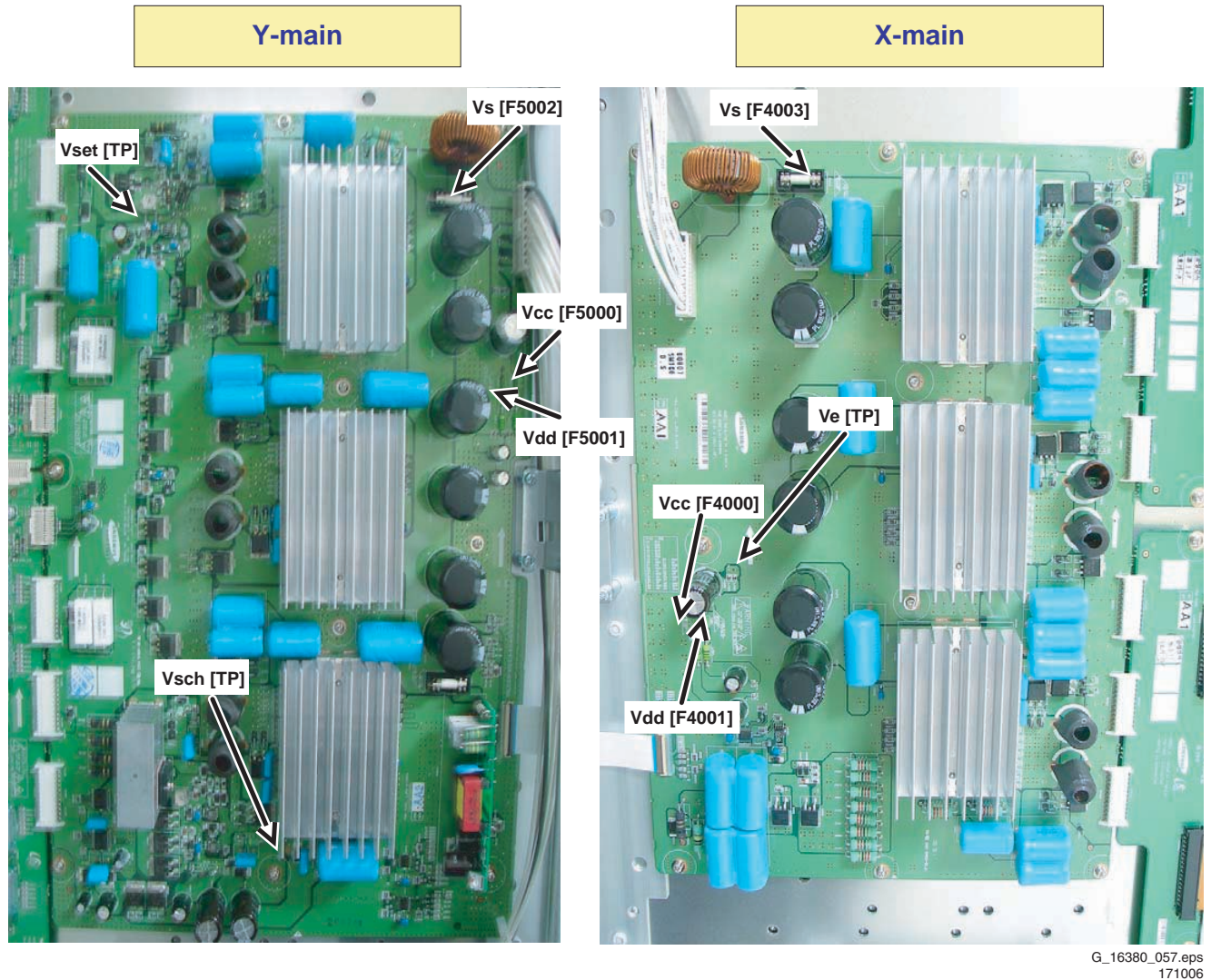
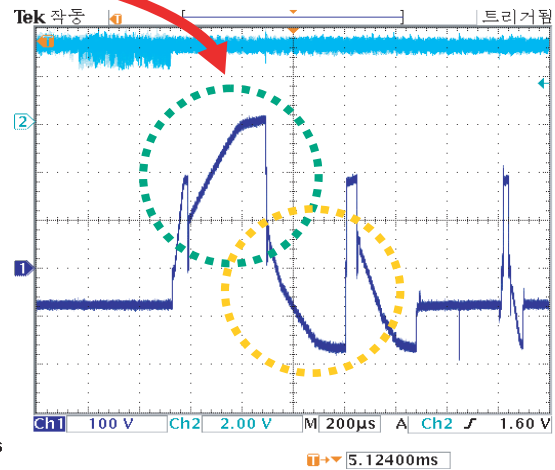
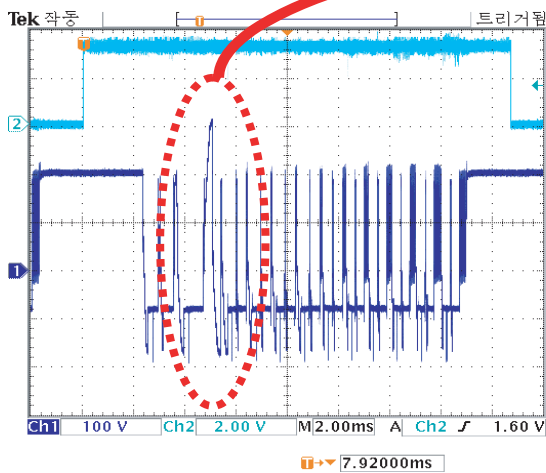


Figure 8-12 Location of the test points for the supply voltages - 63" HD v4

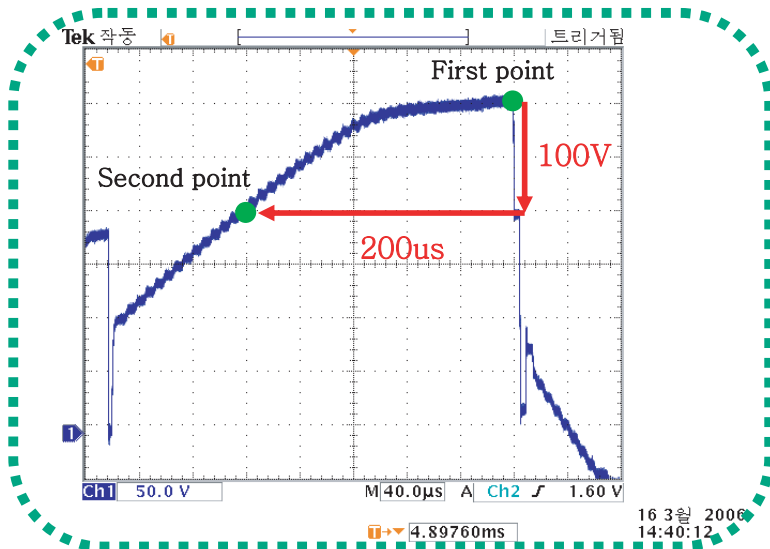
8.2 Waveform Alignments 42" SD v5

1. Set the pattern to Full White (put a jumper on pins 1 and 2 of CN2012 of the Logic Board).
2. Check the waveform using an Oscilloscope.
 - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
 - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Subfield waveform of one TV-Field.
 - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
3. Adjust the waveform of the rising ramp with VR5000 (see Figure "Rising ramp waveform adjustment").
4. Adjust the waveform of the falling ramp with VR5001 (see Figure "Falling ramp waveform adjustment").



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Figure 8-13 Waveform adjustment (Y-Board) - 42 SD v5

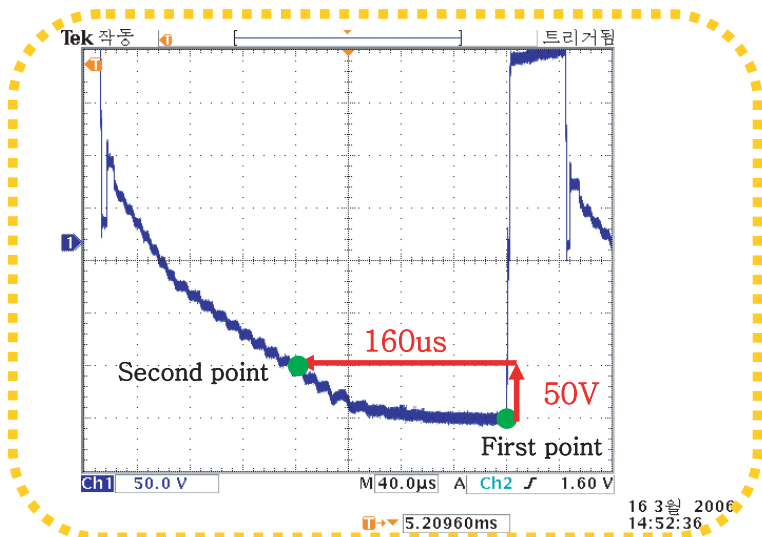


<Rising ramp>

The second point is located 100 V below and 200 usec before the first point.

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Figure 8-14 Rising ramp waveform (Y-Board) - 42 SD v5



<Falling ramp>

The second point is located 50 Volt above and 160 usec before the first point.

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Figure 8-15 Falling ramp flat time adjustment (Y-Board) - 42 SD v5

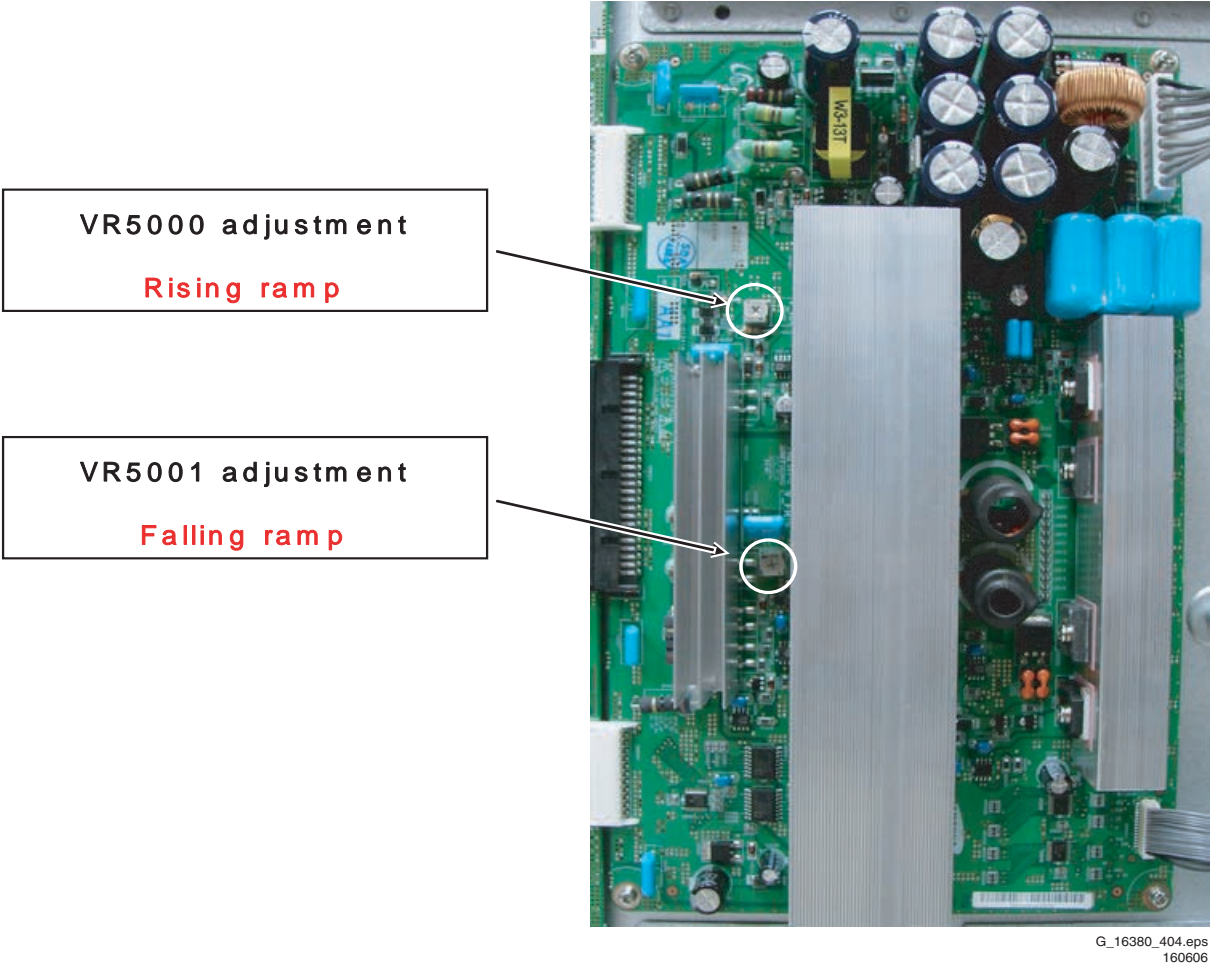


Figure 8-16 Potentiometer locations - 42 SD v5

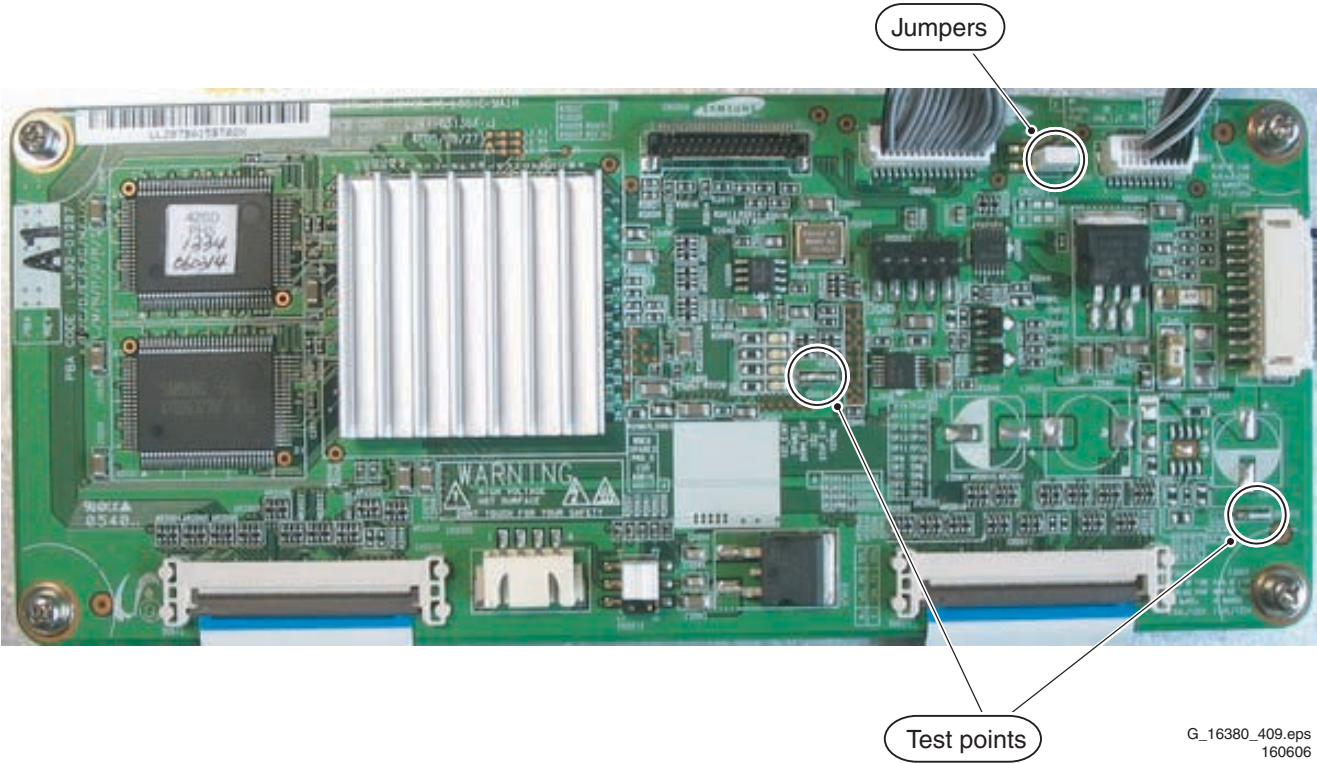


Figure 8-17 Logic PWB - 42 SD v5

8.3 Waveform Alignments 42" HD w1

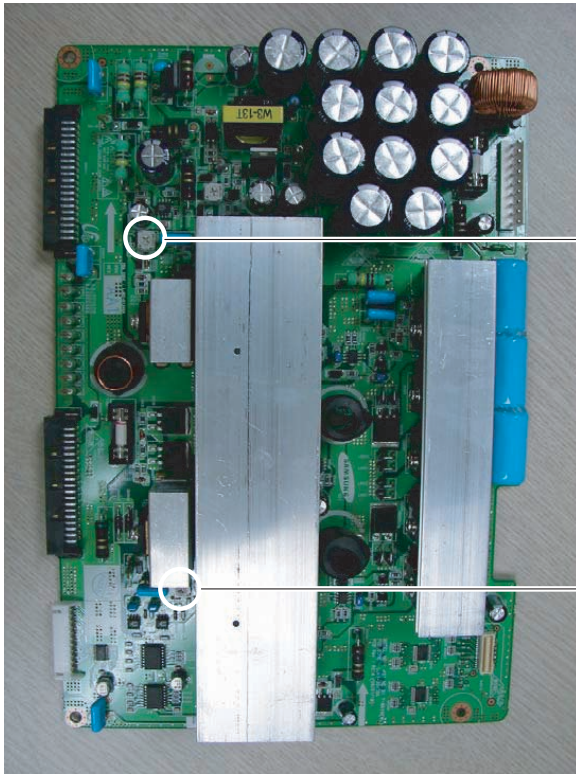
1. Set the pattern to Full White:

- Place jumpers on:
 - J8902 of the PSU alarm board
 - J5003 and J5004 of the PSU
 - Pins 1 and 2 of CN2072 on the Logic Board
- When the display starts showing a cycle of different patterns, push button SW2001 for at least one second. Now the display shows a continuous full white pattern. To restart the cycle of different patterns, push the button once more and wait for a few seconds.

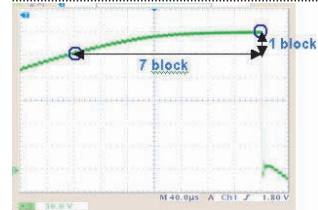
2. Check the waveform using an Oscilloscope.

- Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").

- Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Subfield waveform of one TV-Field.
 - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
 - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
 - Check the Reset waveform when the V_TOGG level is changed.
3. Adjust the waveform of the rising ramp with VR5001 (see Figure "Rising ramp waveform adjustment").
4. Adjust the waveform of the falling ramp with VR5002 (see Figure "Falling ramp waveform adjustment").



VR5001 Adjustment : Rising Ramp
Oscilloscope Setting : 50V / 40us

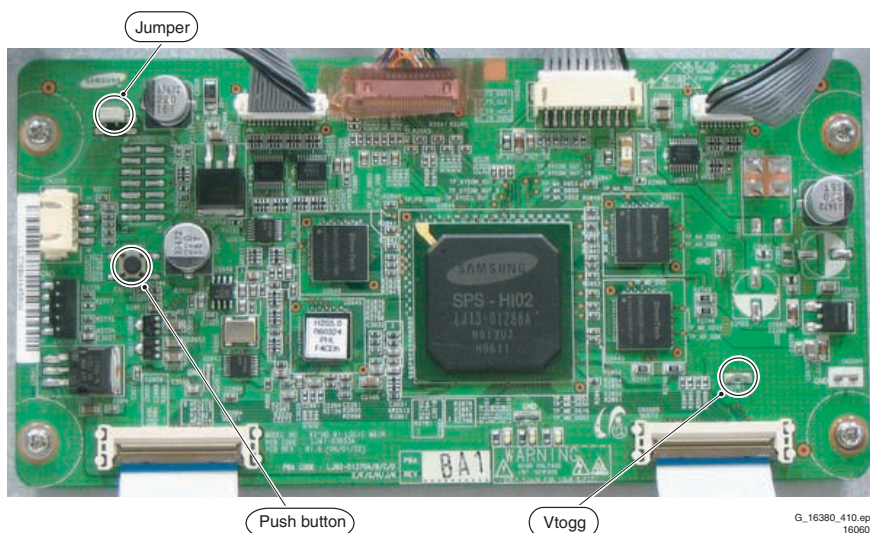


VR5002 Adjustment : Falling Ramp
Oscilloscope Setting : 50V / 40us



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Figure 8-18 Adjusting procedure - 42" HD w1



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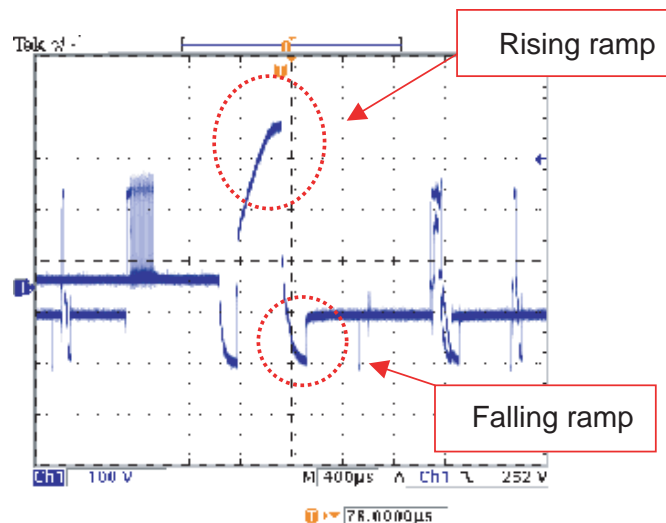
Figure 8-19 Logic PWB - 42 HD w1

8.4 Waveform Alignments 50" HD w1

- Set the pattern to Full White:
 - Place jumpers on:
 - J8902 of the PSU alarm board
 - J5003 and J5004 of the PSU
 - Pin 1 and 2 of CN2072 on the Logic Board
 - When the display starts showing a cycle of different patterns, push button SW2001 for at least one second. Now the display shows a continuous full white pattern. To restart the cycle of different patterns, push the button once more and wait for a few seconds.
- Check the waveform using an Oscilloscope.
 - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
 - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Subfield waveform of one TV-Field.

- Check the waveform by adjusting the Horizontal Division of the oscilloscope.
 - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
 - Check the Reset waveform when the V_TOGG level is changed.
- Adjust the waveform of the rising ramp with VR5001 (see Figure "Rising ramp waveform adjustment").
 - Adjust the waveform of the falling ramp with VR5002 (see Figure "Falling ramp waveform adjustment").

Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the Reset waveform and then move to the 3rd Sub-field for adjusting.



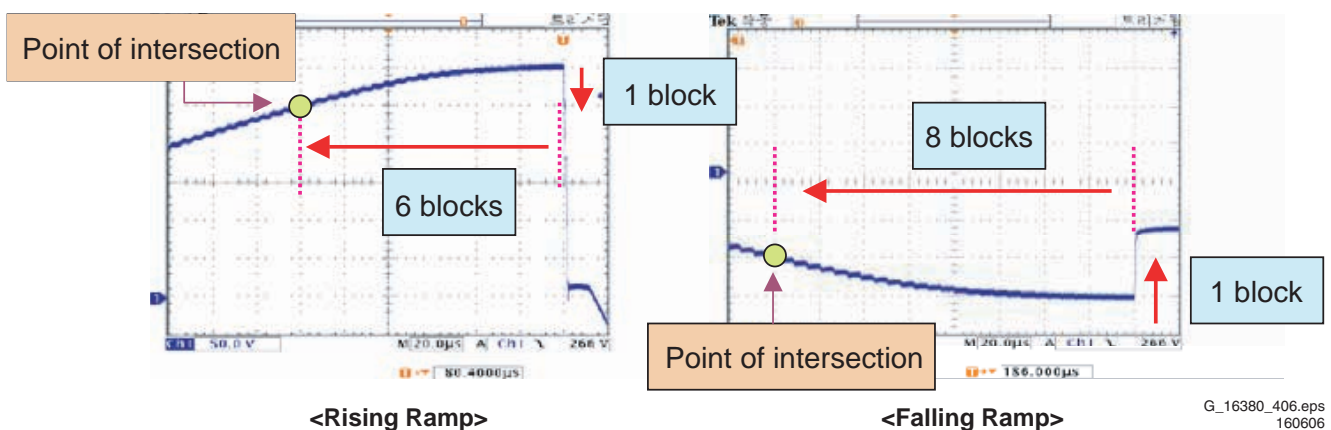
< Main Reset Waveform >

Adjust VR5000 to set the time of Yrr (Main Reset Rising Ramp) like the below picture.

Oscilloscope Setting : 50V / 20us

Adjust VR5001 to set the time of Yfr (Main Reset Falling Ramp) like the below picture.

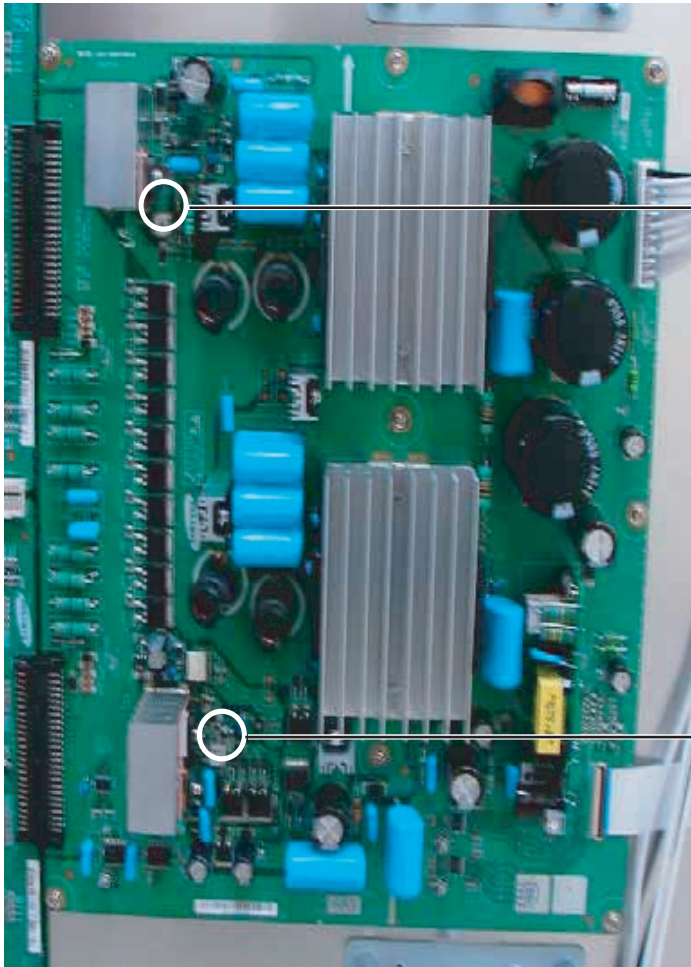
Oscilloscope Setting : 50V / 20us



<Rising Ramp>

<Falling Ramp>

Figure 8-20 TCP ramp waveform inclination adjustment (Y-Board)

**VR5000 Adjustment :**

Adjust VR5000 to set the time of Yrr
(Main Reset Rising Ramp) like the
picture of front page.

Oscilloscope Setting : 50V / 20us

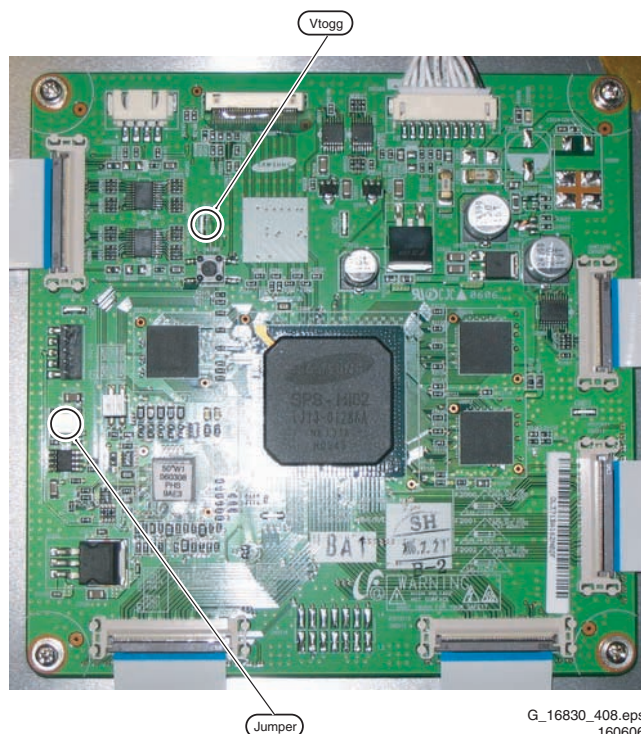
VR5001 Adjustment :

Adjust VR5001 to set the time of Yfr
(Main Reset Falling Ramp) like the
picture of front page.

Oscilloscope Setting : 50V / 20us

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Figure 8-21 Potentiometer locations (Y-Board) - 50 HD w1



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Figure 8-22 Logic Main board - 50 HD w1

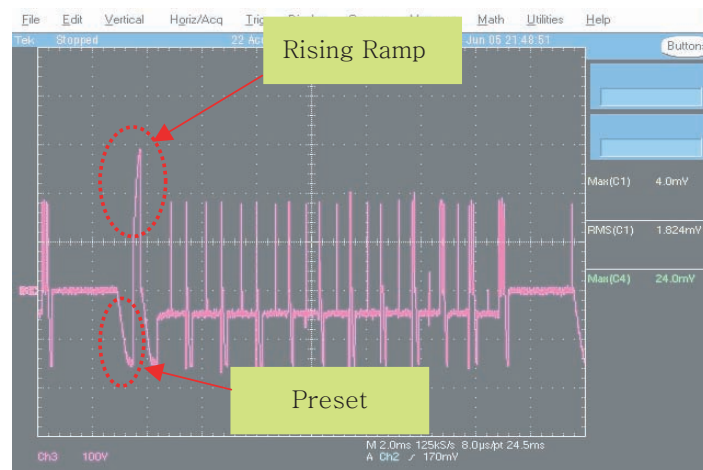
8.5 Waveform Alignments 63" HD v4

1. Set the pattern to Full White:
 - Place a jumper on CN2012 on the Logic Board and switch the display "ON".
2. Check the waveform using an Oscilloscope.
 - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
 - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then

check the first Subfield operating waveform of one TV-Field.

- Check the waveform by adjusting the Horizontal Division of the oscilloscope.
 - Check the Reset waveform when the V_TOGG level is changed.
3. Adjust the intersection point of the rising ramp with VR5000 (see Figure "Rising ramp waveform adjustment").
 4. Adjust the intersection point of the falling ramp with VR5001 (see Figure "Falling ramp waveform adjustment").

W1 Ramp Waveform Inclination Adjustment (Y-Board)



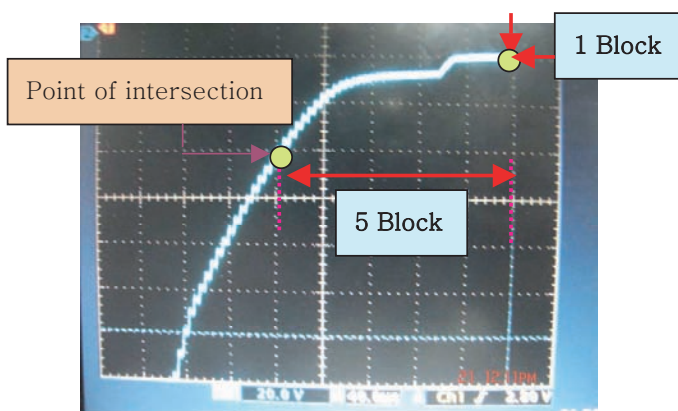
< Main Reset Waveform >

Adjust VR5000 to set the time of Yrr (Main Reset Rising Ramp) like the below picture.

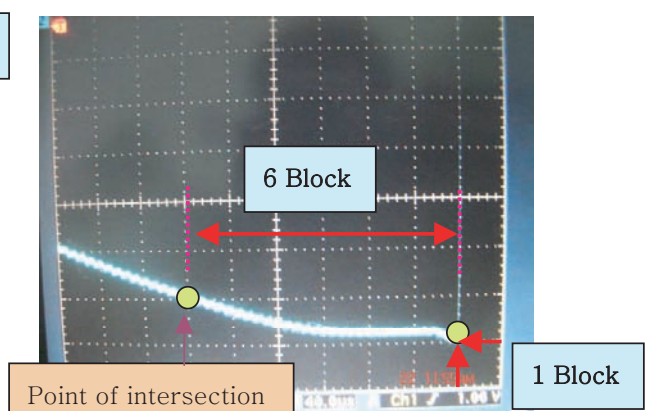
Oscilloscope Setting : 20V / 40us

Adjust VR5001 to set the time of Yfr (Preset) like the below picture.

Oscilloscope Setting : 20V / 40us



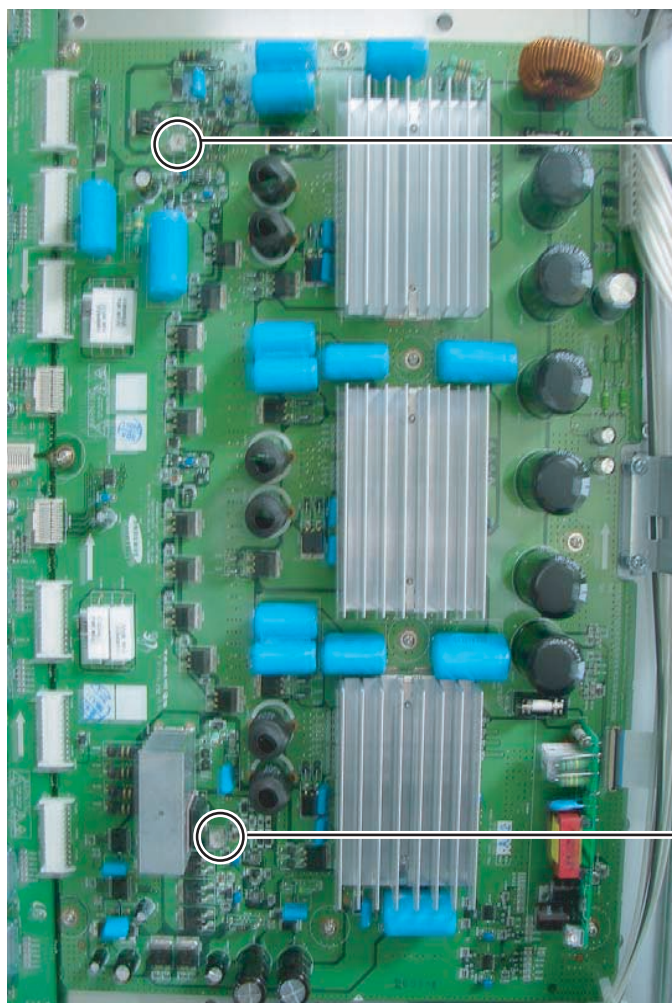
<Rising Ramp>



<Preset>

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181006

Figure 8-23 TCP ramp waveform inclination adjustment (Y-Board)

**VR5000 Adjustment :**

Adjust VR5000 to set the time of Yrr (Main Reset Rising Ramp) like the picture of the previous page.

Oscilloscope Setting : 20V / 40us

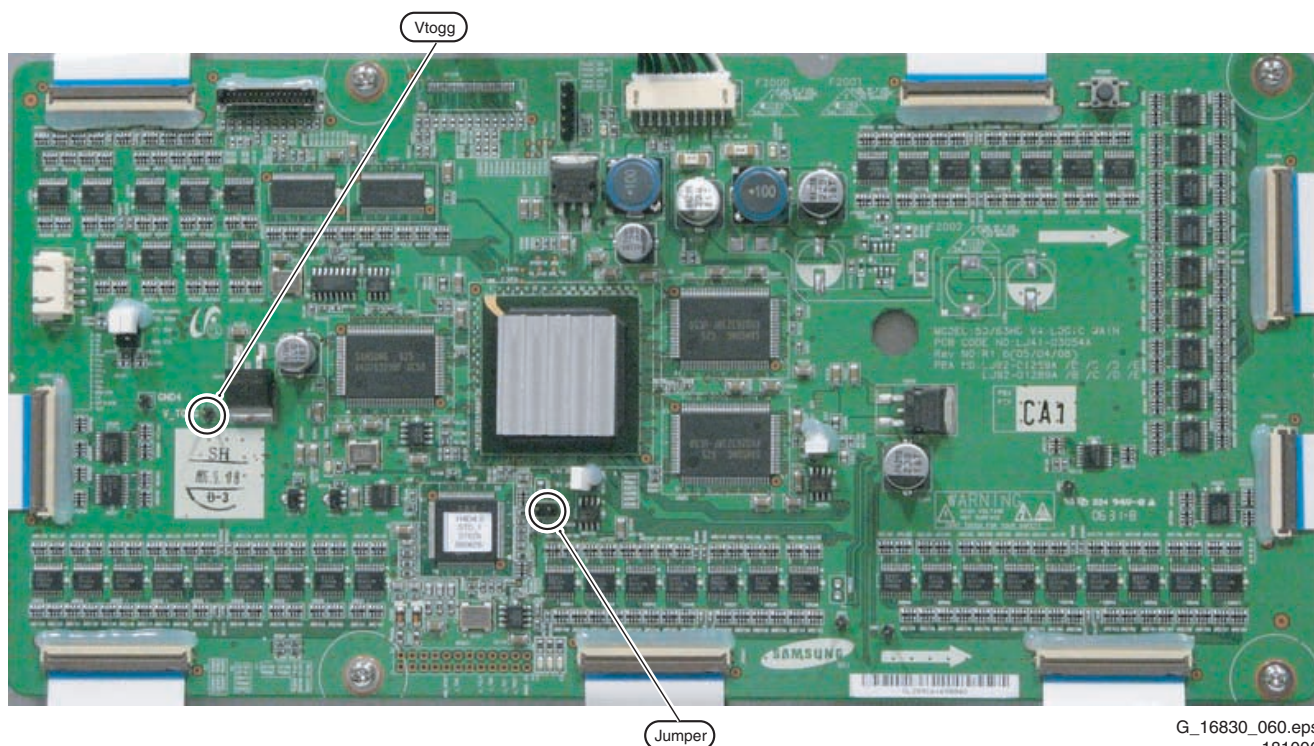
VR5001 Adjustment :

Adjust VR5001 to set the time of Yfr (Preset) like the picture of the previous page.

Oscilloscope Setting : 20V / 40us

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181006

Figure 8-24 Potentiometer locations (Y-Board) - 50 HD w1



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181006

Figure 8-25 Logic Main board - 63" HD v4

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

- 9.1 Main function of Each Assembly
- 9.2 Abbreviation List
- 9.3 IC Data Sheets

9.1 Main function of Each Assembly

9.1.1 X Main Board

The X Main board generates a drive signal by switching the FET in synchronization with logic main board timing, and supplies the X electrode of the panel with the drive signal through the connector.

1. Maintain voltage waveforms (including ERC).
2. Generate X rising ramp signal.
3. Maintain Ve bias between Scan intervals.

9.1.2 Y Main Board

The Y Main board generates a drive signal by switching the FET in synchronization with the logic Main Board timing and sequential supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

1. Maintain voltage waveforms (including ERC).
2. Generate Y-rising Falling Ramp.
3. Maintain V scan bias.

9.1.3 Logic Main Board

The Logic Main board generates and outputs the address drive output signal and the X,Y drive signal by processing the video signals. This Board buffers the address drive output signal and feeds it to the address drive IC (COF module, video signal- X Y drive signal generation, frame memory circuit / address data rearrangement).

9.1.4 Logic Buffer (E, F)

The Logic Buffer transmits data signal and control signal.

9.1.5 Y Buffer Board (Upper, Lower)

The Y Buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises eight scan driver ICs (ST microelectronics STV 7617: 64 or 65 output pins), but four ICs for the SD class.

9.1.6 AC Noise Filter

The AC Noise filter has function for removing noise (low frequency) and blocking surge. It affects safety standards (EMC, EMI).

9.1.7 TCP (Tape Carrier Package)

The TCP applies the Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise four data driver ICs (STV7610A: 96 pins output pins). Seven TCPs are required for signal scan.

9.2 Abbreviation List

AC	Alternating Current
COF	Circuit On Foil
DC	Direct Current
ERC	Energy Recovery Circuit
ESD	Electro Static Discharge
FET	Field Effect Transistor
FFC	Flat Foil Cable
FPC	Flexible Printed Circuit
FTV	Flat TeleVision
HD	High Definition
I/O	Input/Output
IC	Integrated Circuit
LB	Logic Buffer
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signalling
PCB	Printed Circuit Board (same as PWB)
PDP	Plasma Display Panel
PSU	Power Supply Unit
PWB	Printed Wiring Board (same as PCB)
RGB	Red, Green, Blue colour space
SD	Standard Definition
SDI	Samsung Display Industry (supplier)
SMPS	Switched Mode Power Supply
SSB	Small Signal Board
SF	Sub Field
TCP	Tape Carrier Package
VR	Variable Resistor
Vsc	Scan Voltage
YBL	Y Buffer Lower board
YBU	Y Buffer Upper board
YM	Y Main board

9.3 IC Data Sheets

Not applicable.

10. Spare Parts List

- Notes;
- Determine the SDI part / model number of the PDP.

Find the SDI part number on the actual board to be replaced.

SDI part numbers begin with “LJ92”, except for the SMPS the part number begins with “LJ44”.

Find the SDI board part number in the spare parts overview.

Find the SDI part number in this overview that matches the part number that is actually on the original board.

Cross the SDI board part number to the Philips part number.

Order the Philips part number.

Note: The appearance of a leaded and lead-free board can be different; the colour of the PWB and also the layout of the components are sometimes different.
-
- Figure 10-1 Lead-free logo SDI
- Table 10-1 Spare parts overview
- | PDP type | 42 SD v5 | | 42 HD w1 | | 50 HD w1 | | 63 HD v4 | |
|---|----------------|----------------|----------------|----------------|----------------|-----------------|----------------|-----------------|
| PDP 12 NC | 9322 233 14682 | | 9322 240 08682 | | 9322 240 25682 | | 9322 246 18682 | |
| PDP model type and version | S42SD-YD09 | PP42SD-019A | S42AX-YD02 | PP42AX-009A | S50HW-YD01 | PP50HW-010A | S63HW-YD05 | PP63HW-005A |
| | | | | | | | | |
| BOARDS | SDI part # | 12NC | SDI part # | 12NC | SDI part # | 12NC | SDI part # | 12NC |
| Logic-Buffer (E) | LJ92-01322B | 9965 000 37577 | LJ92-01343A | 9965 000 36813 | LJ92-01372A | 9965 000 36826 | LJ92-01193A | 9965 000 42586 |
| Logic-Buffer (F) | LJ92-01323B | 9965 000 37608 | LJ92-01342A | 9965 000 36814 | LJ92-01373A | 9965 000 36827 | LJ92-01194A | 9965 000 42587 |
| Logic-Buffer (G) | - | - | - | - | LJ92-01374A | 9965 000 36828- | LJ92-01195A | 9965 000 42588- |
| Y-Buffer | LJ92-01339A | 9965 000 36812 | LJ92-01344A | 9965 000 36819 | - | - | - | - |
| Y-Buffer (up) | - | - | - | - | LJ92-01276C | 9965 000 36824 | LJ92-01437A | 9965 000 42589 |
| Y-Buffer (down) | - | - | - | - | LJ92-01277C | 9965 000 36825 | LJ92-01438A | 9965 000 42590 |
| Logic-Board | LJ92-01287C | 9965 000 37576 | LJ92-01370B | 9965 000 36815 | LJ92-01371B | 9965 000 36820 | LJ92-01289C | 9965 000 36820 |
| X-Main Board | LJ92-01340A | 9965 000 36810 | LJ92-01345A | 9965 000 36817 | LJ92-01388A | 9965 000 36822 | LJ92-01385A | 9965 000 42594 |
| Y-Main Board | LJ92-01341A | 9965 000 36811 | LJ92-01346A | 9965 000 36818 | LJ92-01391A | 9965 000 36823 | LJ92-01386A | 9965 000 42595 |
| SMPS (PSU) | LJ44-00101C | 9965 000 33880 | LJ44-00117A | 9965 000 36816 | LJ44-00118A | 9965 000 36821 | LJ44-00123A | 9965 000 42596 |
| SMPS (Sub PSU) | - | - | - | - | - | - | LJ44-00124A | 9965 000 42597 |
| X-Buffer (up) | - | - | - | - | - | - | LJ92-01375A | 9965 000 42591 |
| X-Buffer (down) | - | - | - | - | - | - | LJ92-01376A | 9965 000 42592 |
| | | | | | | | | |
| CABLES + CONNECTORS | SDI part # | 12NC | SDI part # | 12NC | SDI part # | 12NC | SDI part # | 12NC |
| Cable-flat Logic + Y-Main | LJ39-00164A | 9965 000 37609 | LJ39-00265A | 9965 000 37612 | 3809-001789 | 9965 000 37614 | 3809-001546 | 996500042799 |
| Cable-flat Logic + X-Main | LJ39-00252A | 9965 000 37610 | LJ39-00264A | 9965 000 37613 | 3809-001788 | 9965 000 37615 | 3809-001695 | 996500042800 |
| Cable-flat Logic + Logic Buf (E) | 3809-001791 | 9965 000 37611 | 3809-001629 | 9965 000 37617 | 3809-001771 | 9965 000 37618 | - | - |
| Cable-flat Logic + Logic Buf (F) | 3809-001791 | 9965 000 37611 | 3809-001629 | 9965 000 37617 | 3809-001771 | 9965 000 37618 | - | - |
| Cable-flat Logic + Logic Buf (G) | - | - | - | - | 3809-001790 | 9965 000 37616 | - | - |
| Cable-flat Logic + Logic Buf (E) upper | - | - | - | - | - | - | 3809-001743 | 996500042801 |
| Cable-flat Logic + Logic Buf (F) upper | - | - | - | - | - | - | 3809-001742 | 996500042802 |
| Cable-flat Logic + Logic Buf (G) upper | - | - | - | - | - | - | 3809-001745 | 996500042803 |
| Cable-flat Logic + Logic Buf (E) lower | - | - | - | - | - | - | 3809-001744 | 996500042804 |
| Cable-flat Logic + Logic Buf (F) lower | - | - | - | - | - | - | 3809-001741 | 996500042805 |
| Cable-flat Logic + Logic Buf (G) lower | - | - | - | - | - | - | 3809-001768 | 996500042806 |
| Connector Logic Buf (E)+Logic Buf (F) | LJ39-00202A | 9965 000 37619 | LJ39-00259A | 9965 000 37623 | LJ39-00257A | 9965 000 37627 | LJ39-00215A | 996500042807 |
| Connector Logic Buf (F)+Logic Buf (G) | - | - | - | - | LJ39-00257A | 9965 000 37627 | LJ39-00215A | 996500042807 |
| Connector SMPS + Logic Buf (E) | LJ39-00256A | 9965 000 37620 | LJ39-00241A | 9965 000 37624 | LJ39-00266A | 9965 000 37628 | - | - |
| Connector SMPS + Logic Buf (E) upper | - | - | - | - | - | - | LJ39-00234A | 996500042808 |
| Connector SMPS + Logic Buf (E) lower | - | - | - | - | - | - | LJ39-00184A | 996500042809 |
| Connector SMPS + Logic Main | LJ39-00209A | 9965 000 37621 | LJ39-00155A | 9965 000 37625 | LJ39-00266A | 9965 000 37628 | LJ39-00293A | 996500042810 |
| Connector SMPS + Y-Main | LJ39-00263A | 9965 000 37626 | LJ39-00263A | 9965 000 37626 | LJ39-00221A | 9965 000 37629 | LJ39-00239A | 996500042811 |
| Connector SMPS + X-Main | LJ39-00262A | 9965 000 37622 | LJ39-00262A | 9965 000 37622 | LJ39-00220A | 9965 000 37630 | LJ39-00185A | 996500042812 |
| | | | | | | | | |
| CTN / Chassis | CTN | Chassis | CTN | Chassis | CTN | Chassis | CTN | Chassis |
| Sets/Chassis in which this PDP type is used (this list is for indicative purposes only, we do not pretend it is complete) | 42PF5521D/10 | LC4.41E AB | 42PF9431D/37 | BJ2.5U PA | 50PF9631D/37 | BJ2.4U PA | 63PF9631D/37 | BJ3.0U PA |
| | 42PF5521D/12 | LC4.41E AB | 42PF9631D/37 | BJ2.4U PA | 50PF9731D/37 | BJ2.4U PA | - | - |

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- Name changed from “SDI PDP Repair Manual” to “SDI PDP 2K6”.
- Model 63” HD v4 added.

Service Service Service

SDI PDP 2K7

S42AX-YD04 (42-inch HD, W2)

S42AX-YD08 (42-inch HD, W2 Plus)

S50HW-YD05 (50-inch HD, W2)

S50HW-YD07 (50-inch HD, W2 Plus)

Service Manual

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1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

- 1.1 PDP Overview
- 1.2 Serial Numbers
- 1.3 Chassis Overview

Notes:

- Figures can deviate due to the different model executions.
- Specifications are indicative (subject to change).

1.1 PDP Overview

Table 1-1 PDP overview

	PDP Type / Version	Model Name	H x V Pixel
1	42" HD W2	S42AX-YD04	1024 x 768
2	42" HD W2 Plus	S42AX-YD08	1024 x 768
3	50" HD W2	S50HW-YD05	1366 x 768
4	50" HD W2 Plus	S50HW-YD07	1365 x 768

1.1.1 42" HD W2

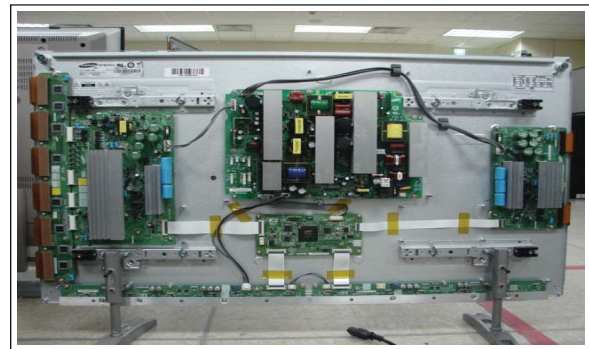


Figure 1-1 Rear view of plasma panel (42" HD W2)

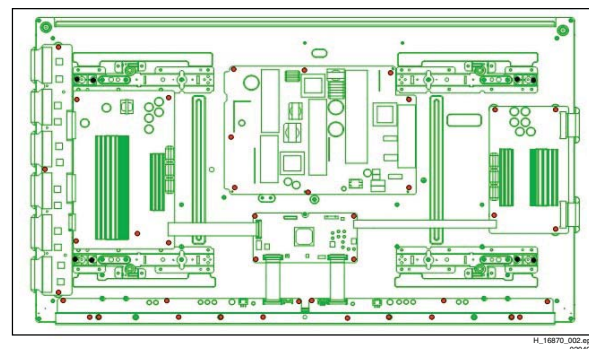


Figure 1-2 Location of mounting screws (42" HD W2)

Note:

- Black dot= screw 4x12 (n= 8).
- Red dot= screw 3x10 (n= 40).
- Screw torque 9.5 ± 0.5 kgf.cm.

No	Item	Specification 42" HD W2	
1	Pixel	1.024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)	
3	Pixel Pitch	0.912mm (H) x 0.693mm (V)	
4	Cell Pitch	R	Horizontal 0.304 mm Vertical 0.693 mm
		G	Horizontal 0.304 mm Vertical 0.693 mm
		B	Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	933.89 (H) x 532.22 (V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	1073.7 million colours (10-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1000 (W) x 588.3 (H) x 65.3 (D) mm	
11	Weight	Module 3	About 17.5 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.2 42" HD W2 Plus

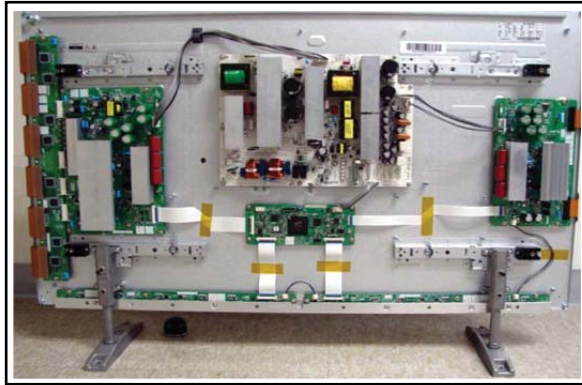
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Figure 1-3 Rear view of plasma panel (42" HD W2 Plus)

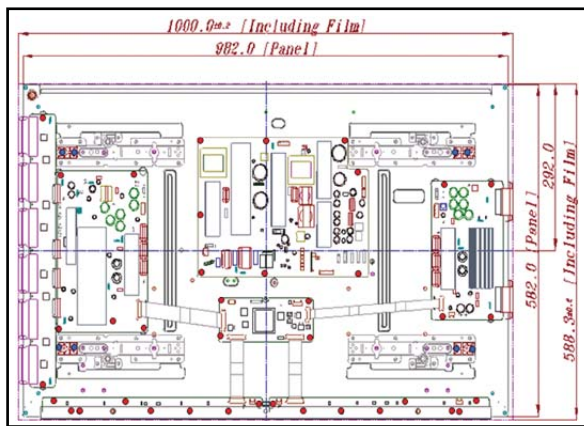
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Figure 1-4 Location of mounting screws (42" HD W2 Plus)

Note:

- Blue dot= screw 4x12 (n= 8).
- Red dot= screw 3x10 (n= 38).
- Screw torque 9.5 ± 0.5 kgf.cm.

No	Item	Specification 42" HD W2 Plus	
1	Pixel	1,024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)	
3	Pixel Pitch	0.912mm (H) x 0.693mm (V)	
4	Cell Pitch	R	Horizontal 0.304 mm Vertical 0.693 mm
		G	Horizontal 0.304 mm Vertical 0.693 mm
		B	Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	933.89 (H) x 532.22 (V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	1073.7 million colours (10-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1000 (W) x 588.3 (H) x 65.3 (D) mm	
11	Weight	Module 3	About 17.5 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.3 50" HD W2

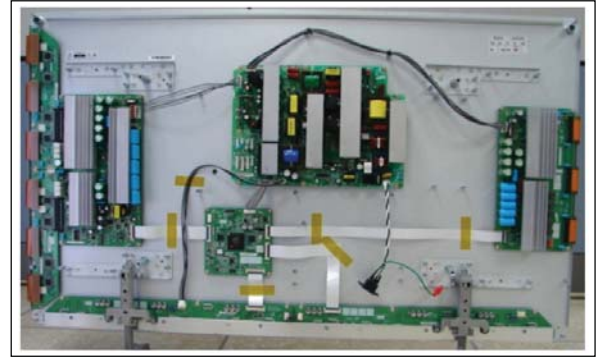
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Figure 1-5 Rear view of plasma panel (50" HD W2)

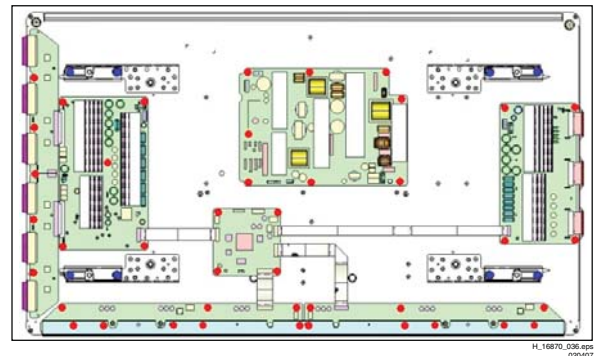
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Figure 1-6 Location of mounting screws (50" HD W2)

Note:

- Blue dot= screw 4x12 (n= 8).
- Red dot= screw 3x10 (n= 42).
- Screw torque 9.5 ± 0.5 kgf.cm.

No	Item	Specification 50" HD W2	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,095 (H) x 768 (V) cells	
3	Pixel Pitch	0.810 mm (H) x 0.810 mm (V)	
4	Cell Pitch	R	Horizontal 0.270 mm Vertical 0.810 mm
		G	Horizontal 0.270 mm Vertical 0.810 mm
		B	Horizontal 0.270 mm Vertical 0.810 mm
5	Display size	1105.65 mm (H) x 622.08 mm (H)	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	1073.7 million colours (10-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1175 (W) x 682 (H) x 63.8 (D) mm	
11	Weight	Module 3	About 24.2 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.4 50" HD W2 Plus

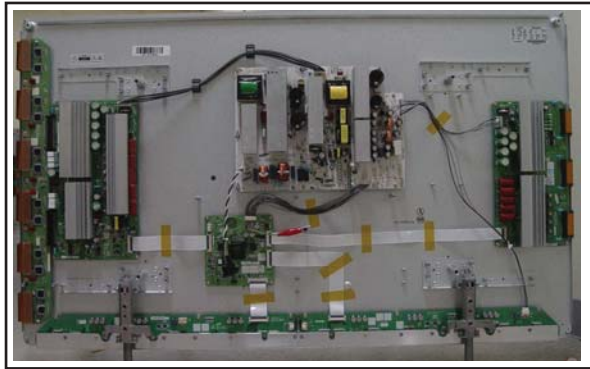
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Figure 1-7 Rear view of plasma panel (50" HD W2 Plus)

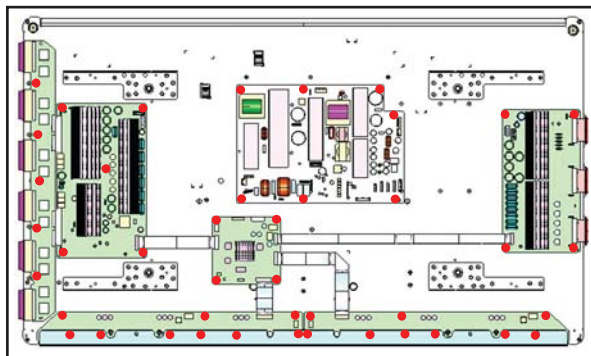
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Figure 1-8 Location of mounting screws (50" HD W2 Plus)

Note:

- Red dot= screw 3x10 (n= 43).
- Screw torque 9.5 ± 0.5 kgf.cm.

No	Item	Specification 50" HD W2 Plus	
1	Pixel	1,365 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4095 (H) x 768 (V)	
3	Pixel Pitch	0.810mm (H) x 0.810mm (V)	
4	Cell Pitch	R	Horizontal 0.270 mm Vertical 0.810 mm
		G	Horizontal 0.270 mm Vertical 0.810 mm
		B	Horizontal 0.270 mm Vertical 0.810 mm
5	Display size	1105.65 (H) x 622.08 (V) mm	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	549.75 billion colours (13-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1175 (W) x 682 (H) x 63.8 (D) mm	
11	Weight	Module 1	About 22.3 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.2 Serial Numbers

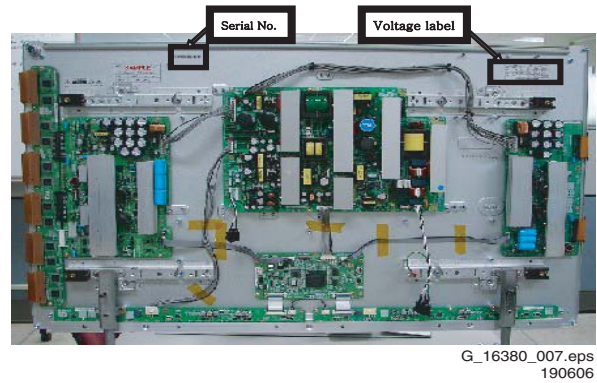
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Figure 1-9 Location of the serial number

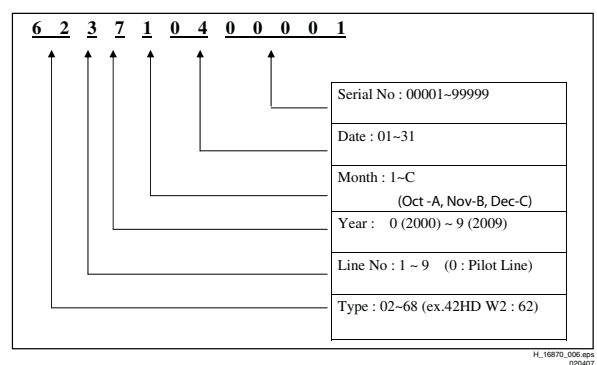
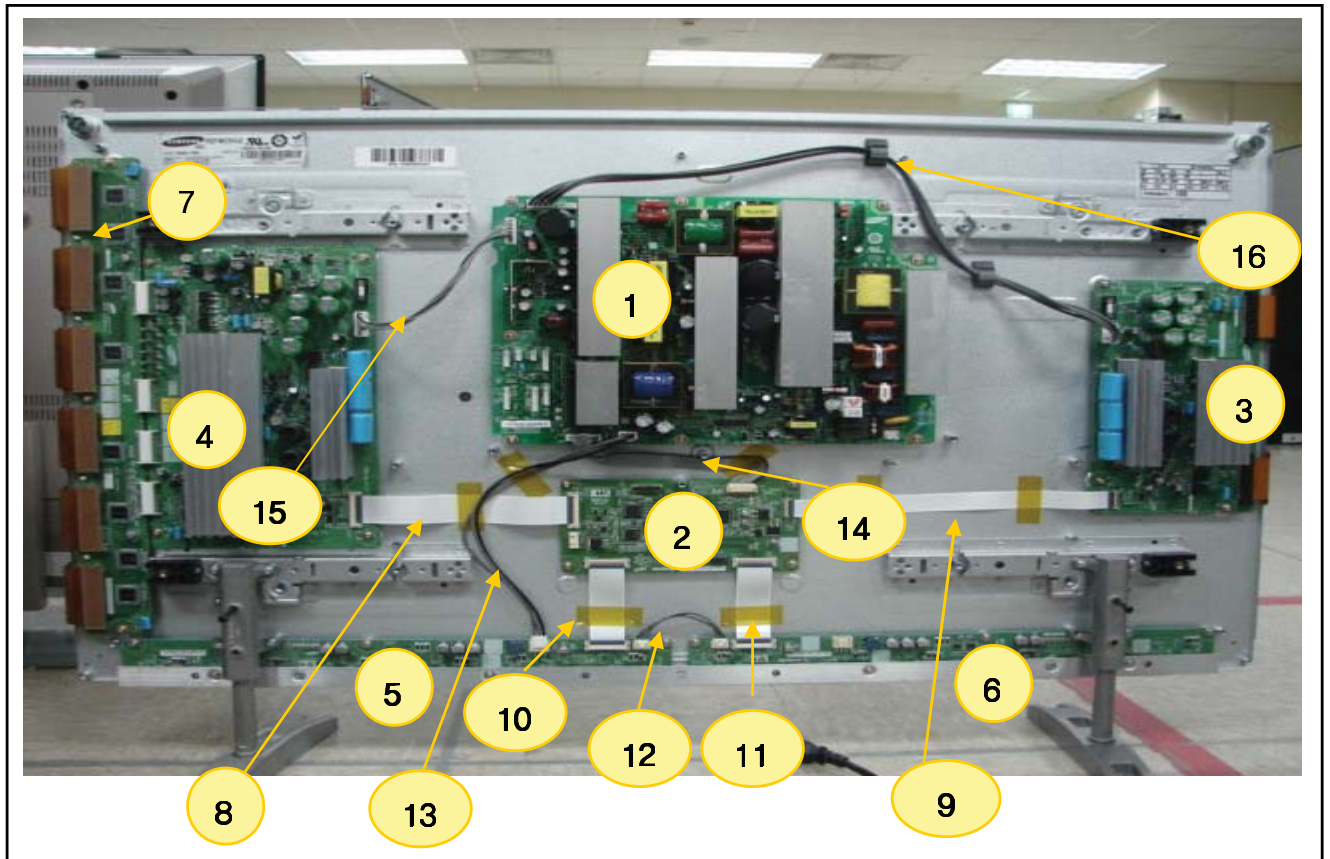
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Figure 1-10 Explanation of the serial number

1.3 Chassis Overview

1.3.1 42" HD W2



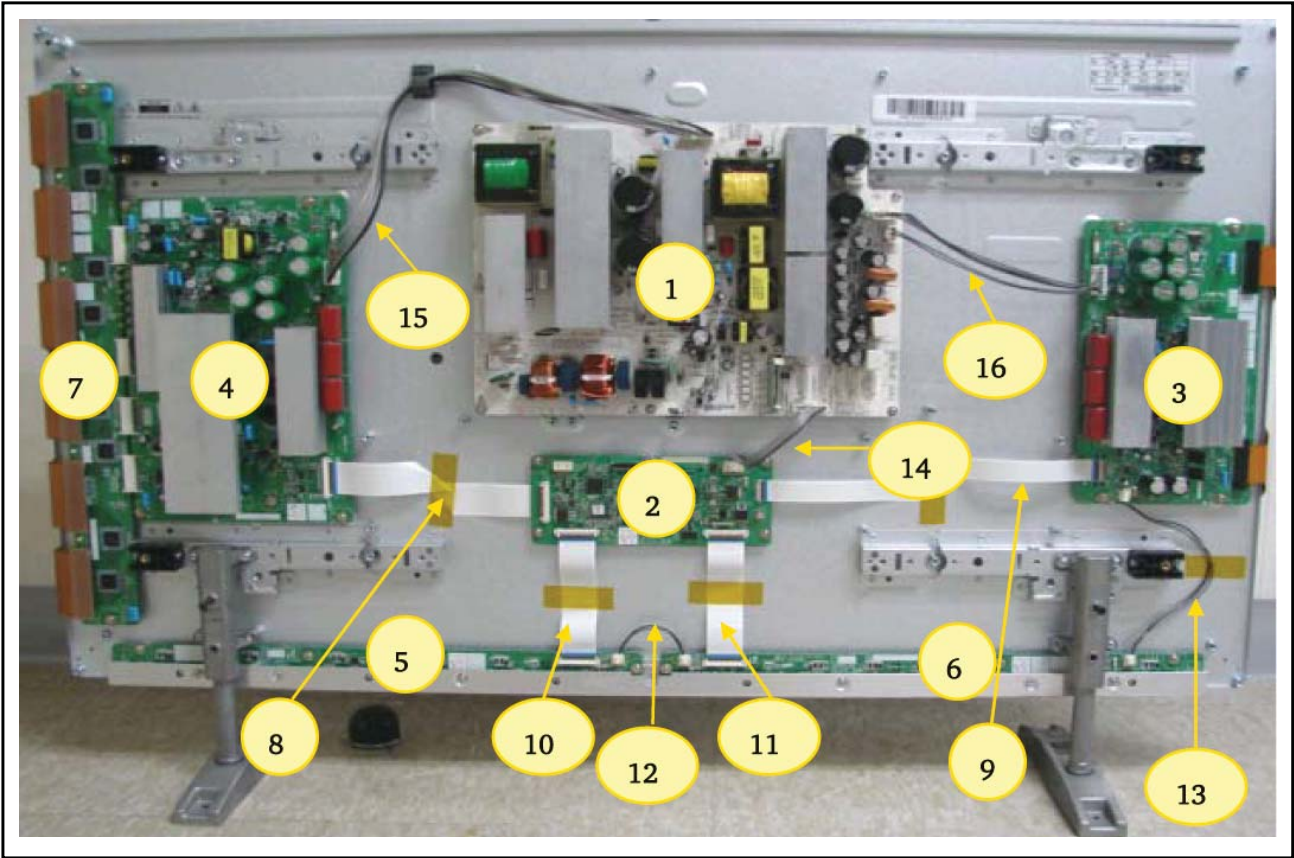
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Figure 1-11 PWB location (42" HD W2)

Table 1-2 PWB overview (42" HD W2)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER Board	Assy PWB Buffer
8	LOGIC + Y-MAIN	FFC Cable-flat
9	LOGIC + X-MAIN	FFC Cable-flat
10	LOGIC + LOGIC BUF(E)	FFC Cable-flat
11	LOGIC + LOGIC BUF(F)	FFC Cable-flat
12	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
13	SMPS + LOGIC BUF(E)	Lead connector
14	SMPS + LOGIC MAIN	Lead connector
15	SMPS + Y-MAIN	Lead connector
16	SMPS + X-MAIN	Lead connector

1.3.2 42" HD W2 Plus



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240807

Figure 1-12 PWB location (42" HD W2 Plus)

Table 1-3 PWB overview (42" HD W2 Plus)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER Board	Assy PWB Buffer
8	LOGIC + Y-MAIN	FFC Cable-flat
9	LOGIC + X-MAIN	FFC Cable-flat
10	LOGIC + LOGIC BUF(E)	FFC Cable-flat
11	LOGIC + LOGIC BUF(F)	FFC Cable-flat
12	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
13	X-MAIN + LOGIC BUF(F)	Lead connector
14	SMPS + LOGIC MAIN	Lead connector
15	SMPS + Y-MAIN	Lead connector
16	SMPS + X-MAIN	Lead connector

1.3.3 50" HD W2

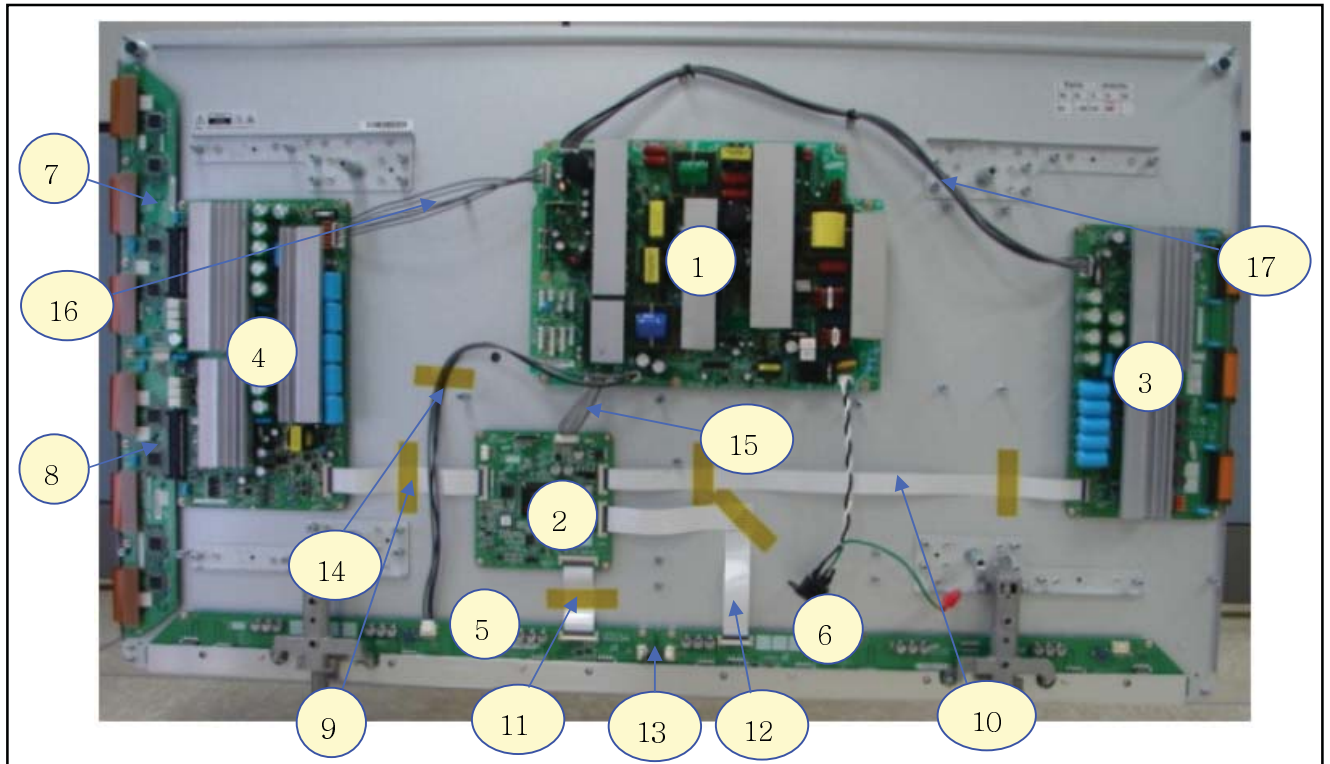
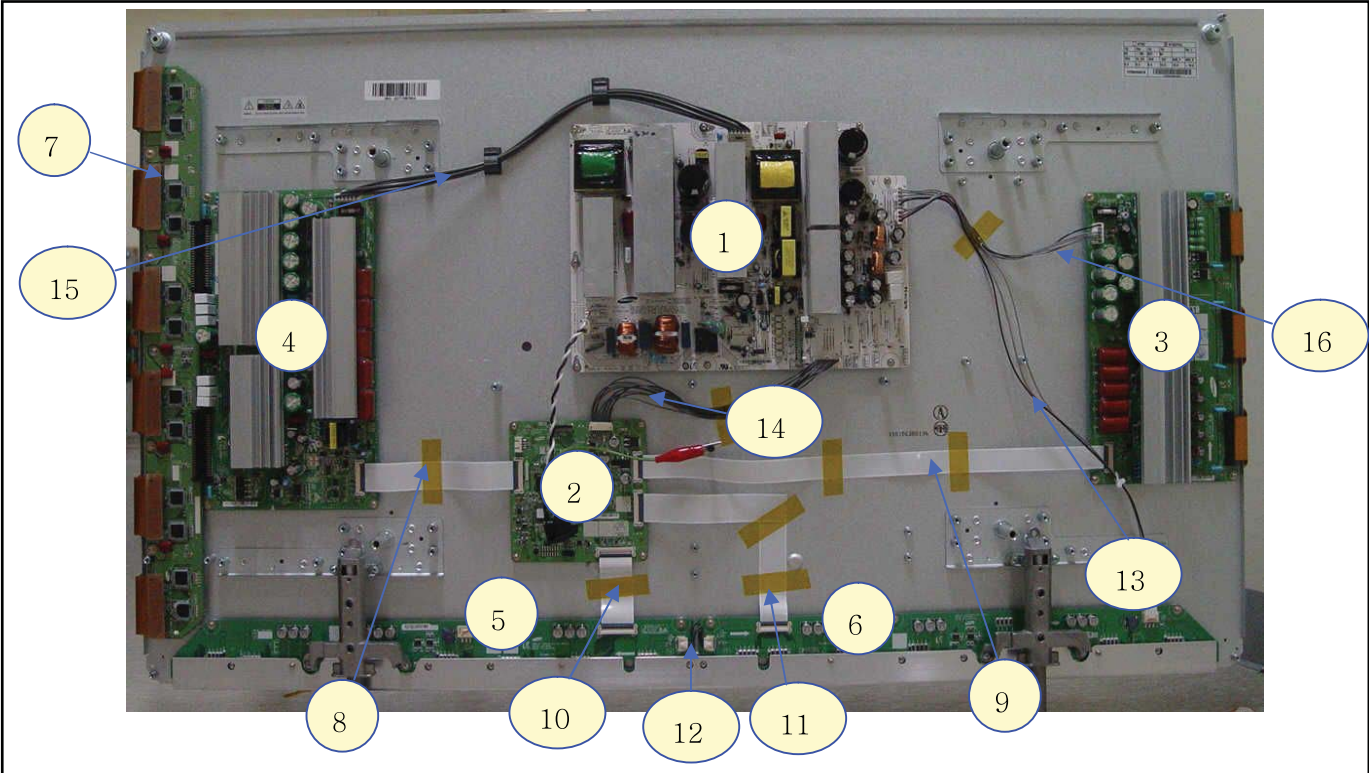
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Figure 1-13 PWB location (50" HD W2)

Table 1-4 PWB overview (50" HD W2)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER (Upper) Board	Assy PWB Buffer
8	Y-BUFFER (Lower) Board	Assy PWB Buffer
9	LOGIC + Y-MAIN	FFC Cable-flat
10	LOGIC + X-MAIN	FFC Cable-flat
11	LOGIC + LOGIC BUF (E)	FFC Cable-flat
12	LOGIC + LOGIC BUF (F)	FFC Cable-flat
13	LOGIC BUF (E) + LOG. BUF (F)	Lead connector
14	SMPS + LOGIC BUF (E)	Lead connector
15	SMPS + LOGIC MAIN	Lead connector
16	SMPS + Y-MAIN	Lead connector
17	SMPS + X-MAIN	Lead connector

1.3.4 50" HD W2 Plus



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Figure 1-14 PWB location (50" HD W2 Plus)

Table 1-5 PWB overview (50" HD W2 Plus)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER UP Board	Assy PWB Buffer
8	LOGIC + Y-MAIN	FFC Cable-flat
9	LOGIC + X-MAIN	FFC Cable-flat
10	LOGIC + LOGIC BUF(E)	FFC Cable-flat
11	LOGIC + LOGIC BUF(F)	FFC Cable-flat
12	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
13	SMPS + LOGIC BUF(F)	Lead connector
14	SMPS + LOGIC MAIN	Lead connector
15	SMPS + Y-MAIN	Lead connector
16	SMPS + X-MAIN	Lead connector

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

- 2.1 Handling Precautions
- 2.2 Safety Precautions
- 2.3 Notes

Notes:

- Only authorised persons should perform servicing of this module.
- When using/handling this unit, pay special attention to the PDP Module: it should not be enforced into any other way than next rules, warnings, and/or cautions.
- **"Warning"** indicates a hazard that may lead to death or injury if the warning is ignored and the product is handled incorrectly.
- **"Caution"** indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

2.1 Handling Precautions

- The PDP module use high voltage that is dangerous to humans. Before operating the PDP, always check for dust to prevent short circuits. Be careful touching the circuit device when power is "on".
- The PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- The PDP module has a lot of electric devices. The service engineer must wear equipment (for example, earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- The PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. The operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is "off". Operator must wait for discharging of remaining voltage during at least 1 minute.

2.2 Safety Precautions

2.2.1 Safety Precautions

- Before replacing a board, discharge forcibly the remaining electricity from the board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.
- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuff including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change: Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, it cause danger on safety. And, if you change the design or insert, manufacturer guarantee will be not effect.
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between

parts and circuit board. Check the cord of AC power preparing damage.

- Product Safety Mark: Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned "off", before next repair.
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

2.2.2 ESD Precautions

There are parts, which are easily damaged by electrostatics (for example Integrated Circuits, FETs, etc.) Electrostatic damage rate of product will be reduced by the following technics:

- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring (it must be operated after removing dust on it. It comes under precaution of electric shock).
- After removing the assembly, lay it with the tracks on a conductive surface to prevent charging.
- Do not use chemical stuff containing Freon. It generates positive electric that can damage ESD sensitive devices.
- You must use a soldering device for ground-tip when soldering or de-soldering these devices.
- You must use anti-static solder removal device. Most removal devices do not have antistatic which can charge a enough positive electric enough for damaging these devices.
- Before removing the protective material from the lead of a new device, bring the protective material into contact with the chassis or assembly.
- When handing an unpacked device for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the device.
- Do not take a new device from the protective case until the it is ready to be installed. Most devices have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminium)

2.3 Notes

A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel, it is recommended to do some maintenance by a qualified service employee only.

2.3.1 Safe PDP Handling

- The work procedures shown with the "Note" indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times, other than when adjusting and checking the product, be sure to turn "off" the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of PWBs, start the servicing work at least 30 seconds after the main power has been turned "off". Especially when installing and removing the Power Supply PWB and the SUS PWB in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned "off".

- While the main power is “on”, do not touch any parts or circuits other than the ones specified. The high voltage Power Supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit PWB, be sure to remove static electricity from your body before handling the circuit PWB.
- Be sure to handle the circuit PWB by holding the large parts as the heat sink or transformer. Failure to observe this

precaution may result in the occurrence of an abnormality in the soldered areas.

- Do not stack the circuit PWB. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original

3. Directions For Use

Not applicable.

4. Mechanical Instructions

Index of this chapter:

- 4.1 Dis-assembling / Re-assembling
 - 4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)
 - 4.1.2 Flat Cable Connector of X-main Board
 - 4.1.3 Assembling & Disassembling FFC and TCP Cables from their Connectors
 - 4.1.4 Exchange of LBE and LBF board - 42" HD W2
 - 4.1.6 Exchange of LBE and LBF board - 50" HD W2
 - 4.1.8 Exchange YB and YM board - 42" HD W2 & 42" HD W2 Plus
 - 4.1.9 Exchange YB and YM board - 50" HD W2 & 50" HD W2 Plus

4.1 Dis-assembling / Re-assembling

4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)

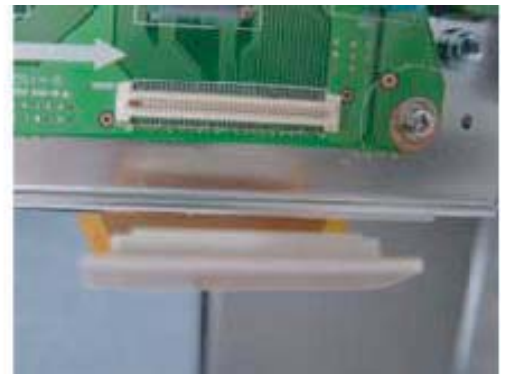
- Dis-assembly: Pull out the FPC from the connector by holding the lead of the FPC with both hands.
- Re-assembly: Push the lead of the FPC with equal force on both sides into the connector.

Note: Be careful not to damage the connector pins during connecting.



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Figure 4-1 Dis-assembly FPC of Y-buffer

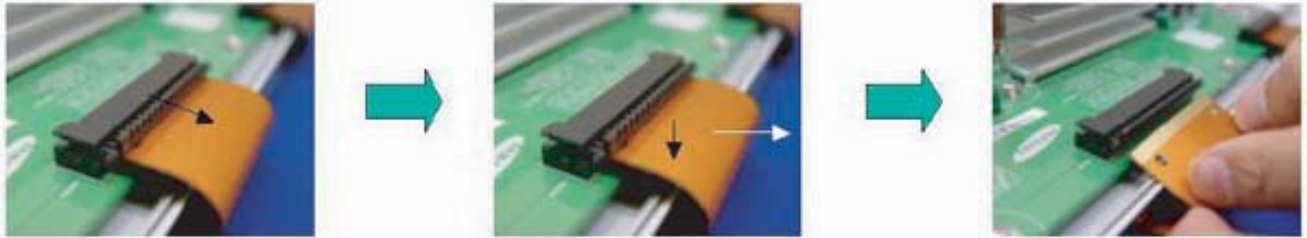


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Figure 4-2 Re-assembly FPC of Y-buffer

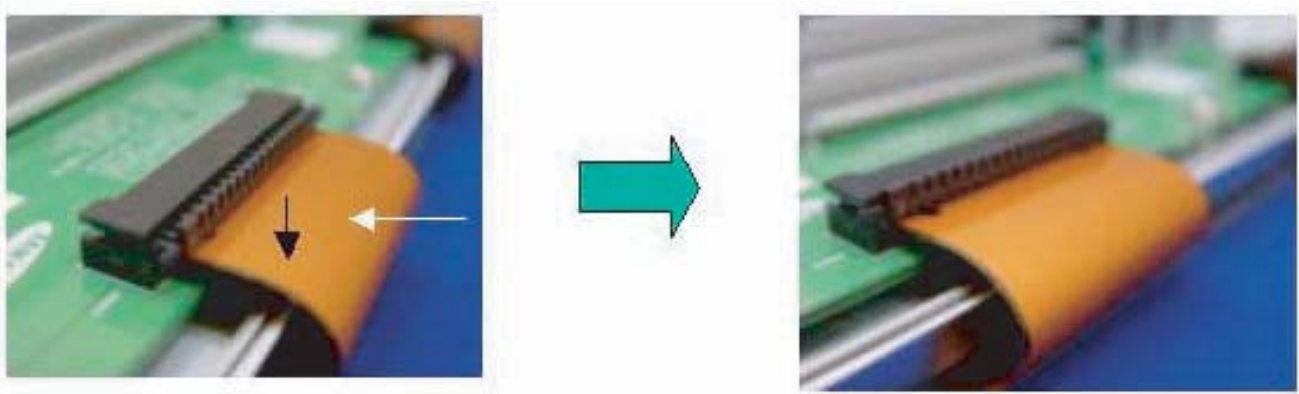
4.1.2 Flat Cable Connector of X-main Board

- Dis-assembly:
 1. Pull out the clamp of the connector.
 2. Pull the Flat cable out, while pressing it down lightly.
- Re-assembly: Insert the Flat Cable into the connector, while pressing it down lightly until you hear a "Click".



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Figure 4-3 Dis-assembly FCC of X-main board



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Figure 4-4 Re-assembly FCC of X-main board

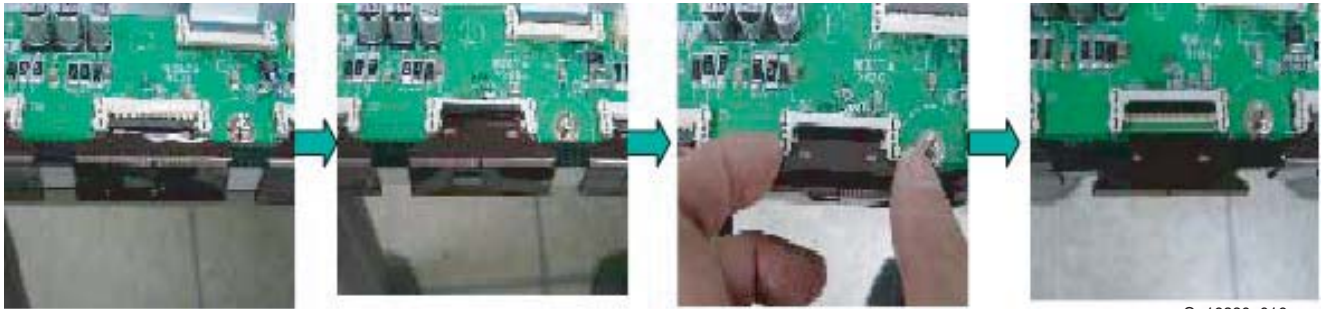
4.1.3 Assembling & Disassembling FFC and TCP Cables from their Connectors

- Dis-assembling of TCP:
 1. Open the clamp carefully.
 2. Pull the TCP out from its connector.
- Re-assembling of TCP:
 1. Put the TCP into the connector carefully

2. Close the clamp completely, until you hear a “Click”.

Notes:

- Carefully check if there is no foreign material on the inside of the connector before inserting the TCP.
- Be careful, do not damage the board by ESD during handling of the TCP.



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Figure 4-5 Dis-assembly of TCP



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Figure 4-6 Re-assembly of TCP



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Figure 4-7 Mis-assembly of TCP



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Figure 4-8 Dis- and re-assembly of FFC

4.1.4 Exchange of LBE and LBF board - 42" HD W2

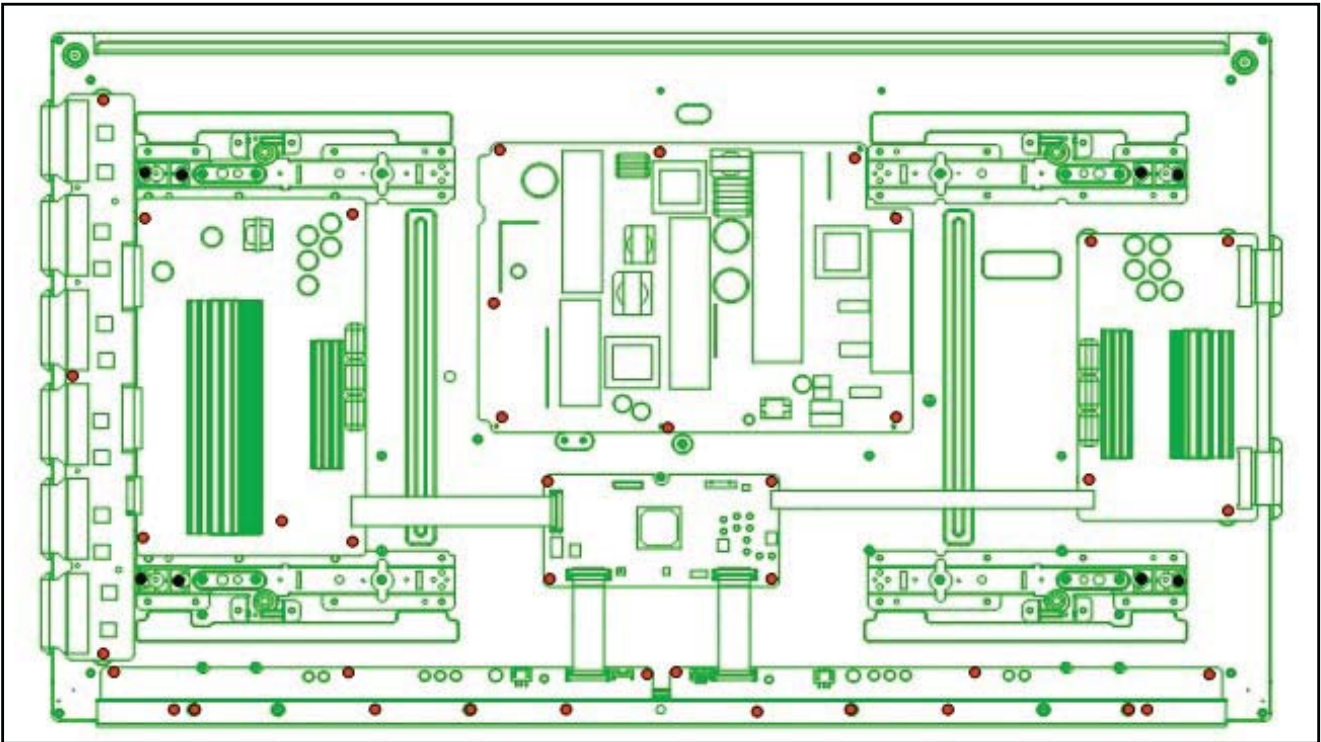
1. Remove the screws in order of 2-3-1-4 from the heatsink and remove the heatsink ("Photos 1 & 3").
2. Remove the TCP, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Place the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the screw mounting order 2-3-1-4.

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.



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Figure 4-9 Photo 1 - Heatsink 42" HD W2



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Figure 4-10 Photo 2 - Exchange of LBE, LBF board 42" HD W2



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Figure 4-11 Photo 3 - Heat sink removal

4.1.5 Exchange of LBE and LBF board - 42" HD W2 Plus

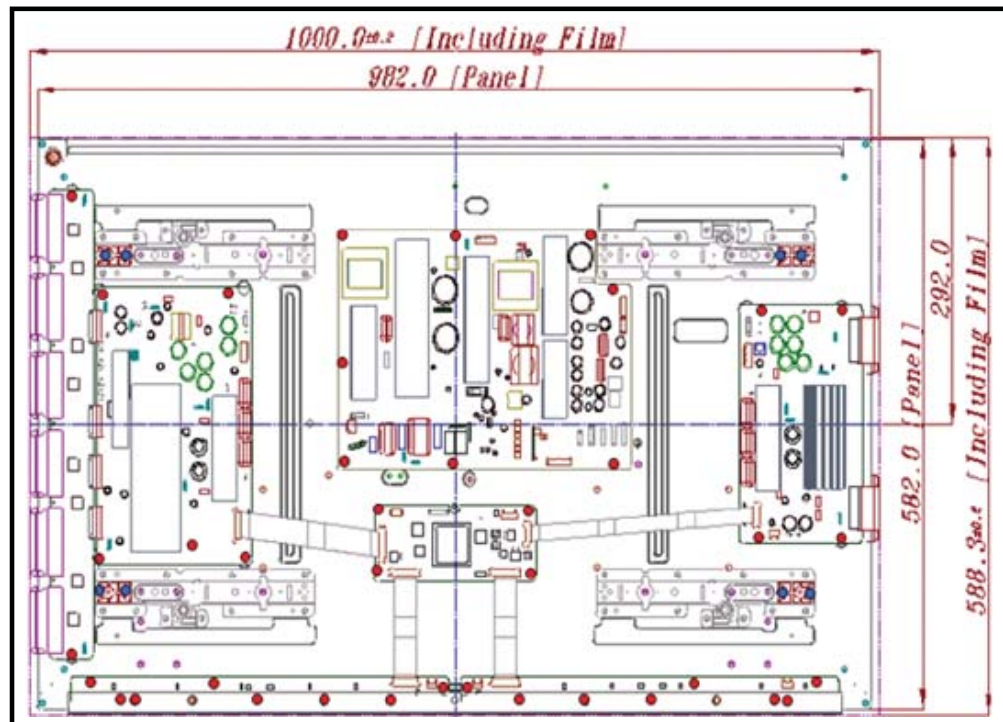
1. Remove the screws in order of 2-3-1-4 from the heatsink and remove the heatsink ("Photos 1 & 3").
2. Remove the TCP, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Place the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the screw mounting order 2-3-1-4.

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.



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Figure 4-12 Photo 1 - Heatsink 42" HD W2 Plus



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Figure 4-13 Photo 2 - Exchange of LBE, LBF board 42" HD W2 Plus



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Figure 4-14 Photo 3 - Heat sink removal

4.1.6 Exchange of LBE and LBF board - 50" HD W2

1. Remove the screws in order of 2-3-1-4 from the heatsink and remove the heatsink ("Photo 1" and "Photo 3").
2. Remove the TCP, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Replace the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the same screw mounting order as described above.

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.



Figure 4-15 Photo 1 - Heatsink 50" HD W2

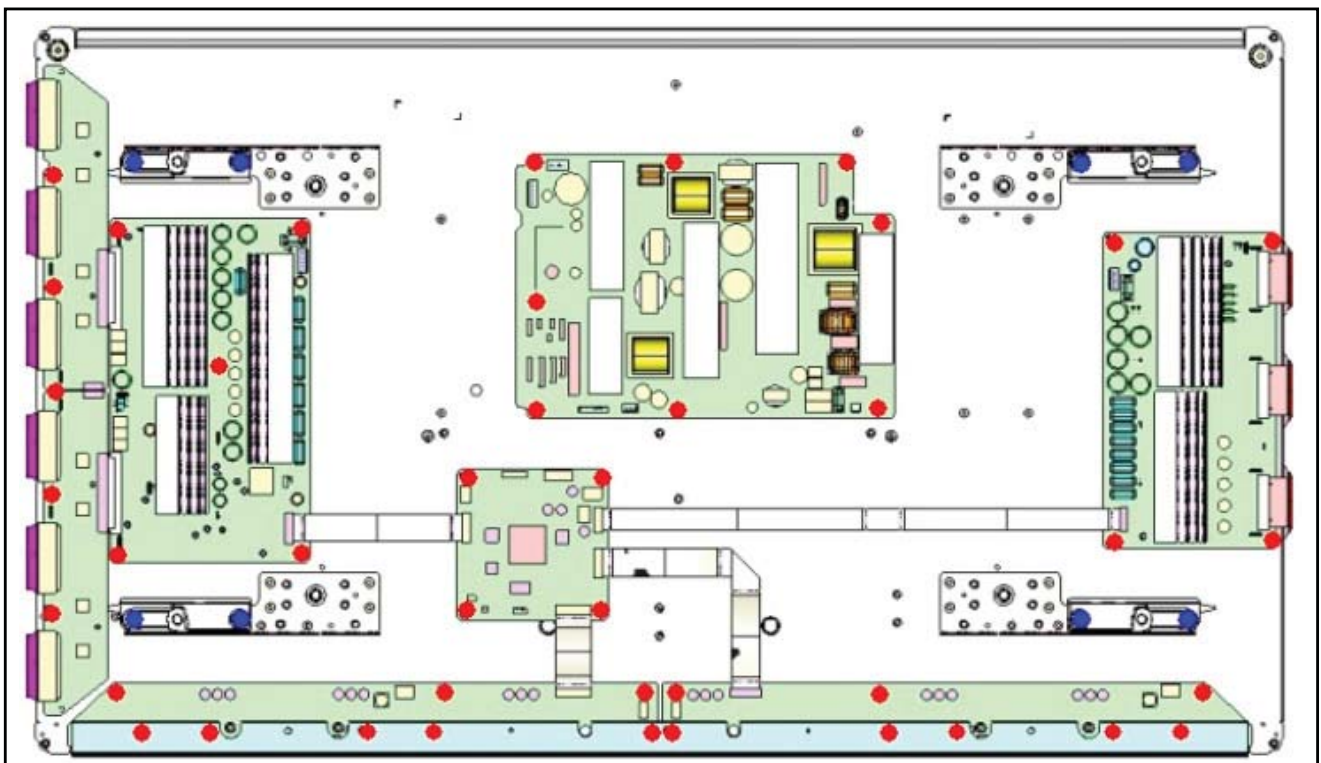


Figure 4-16 Photo 2 - Exchange of LBE and LBF board 50" HD W2



Figure 4-17 Photo 3 - Heat sink removal

4.1.7 Exchange of LBE and LBF board - 50" HD W2 Plus

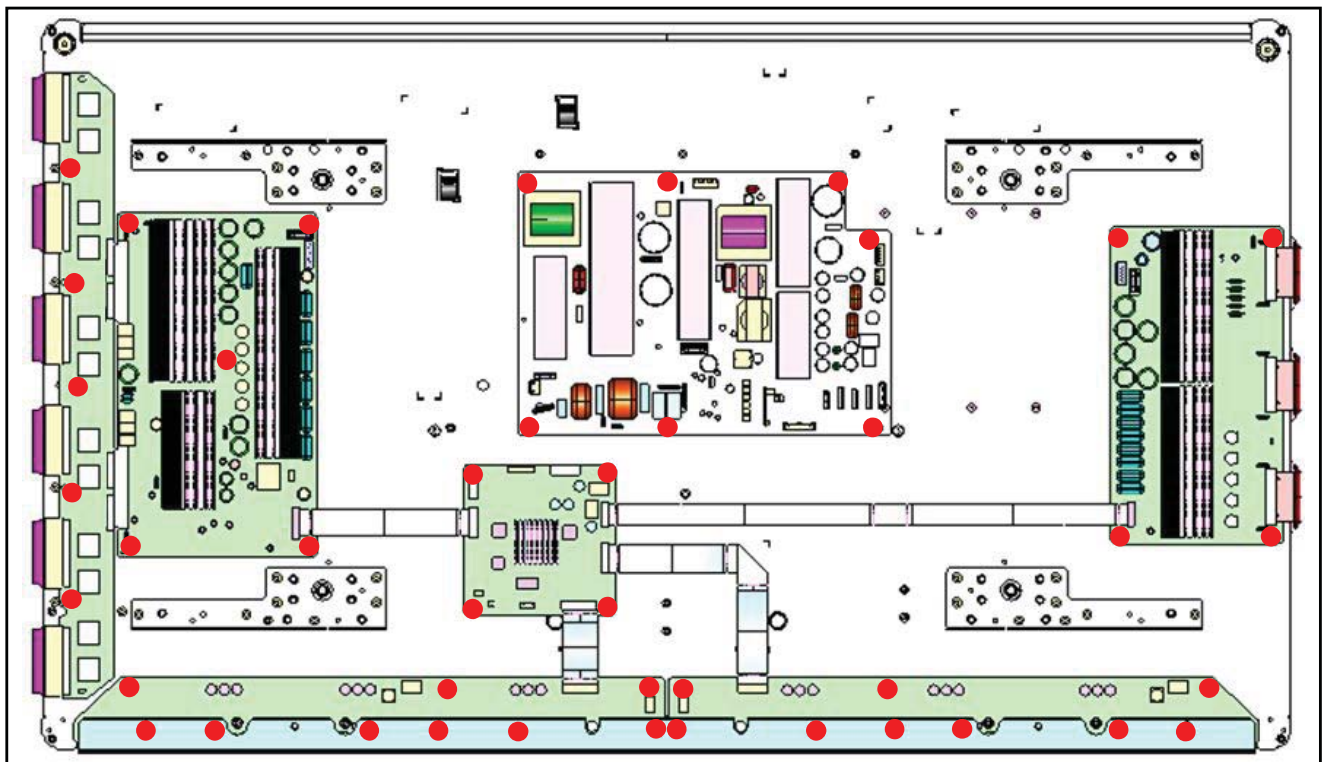
1. Remove the screws in order of 2-3-1-4 from the heatsink and remove the heatsink ("Photos 1 & 3").
2. Remove the TCP, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Place the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the screw mounting order 2-3-1-4.

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.



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Figure 4-18 Photo 1 - Heatsink 50" HD W2 Plus



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Figure 4-19 Photo 2 - Exchange of LBE, LBF board 50" HD W2 Plus

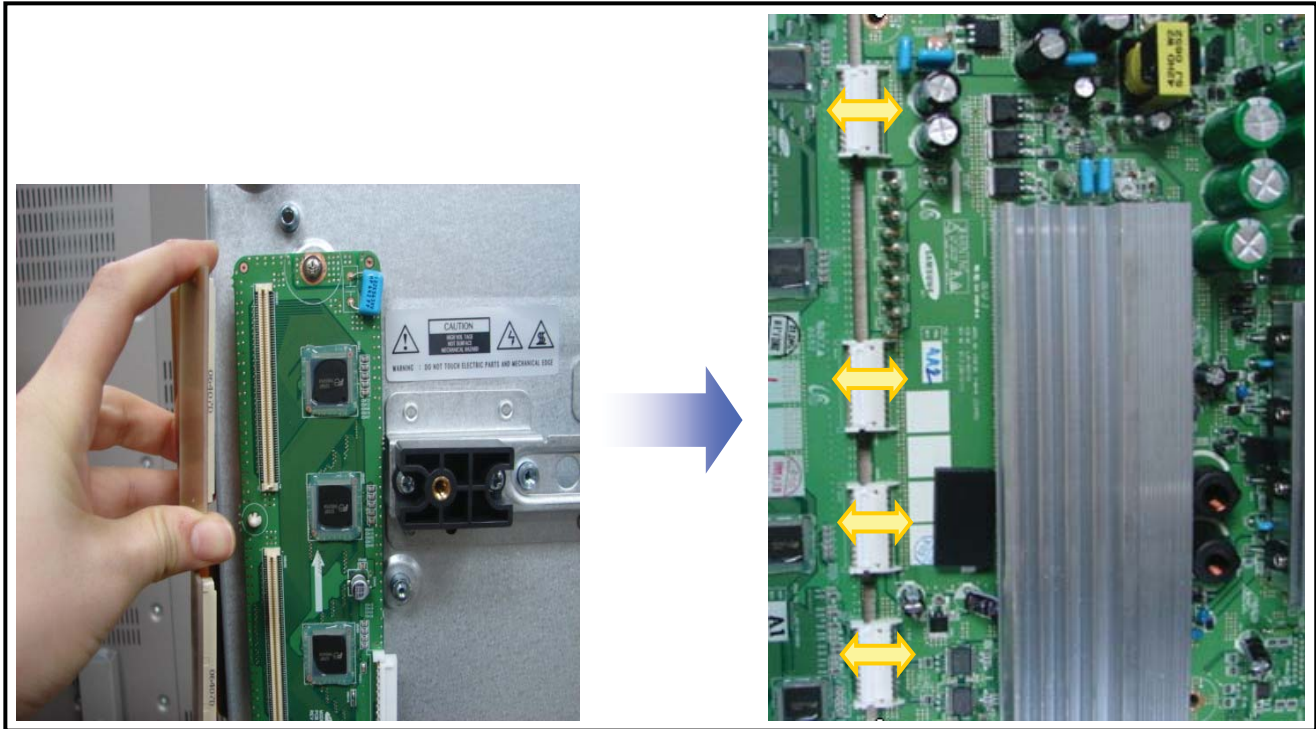


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Figure 4-20 Photo 3 - Heat sink removal

4.1.8 Exchange YB and YM board - 42" HD W2 & 42" HD W2 Plus

1. Unplug all of the FPC connectors of Y-B. See "Photo 1".
2. Loosen all the screws of Y-Buffer and Y-Main.
3. Remove the board from the chassis.
4. Unplug connectors CN5001, CN5002, CN5006 and CN5003 between Y-Buffer and Y-Main. See "Photo 2".
5. Remove Y-Buffer from the Y-main.
6. Replace the defective board.
7. Re-assemble Y-Buffer to the Y-Main.
8. Plug in connectors CN5001, CN5002, CN5006 and CN5003 between Y-Buffer and Y-Main.
9. Arrange the boards on the chassis and tighten them.
10. Connect the FPC connectors.
11. Supply the electric power to the module and then check the waveform of the board.
12. Turn "off" the power after the waveform is adjusted.

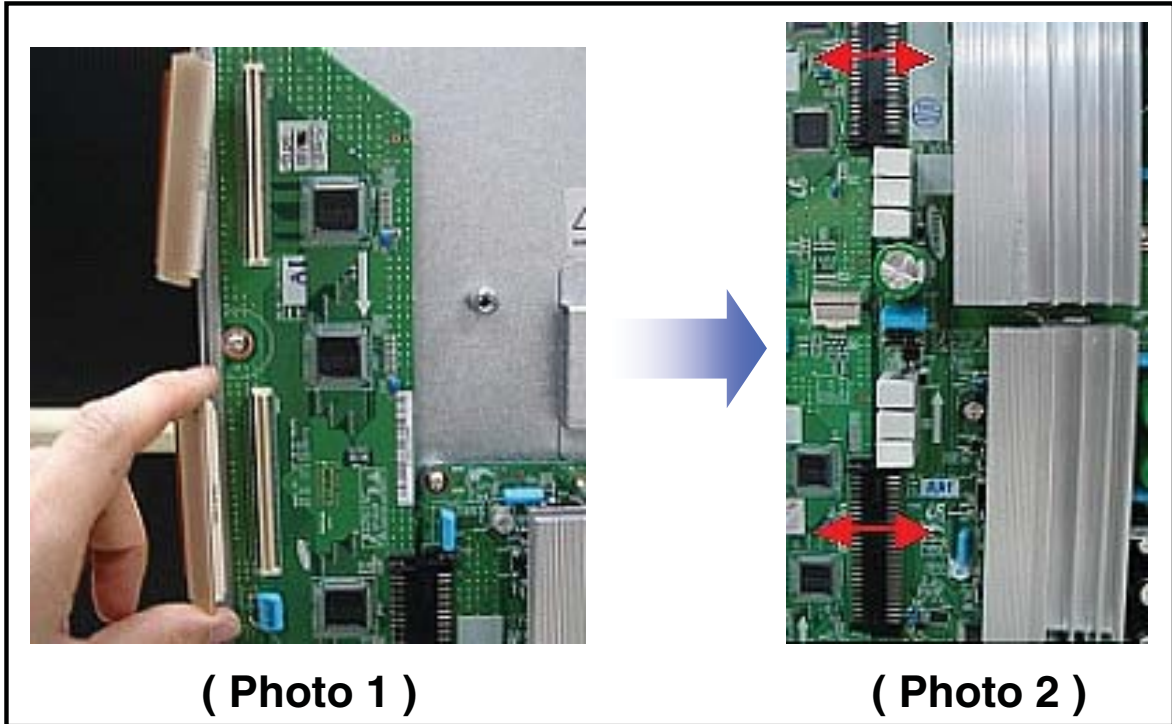


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Figure 4-21 Photo 1 and 2: Dis-assembly of YB and YM board - 42" HD W2 & 42" HD W2 Plus

4.1.9 Exchange YB and YM board - 50" HD W2 & 50" HD W2 Plus

1. Unplug all of the FPC connectors of YB. See "Photo 1".
2. Unplug connectors CN5600 and CN5601 between YB and YM ("Photo 2").
3. Loosen all the screws of YB, and Y-Main.
4. Remove the board from the chassis.
5. Remove the YB from the Y-main.
6. Replace the defective board.
7. Re-assemble the YB to the Y-Main.
8. Plug in connectors CN5600 and CN5601 between YB and YM.
9. Arrange the board on the chassis and then screw to fix.
10. Connect the FPCs.
11. Supply the electric power to the module and then check the waveform of the board.
12. Turn "off" the power after the waveform is adjusted.



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Figure 4-22 Photo 1 and 2: Dis-assembly of YB and YM board - 50" HD W2 & 50" HD W2 Plus

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

- 5.1 Repair Tools
 - 5.1.1 ComPair
 - 5.1.2 Other Service Tools
- 5.2 Fault Finding
 - 5.2.1 Fault finding tree
 - 5.2.2 Faulty Power Supply
 - 5.2.3 No Display
 - 5.2.4 Abnormal display
 - 5.2.5 Horizontal line or block open (some horizontal lines do not exist)
 - 5.2.6 Address open (some vertical lines do not exist)
 - 5.2.7 Address short (some vertical lines appear to be linked on the screen)
 - 5.2.8 Criteria for Panel Replacement, due to Defective Panel Cells
 - 5.2.9 Defect Overview
- 5.3 Defect Description Form

5.1 Repair Tools

5.1.1 ComPair

For the w2 and w2 Plus models, it will be possible to generate test patterns with ComPair. The ComPair interface must be connected to the Logic Board with the special interconnection cable (see table below for the order code).

5.1.2 Other Service Tools

Table 5-1 Overview Service tools

Service Tools	Order Code
ComPair / SDI interconnection cable	3122 785 90800
Foam buffers (2 pcs.)	3122 785 90581

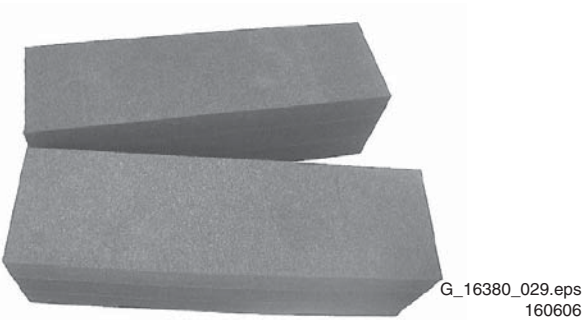


Figure 5-1 Foam buffers

5.2 Fault Finding

5.2.1 Fault finding tree

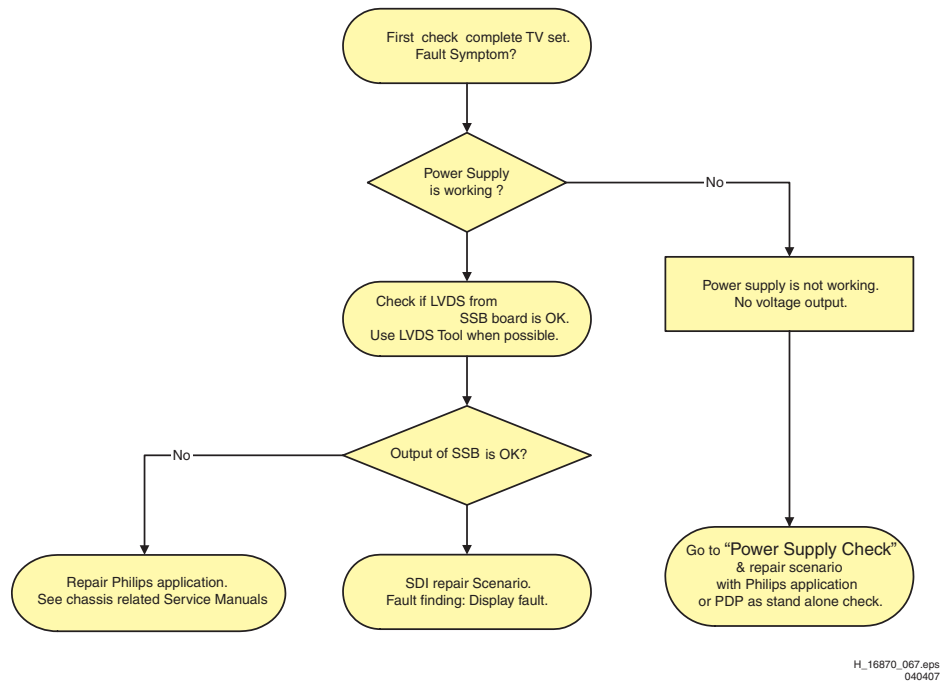


Figure 5-2 Fault symptom overview (complete TV set) [1/2]

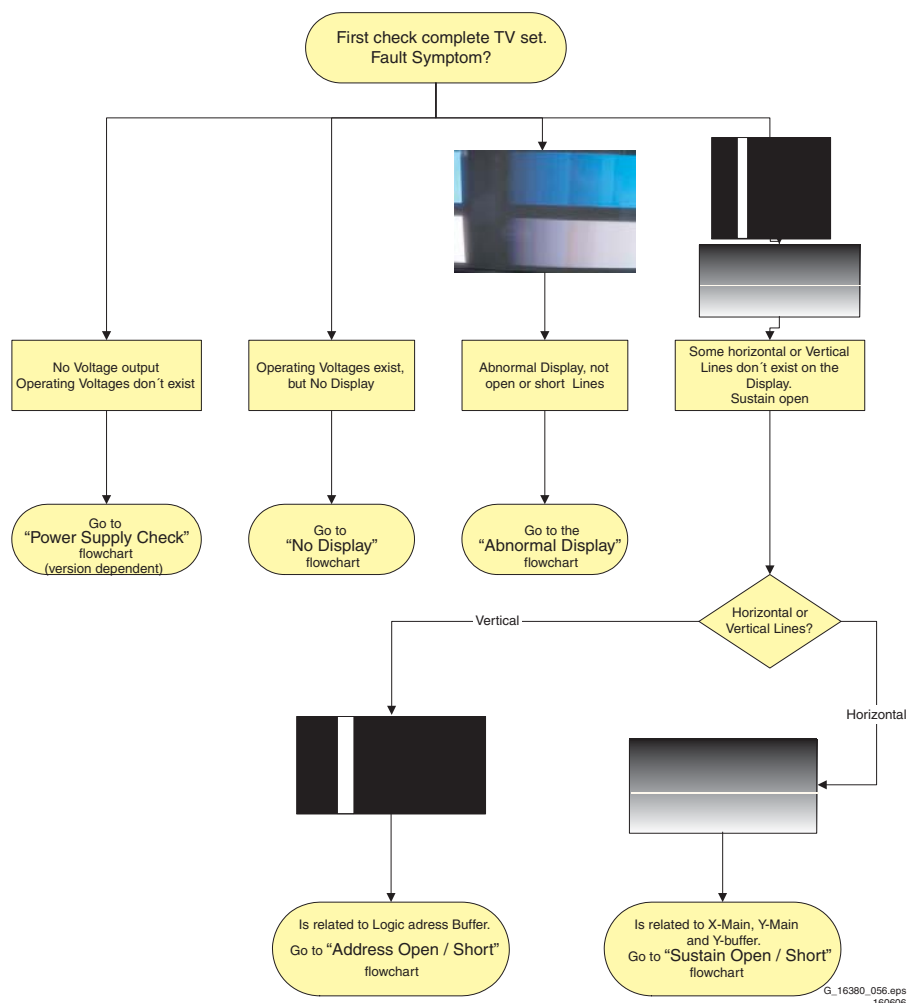


Figure 5-3 Fault symptom overview (complete TV set) [2/2]

5.2.2 Faulty Power Supply

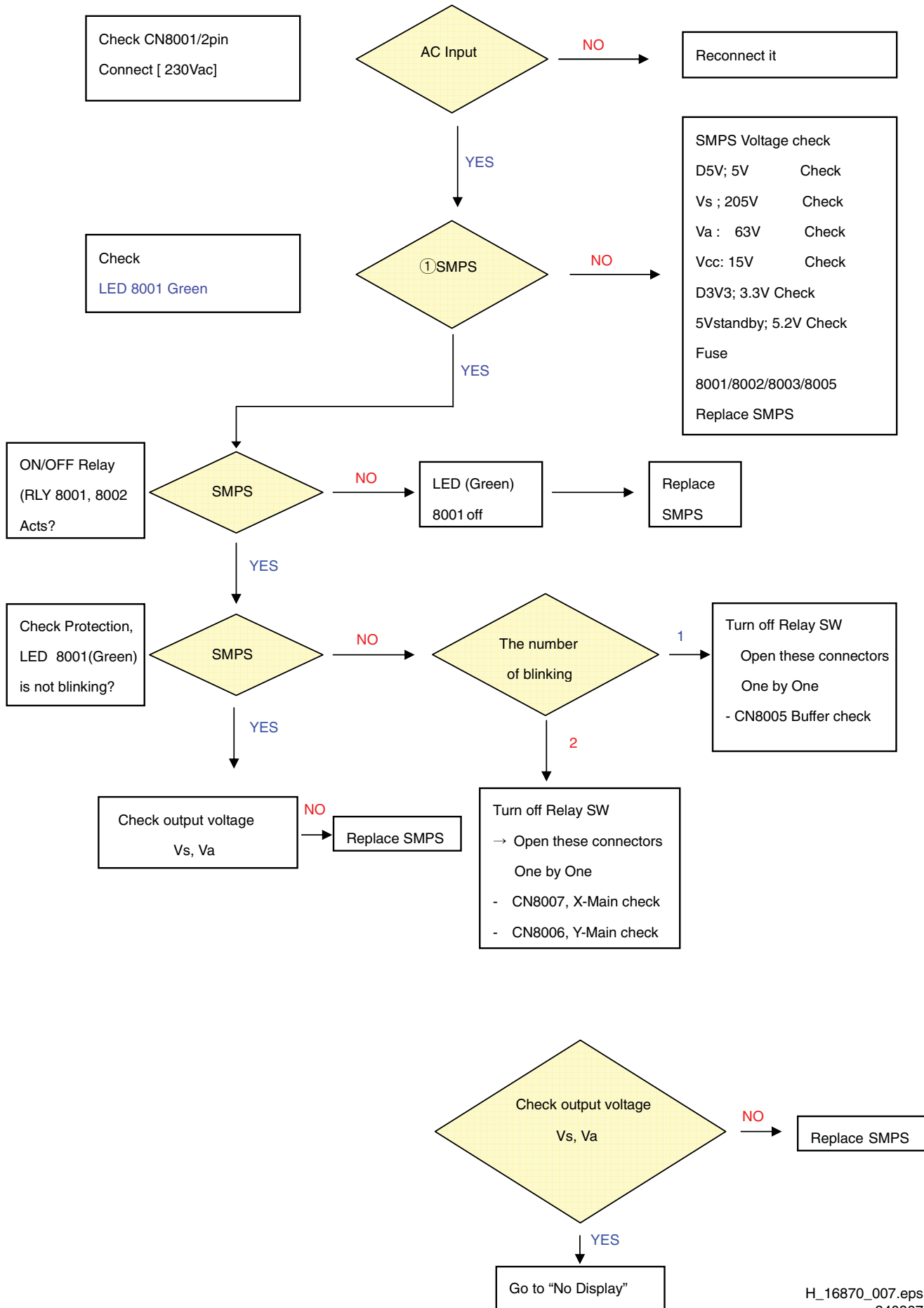


Figure 5-4 Power Supply Check for 42" HD W2 & 42" HD W2 Plus models

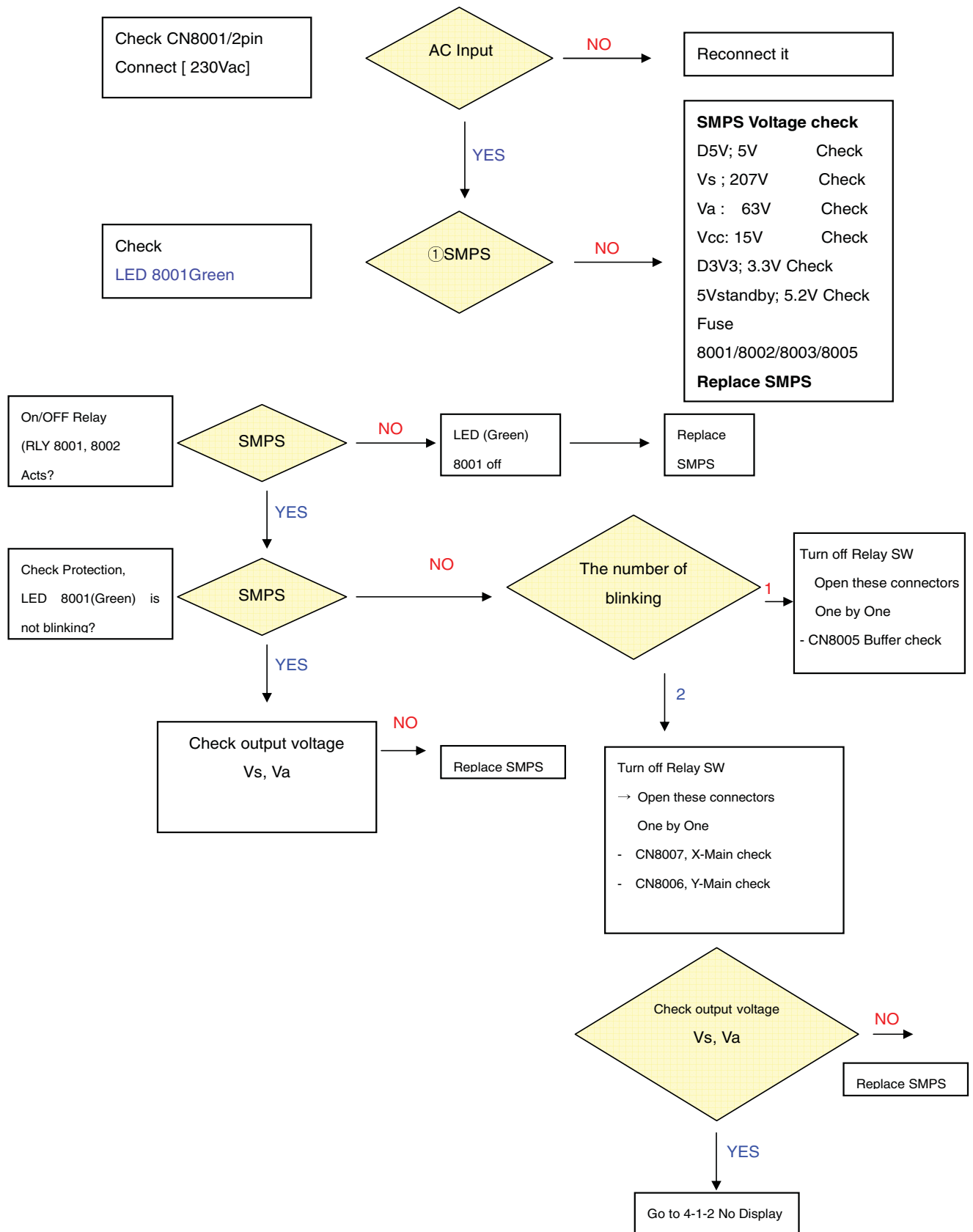


Figure 5-5 Power Supply Check for 50" HD W2 models

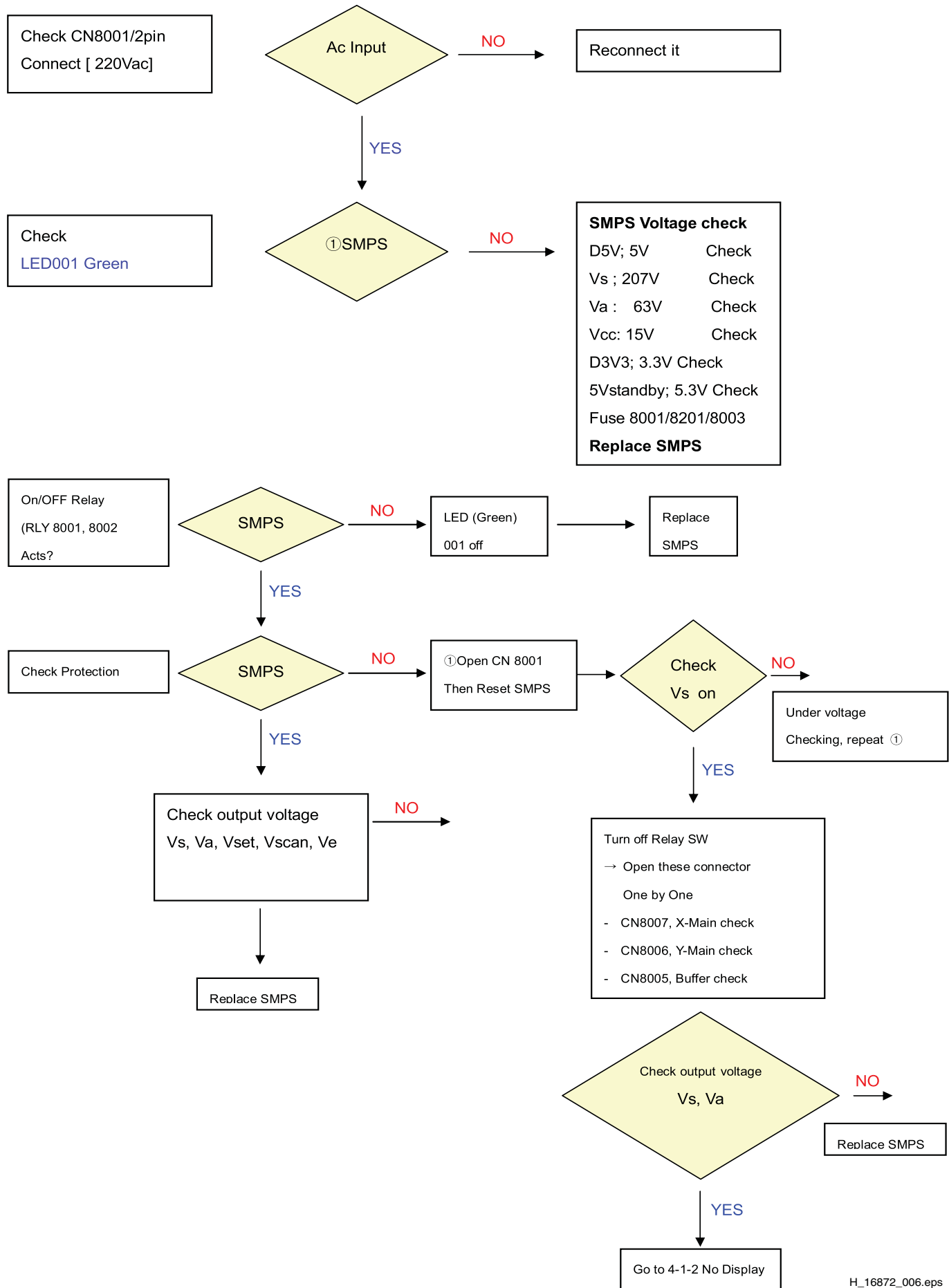


Figure 5-6 Power Supply Check for 50" HD W2 Plus models

5.2.3 No Display

“No Display” is related to Y-Main, X-Main, Logic Main and so on. This page shows you how to check the boards, and the following pages show you how to find the defective board.

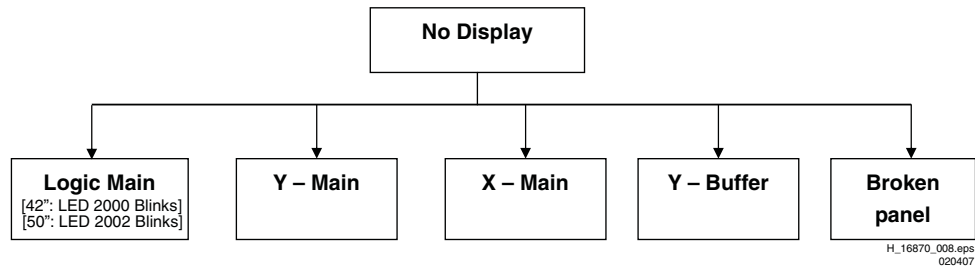


Figure 5-7 Fault symptom: “No Display”, general guide line

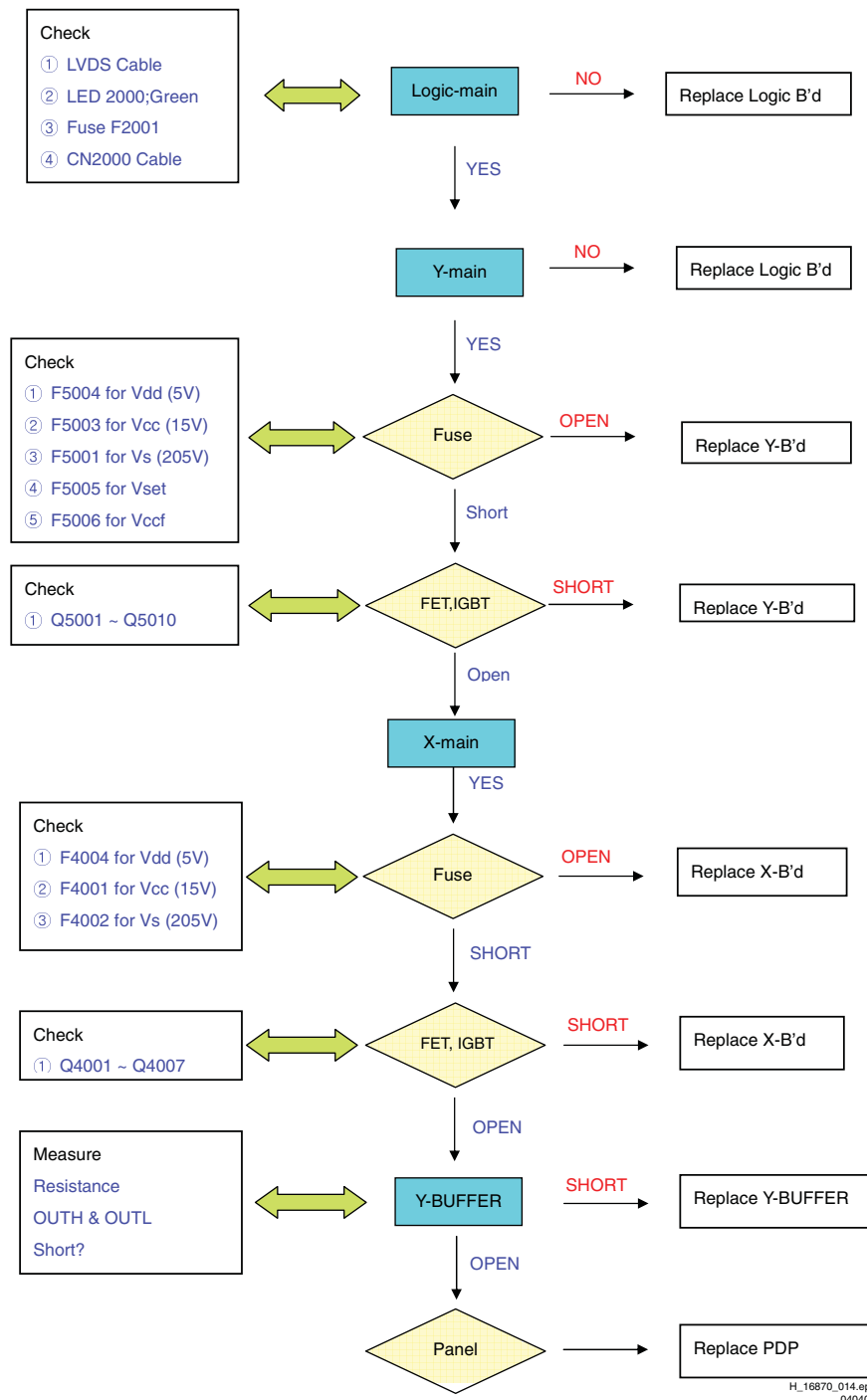





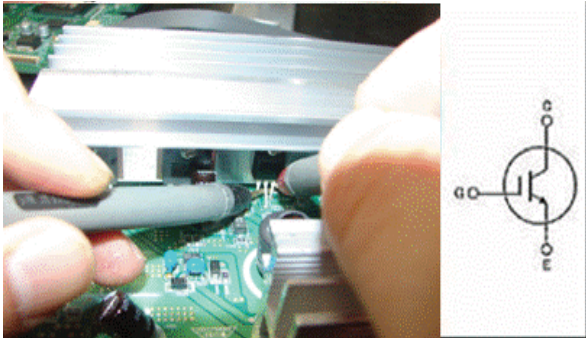


Figure 5-8 Fault finding tree: “No Display”, 42” HD W2 [1/5]

Y-main Check Point

	<p>OR</p> 
<p>Vs fuse (F5001) – OK (0.x ~ x.x ohm)</p>	<p>Vs fuse (F5001) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>15V fuse (F5003) – OK (0.x ~ x.x ohm)</p>	<p>15V fuse (F5003) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>5V fuse (F5004) – OK (0.x ~ x.x ohm)</p>	<p>5V fuse (F5004) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>Vset fuse (F5005) – OK (0.x ~ x.x ohm)</p>	<p>Vset fuse (F5005) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>Vccf (F5006) – OK (0.x ~ x.x ohm)</p>	<p>Vccf (F5006) – OPEN (x.x Mohm)</p>







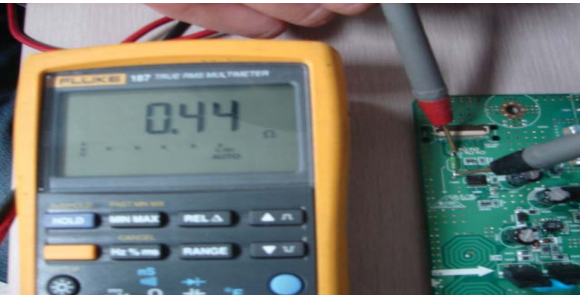


Figure 5-9 Y-Main check points 42" HD W2 [2/5]

IGBT, FET Check Point

	 
	<div>OK</div> <div>Short</div>
<div>FET,IGBT (contain the inner diode)</div> <div>[Ys, Yg, Yscan, Yfr, Yrr, Xs, Xg, Xb]</div>	<div>OK (0.3 ~ 0.9 V)</div> <div>/</div> <div>Short (0.000 ~ 0.00x V)</div>
	 
	<div>OK</div> <div>Short</div>
<div>IGBT (do not contain the inner diode)</div> <div>(Yr, Yf, Xr, Xf)</div>	<div>OK (xx.x kohm)</div> <div>/</div> <div>Short (x.x ohm)</div>
<div>Ys(Q5007), Yg(Q5001), Yscan(Q5008,9), Yfr(Q5006), Yrr(Q5004),</div> <div>Xs(Q4001), Xg(Q4002), Xb(Q4003,4)</div> <div>Yr(Q5003), Yf(Q5002), Xr(Q4006), Xf(Q4005)</div>	

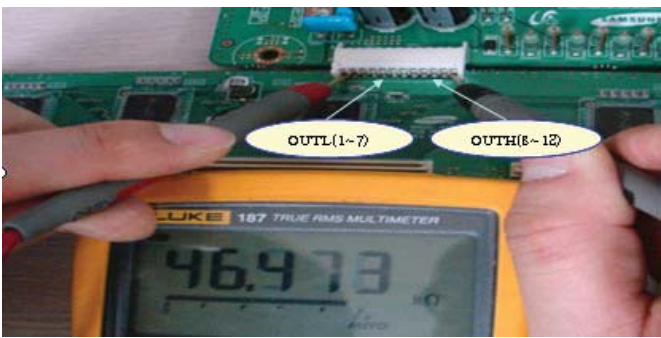
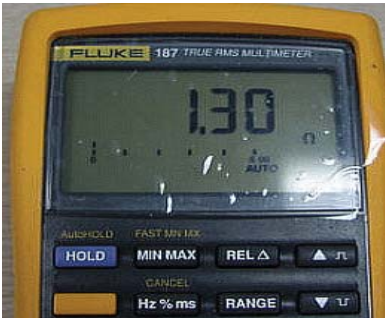
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Figure 5-10 FET, IGBT check points 42" HD W2 [3/5]

X-Main Check Point	
	OR  
Vs fuse (F4002) – OK (0.x ~ x.x ohm)	Vs fuse (F4002) – OPEN (x.x Mohm)
	OR  
15V fuse (F4001) – OK (0.x ~ x.x ohm)	15V fuse (F4001) – OPEN (x.x Mohm)
	OR  
5V fuse (F4004) – OK (0.x ~ x.x ohm)	5V fuse (F4004) – OPEN (x.x Mohm)

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Figure 5-11 X-Main check points 42” HD W2 [4/5]

Y-Buffer Check Point	
	
OUTL↔OUTH – OK (x.x Mohm)	OUTL↔OUTH –Short (x.x ohm)

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Figure 5-12 Y-Buffer check points 42” HD W2 [5/5]

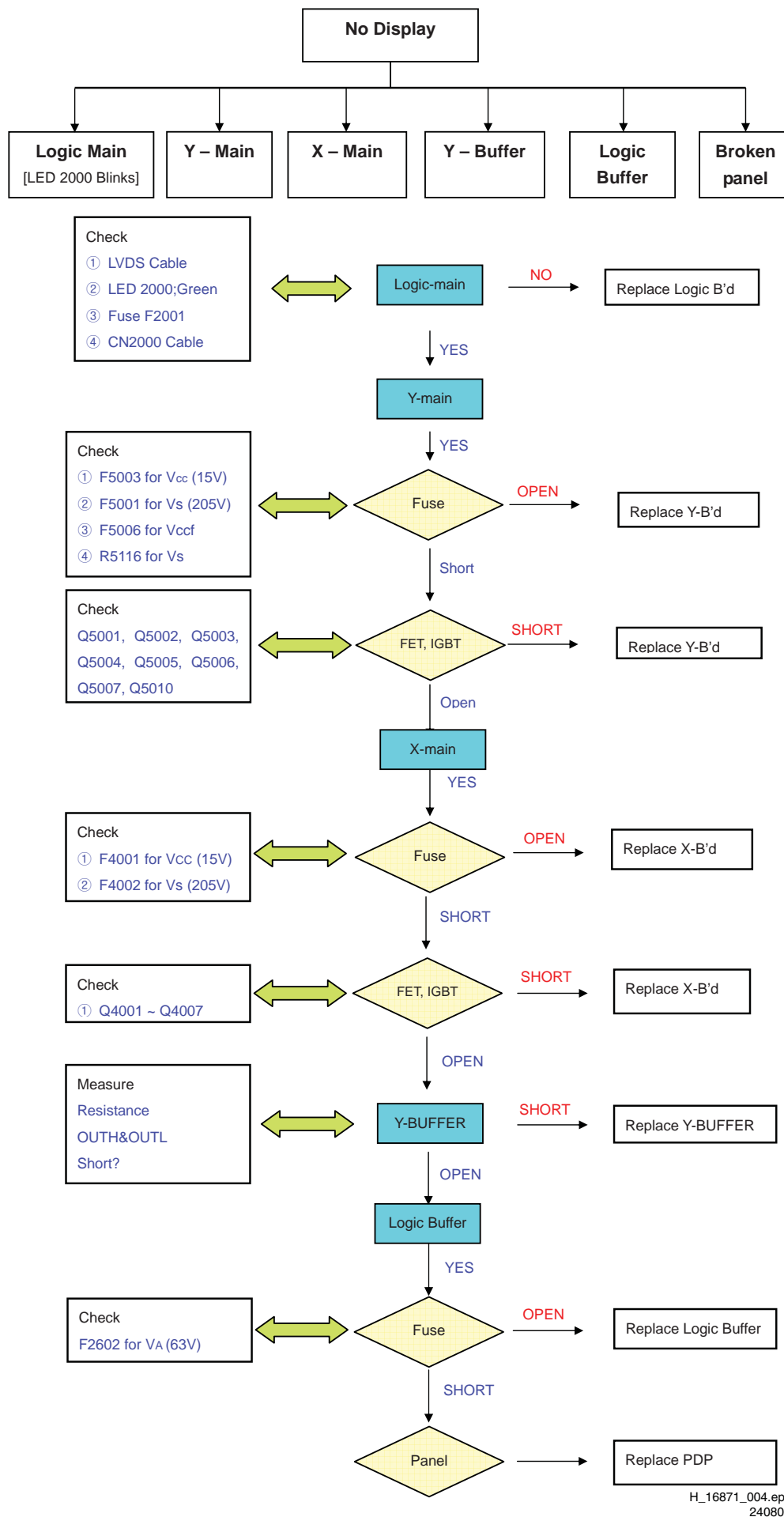
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Figure 5-13 Fault finding tree: "No Display", 42" HD W2 Plus [1/5]



Y-main Check Point

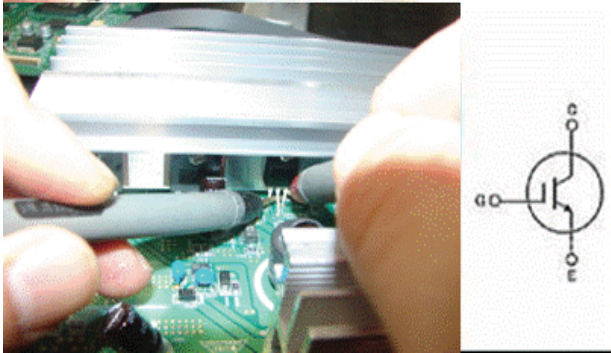

	<div>OR</div> <div>   </div>
<p>Vs fuse (F5001) – OK (0.x ~ x.x ohm)</p>	<p>Vs fuse (F5001) – OPEN (x.x Mohm)</p>
	<div>OR</div> <div>   </div>
<p>15V fuse (F5003) – OK (0.x ~ x.x ohm)</p>	<p>15V fuse (F5003) – OPEN (x.x Mohm)</p>
	<div>OR</div> <div>   </div>
<p>Vccf fuse (F5006) – OK (0.x ~ x.x ohm)</p>	<p>Vcc fuse (F5006) – OPEN (x.x Mohm)</p>
	<div>OR</div> <div>   </div>
<p>R-fusible (R5116) – OK (1.xohm)</p>	<p>R-fusible (R5116) – OPEN (x.x Mohm)</p>

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Figure 5-14 Y-Main check points 42" HD W2 Plus [2/5]

IGBT, FET Check Point







	 <div data-bbox="1023 629 1062 656">OK</div> <div data-bbox="1337 629 1406 656">Short</div>
<p>FET,IGBT (contain the inner diode) [Ys, Yg, Yfr, Yrr, Xs, Xg, Xb]</p>	<p>OK (0.3 ~ 0.9 V) / Short (0.000 ~ 0.00x V)</p>

	 <div data-bbox="1026 1187 1066 1214">OK</div> <div data-bbox="1347 1187 1415 1214">Short</div>
<p>IGBT (do not contain the inner diode) (Yr, Yf, Xr, Xf)</p>	<p>OK (xx.x kohm) / Short (x.x ohm)</p>

Ys(Q5007), Yg(Q5001), Yfr(Q5006), Yrr(Q5004),
Xs(Q4001), Xg(Q4002), Xb(Q4003,4)
Yr(Q5003), Yf(Q5002), Xr(Q4006), Xf(Q4005)

Figure 5-15 FET, IGBT check points 42” HD W2 Plus [3/5]

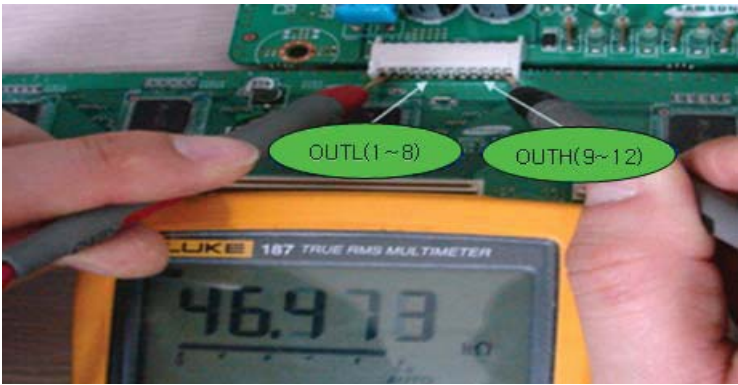

X-main Check Point

	OR	
		
Vs fuse (F4002) – OK (0.x ~ x.x ohm)	Vs fuse (F4002) – OPEN (x.x Mohm)	
	OR	
		
15V fuse (F4001) – OK (0.x ~ x.x ohm)	15V fuse (F4001) – OPEN (x.x Mohm)	

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Figure 5-16 X-Main check points 42" HD W2 Plus [4/5]

Y-buffer Check Point

	
OUTL↔OUTH – OK (x.x Mohm)	OUTL↔OUTH –Short (x.x ohm)

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240807

Figure 5-17 Y-Buffer check points 42" HD W2 Plus [5/5]

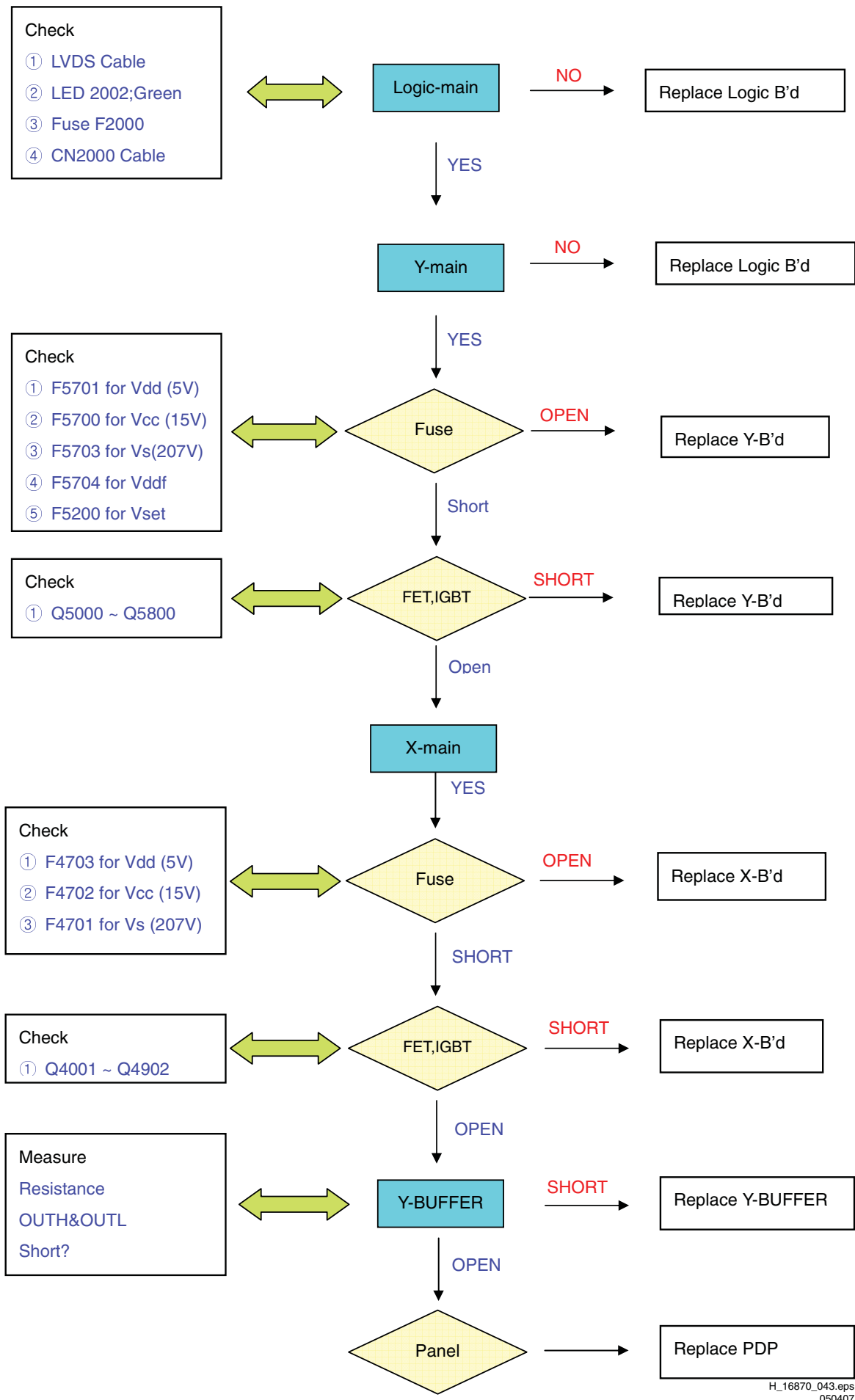
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050407

Figure 5-18 Fault finding tree: "No Display", 50" HD W2 [1/5]

Y-main Check Point




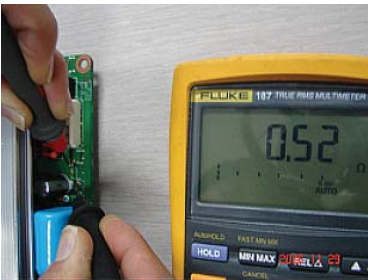


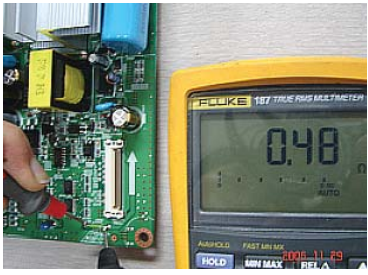


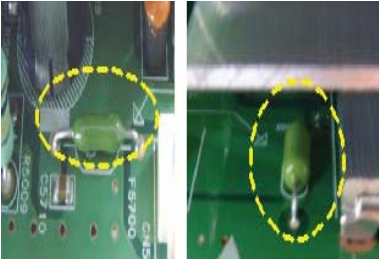









	<p>OR</p>  
<p>Vs fuse (F5703) – OK (0.x ~ x.x ohm)</p>	<p>Vs fuse (F5703) – OPEN (x.x Mohm)</p>
	<p>OR</p>  
<p>15V fuse (F5700) – OK (0.x ~ x.x ohm)</p>	<p>15V fuse (F5004) – OPEN (x.x Mohm)</p>
	<p>OR</p>  
<p>5V fuse (F5701) – OK (0.x ~ x.x ohm)</p>	<p>5V fuse (F5001) – OPEN (x.x Mohm)</p>
	<p>OR</p>  
<p>Vset fuse (F5200) – OK (0.x ~ x.x ohm)</p>	<p>Vset fuse (F5200) – OPEN (x.x Mohm)</p>
	<p>OR</p>  
<p>Vddf (F5704) – OK (0.x ~ x.x ohm)</p>	<p>Vddf (F5704) – OPEN (x.x Mohm)</p>


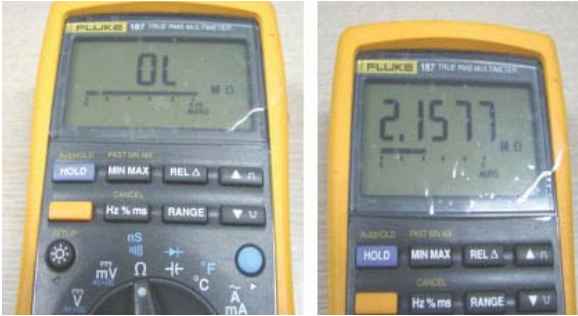
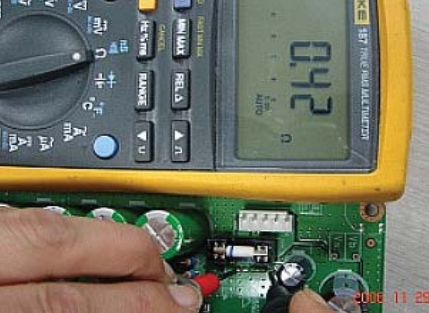


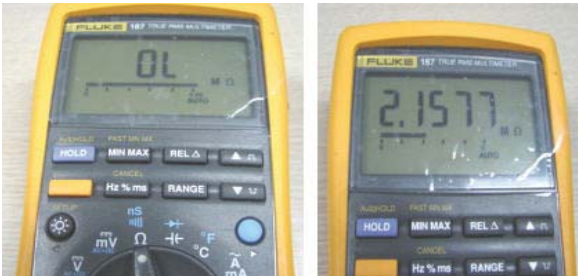

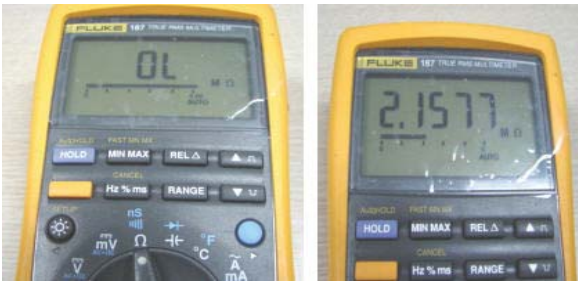
Figure 5-19 Y-Main check points 50" HD W2 [2/5]

IGBT, FET Check Point

	 <p style="text-align: center;">OK Short</p>
<p style="text-align: center;">FET,IGBT (contain the inner diode) [Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xb]</p>	<p style="text-align: center;">OK (0.3 ~ 0.9 V) / Short (0.000 ~ 0.00x V)</p>
	 <p style="text-align: center;">OK Short</p>
<p style="text-align: center;">IGBT (do not contain the inner diode) (Yr, Yf, Xr, Xf)</p>	<p style="text-align: center;">OK (xx.x kohm) / Short (x.x ohm)</p>
<p>Ys(Q5100,01), Yg(Q5102,03), Ypn(Q5302,03,04,06), Yscan(Q5400,01), Yfr(Q5500), Yrr(Q5200), Xs(Q4101,02), Xg(Q4103,04), Xb(Q4901,02) Yr(Q5000,02), Yf(Q5001,03), Xr(Q4001), Xf(Q4002,03)</p>	

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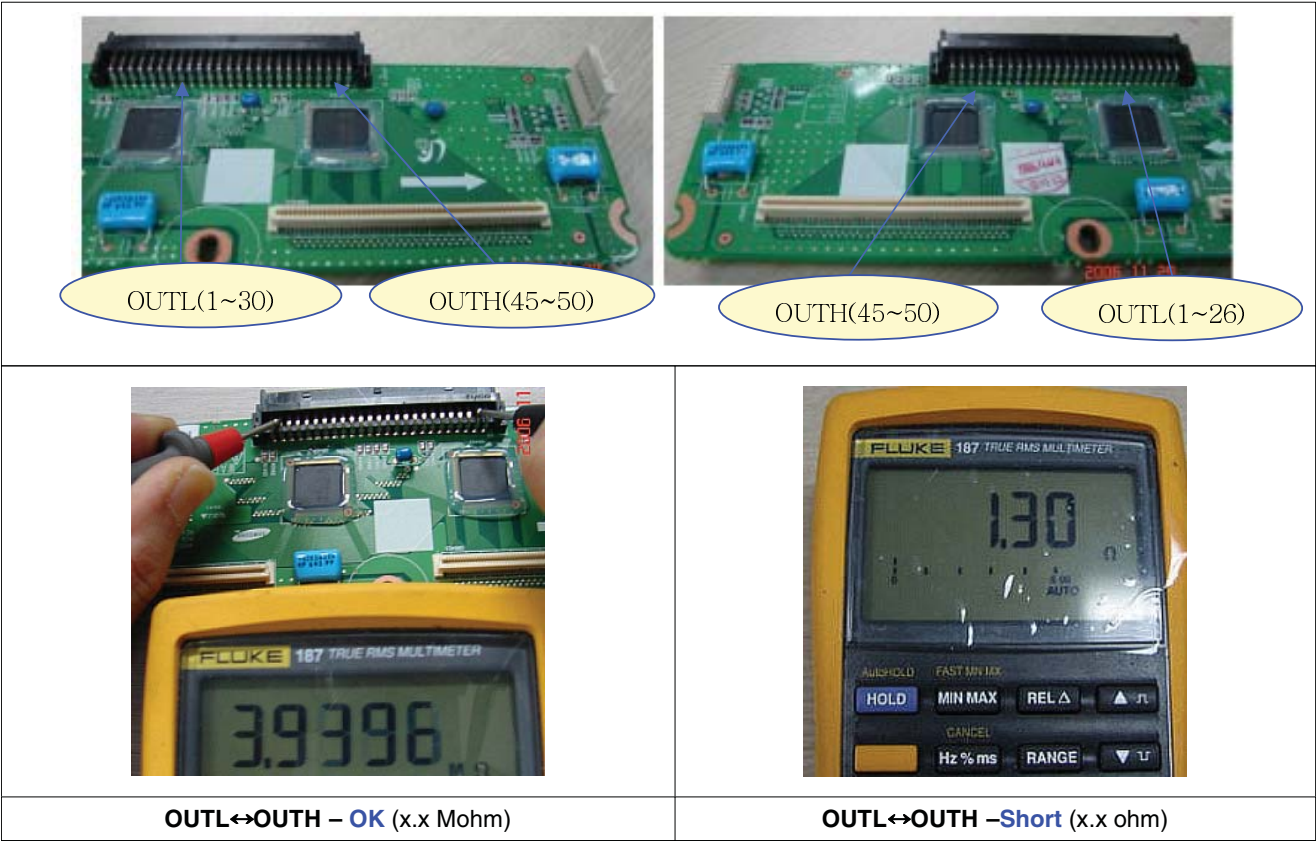
Figure 5-20 FET, IGBT check points 50" HD W2 [3/5]

	<p>OR</p> 
<p>Vs fuse (F4701) – OK (0.x ~ x.x ohm)</p>	<p>Vs fuse (F4701) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>15V fuse (F4702) – OK (0.x ~ x.x ohm)</p>	<p>15V fuse (F4702) – OPEN (x.x Mohm)</p>
	<p>OR</p> 
<p>5V fuse (F4703) – OK (0.x ~ x.x ohm)</p>	<p>5V fuse (F4703) – OPEN (x.x Mohm)</p>
	
<p>5V fuse (F4800) – OK (0.x ~ x.x ohm)</p>	<p>5V fuse (F4800) – OPEN (x.x Mohm)</p>

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Figure 5-21 X-Main check points 50" HD W2 [4/5]

Y-buffer Check Point



H_16870_049.eps
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Figure 5-22 Y-Buffer check points 50” HD W2 [5/5]

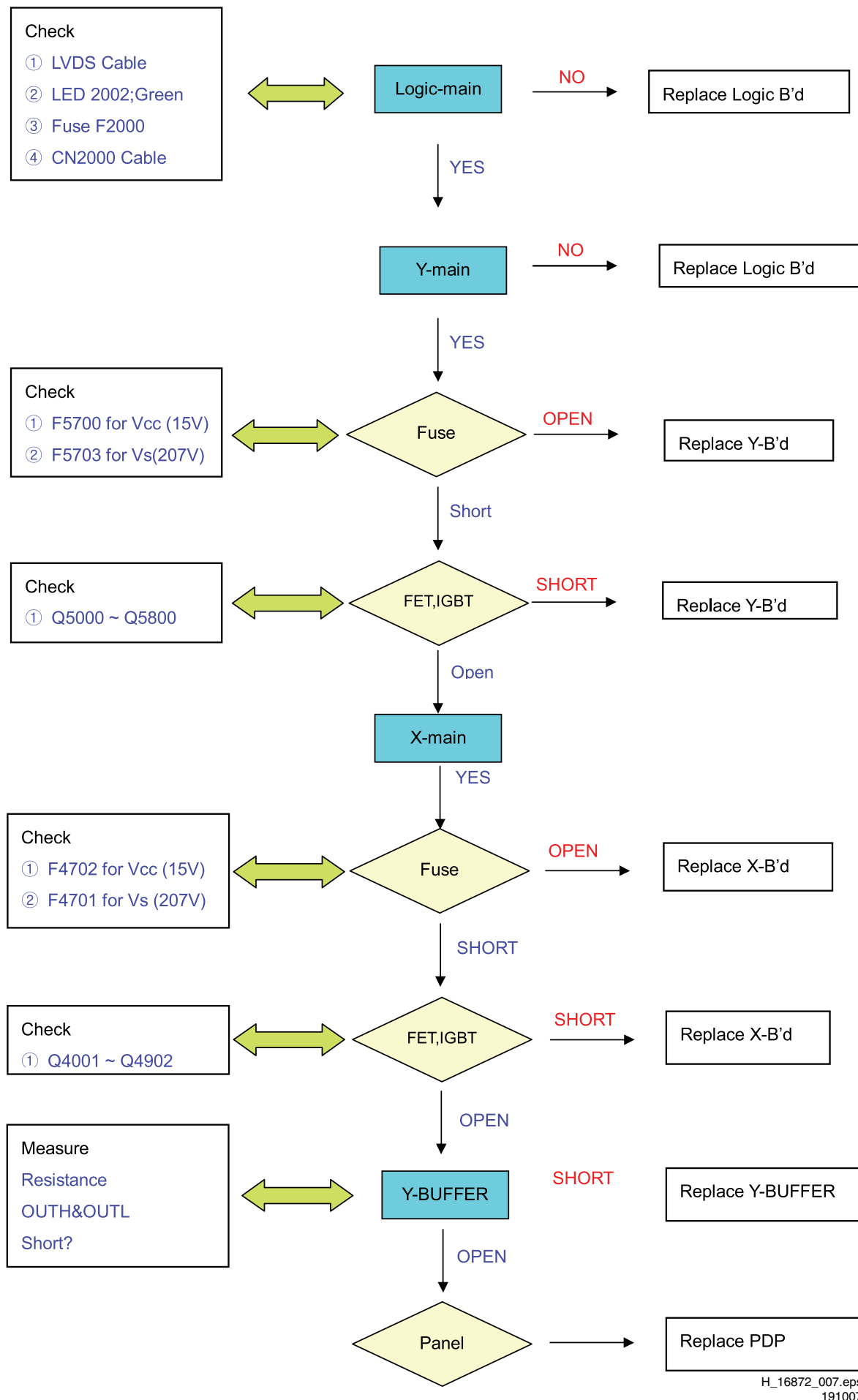


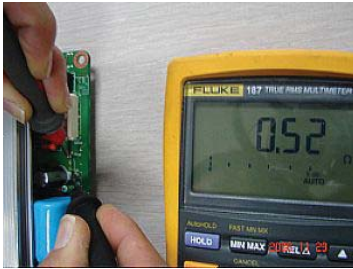







Figure 5-23 Fault finding tree: "No Display", 50" HD W2 Plus [1/5]

Samsung SDI Co. Ltd.	Y-main Check Point	Plasma Display Module
	Vs fuse (F5703) – OK (0.x ~ x.x ohm)	OR 
	15V fuse (F5700) – OK (0.x ~ x.x ohm)	OR 
		Vs fuse (F5703) – OPEN (x.x Mohm)
		15V fuse (F5004) – OPEN (x.x Mohm)







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Figure 5-24 Y-Main check points 50" HD W2 Plus [2/5]

IGBT, FET Check Point	
	
FET, IGBT (contain the inner diode) [Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xb]	OK (0.3 ~ 0.9 V) / Short (0.000 ~ 0.00x V)
	
IGBT (do not contain the inner diode) (Yr, Yf, Xr, Xf)	OK (xx.x kohm) / Short (x.x ohm)
Ys(Q5100,01), Yg(Q5102,03), Ypn(Q5302,03,04,06), Yscan(Q5400,01), Yfr(Q5500), Yrr(Q5200), Xs(Q4101,02), Xg(Q4103,04), Xb(Q4901,02) Yr(Q5000,02), Yf(Q5001,03), Xr(Q4001), Xf(Q4002,03)	

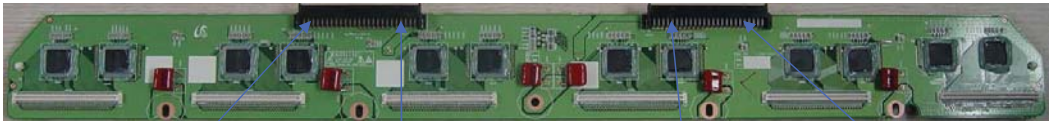
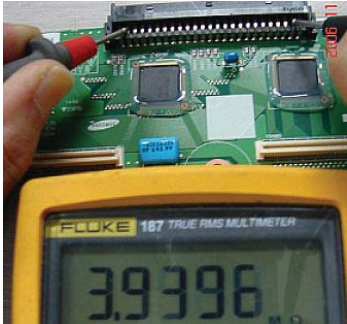

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Figure 5-25 FET, IGBT check points 50" HD W2 Plus [3/5]

	OR  
Vs fuse (F4701) – OK (0.x ~ x.x ohm)	Vs fuse (F4701) – OPEN (x.x Mohm)
	OR  
15V fuse (F4702) – OK (0.x ~ x.x ohm)	15V fuse (F4702) – OPEN (x.x Mohm)

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Figure 5-26 X-Main check points 50” HD W2 Plus [4/5]

<div>Y-buffer Check Point</div> 	
	
OUTL↔OUTH – OK (x.x Mohm)	OUTL↔OUTH –Short (x.x ohm)

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Figure 5-27 Y-Buffer check points 50” HD W2 Plus [5/5]

5.2.4 Abnormal display

“Abnormal Display” is related to Y-Main, X-Main, Logic Main and so on. This page shows you how to check the boards, and the following pages show you how to find the defective board.

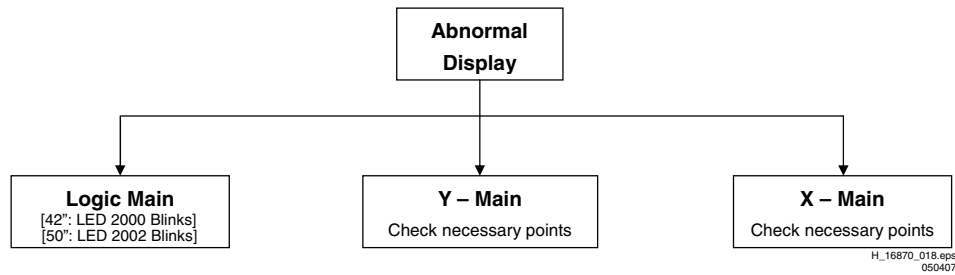


Figure 5-28 Fault symptom: “Abnormal Display”, general guide line

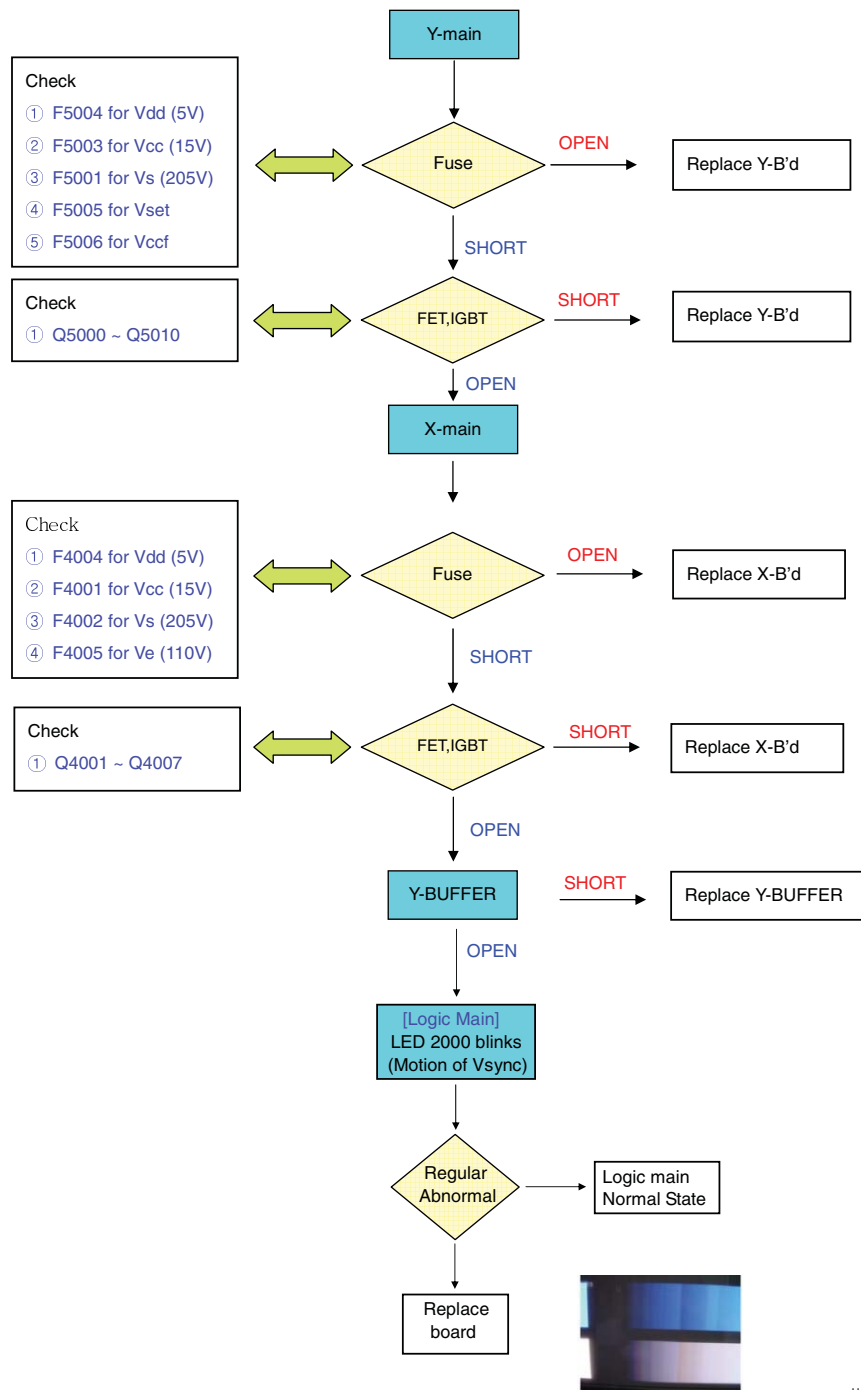


Figure 5-29 Fault symptom: “Abnormal Display” 42” HD W2

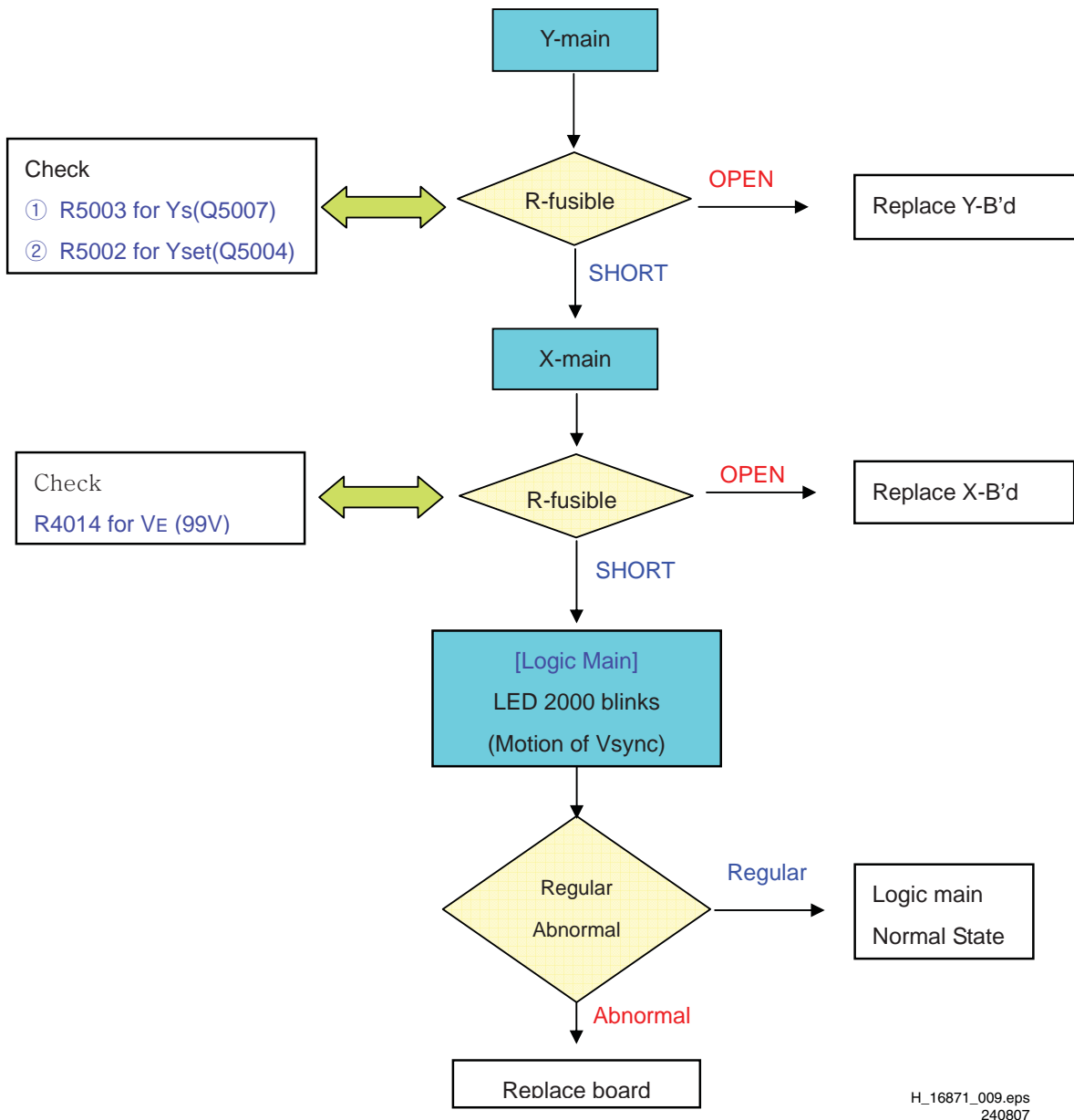
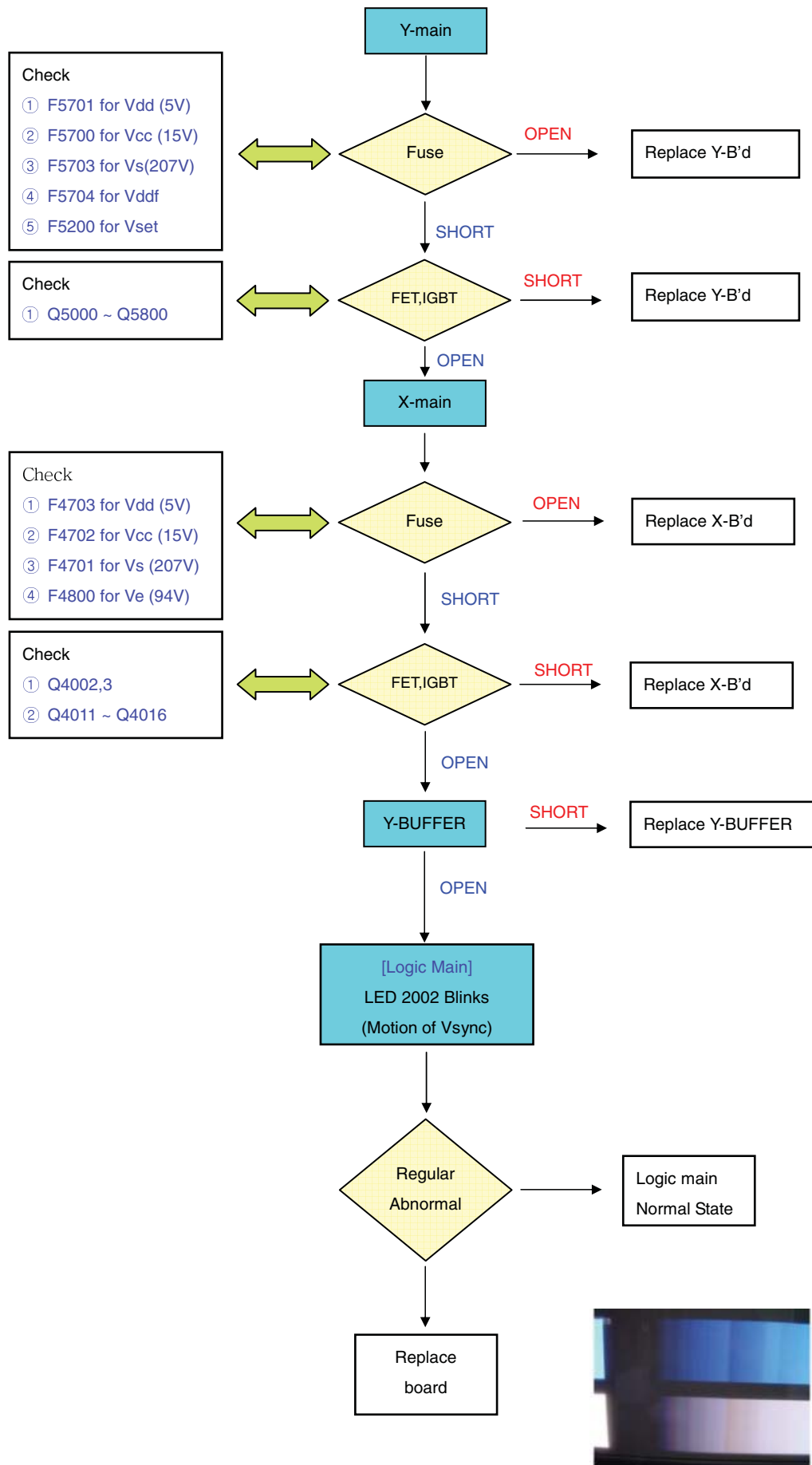


Figure 5-30 Fault symptom: "Abnormal Display" 42" HD W2 Plus



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050407

Figure 5-31 Fault symptom: "Abnormal Display" 50" HD W2

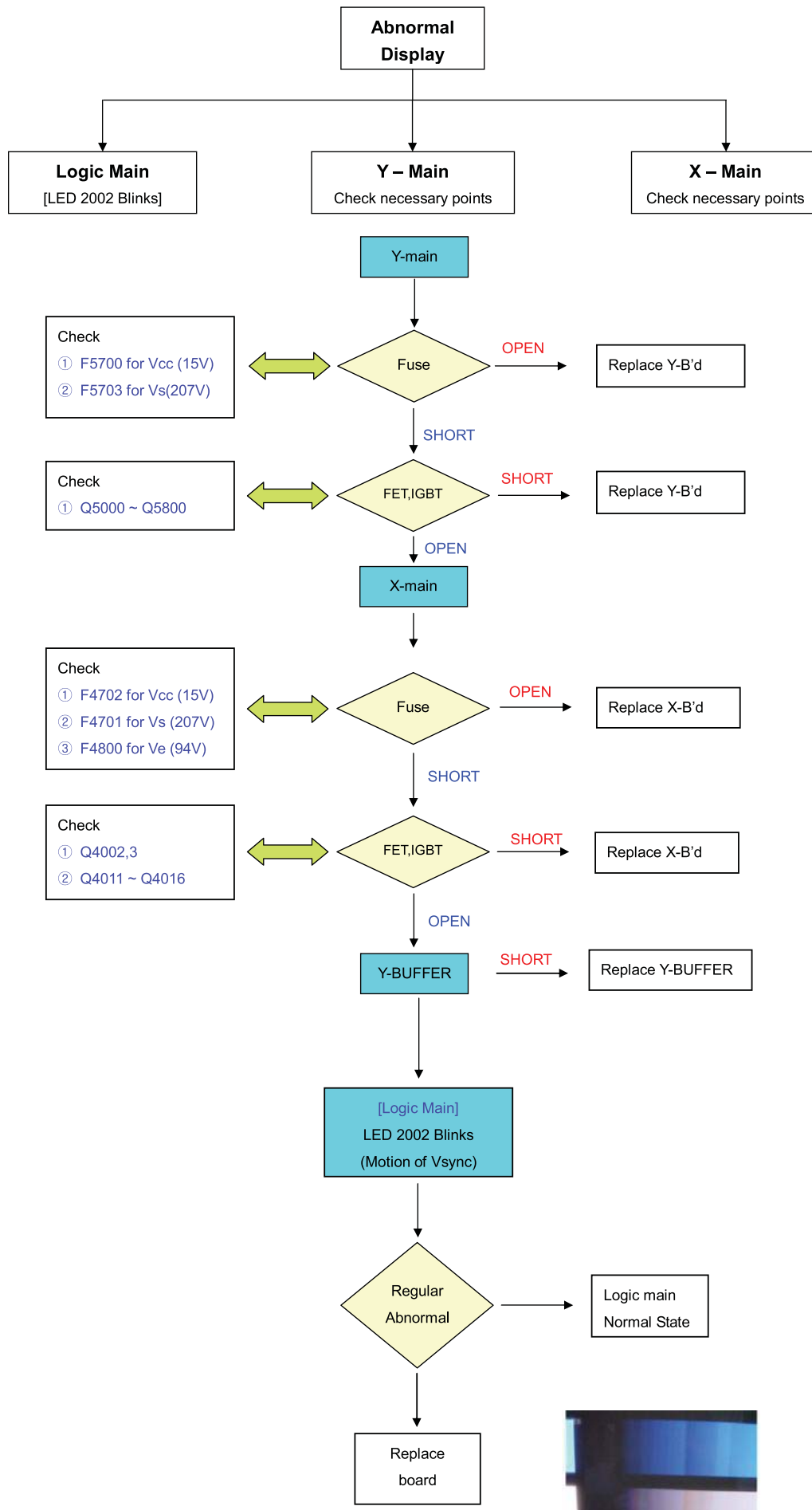


Figure 5-32 Fault symptom: "Abnormal Display" 50" HD W2 Plus

5.2.5 Horizontal line or block open (some horizontal lines do not exist)

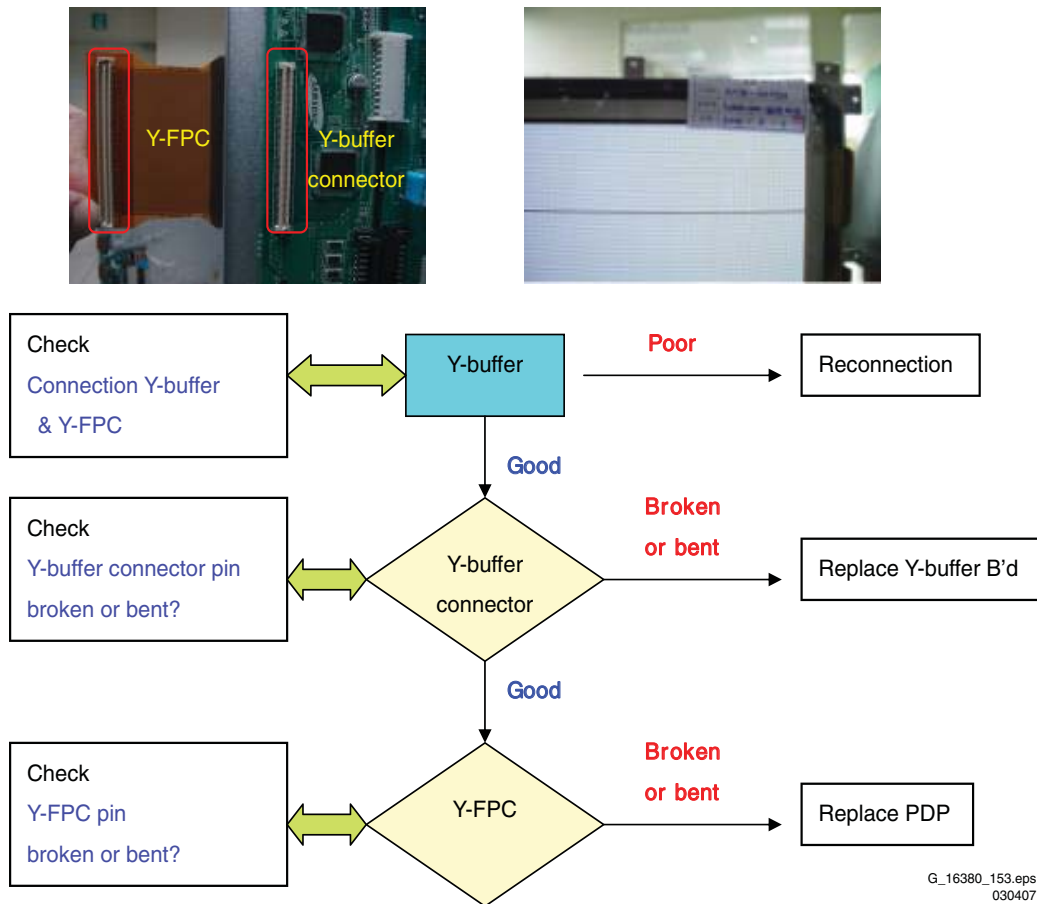


Figure 5-33 Fault symptom: "Horizontal line or block open"

5.2.6 Address open (some vertical lines do not exist)

"Address open" is related to Logic Main, Logic Buffer, FFC, TCP and so on. This page shows you how to check the boards, and the following pages show you how to find the defective board.

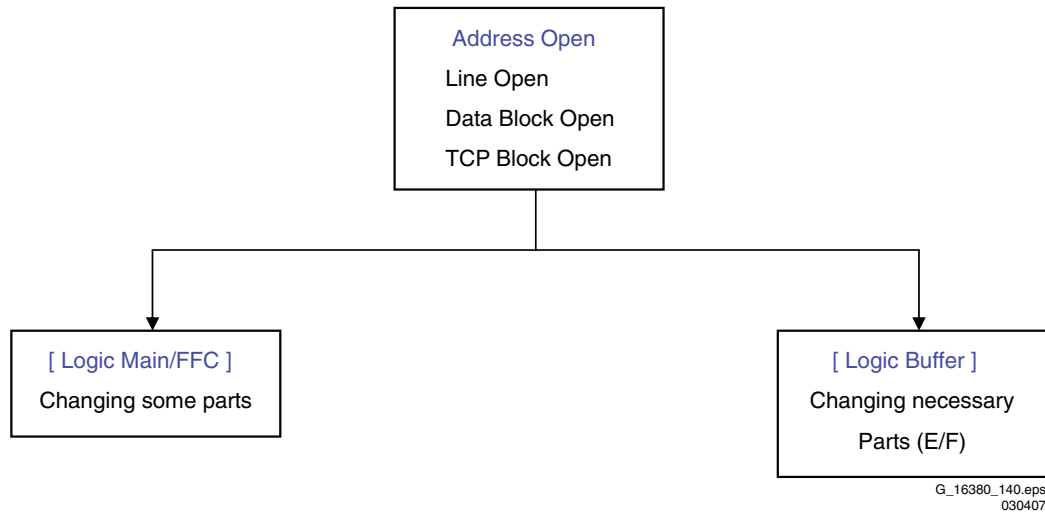


Figure 5-34 Fault symptom: "Address open" [1/2]

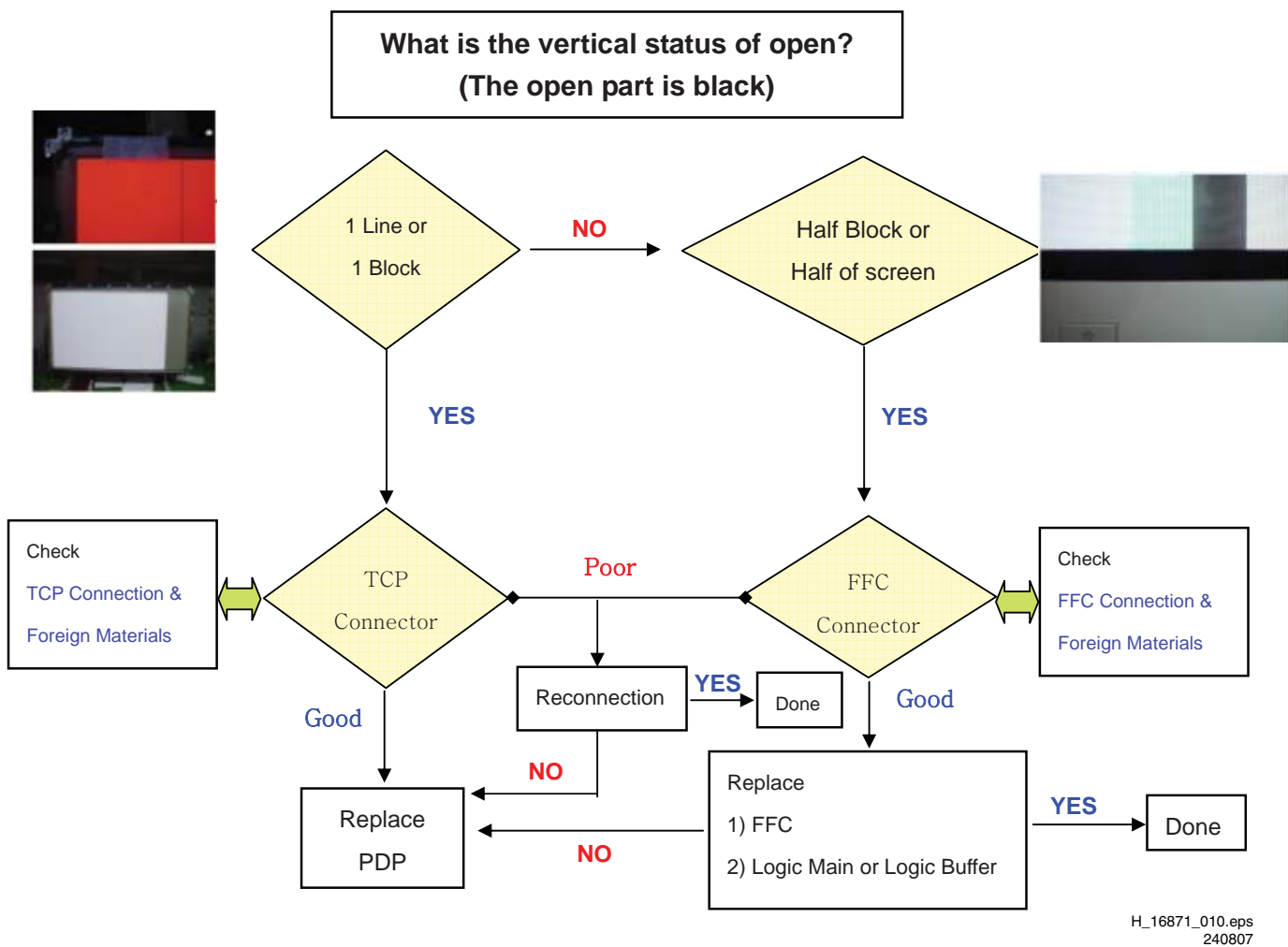


Figure 5-35 Fault symptom: "Address open" [2/2]

5.2.7 Address short (some vertical lines appear to be linked on the screen)

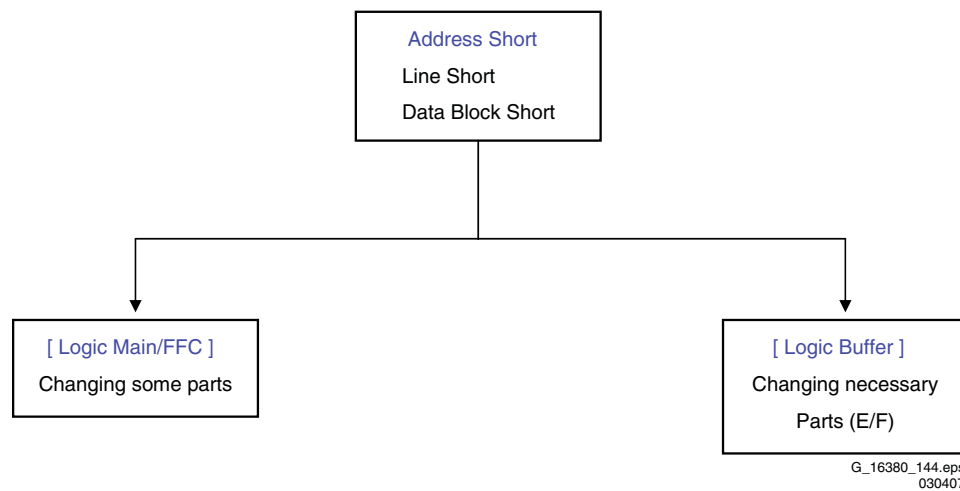


Figure 5-36 Fault symptom: "Address short" [1/2]

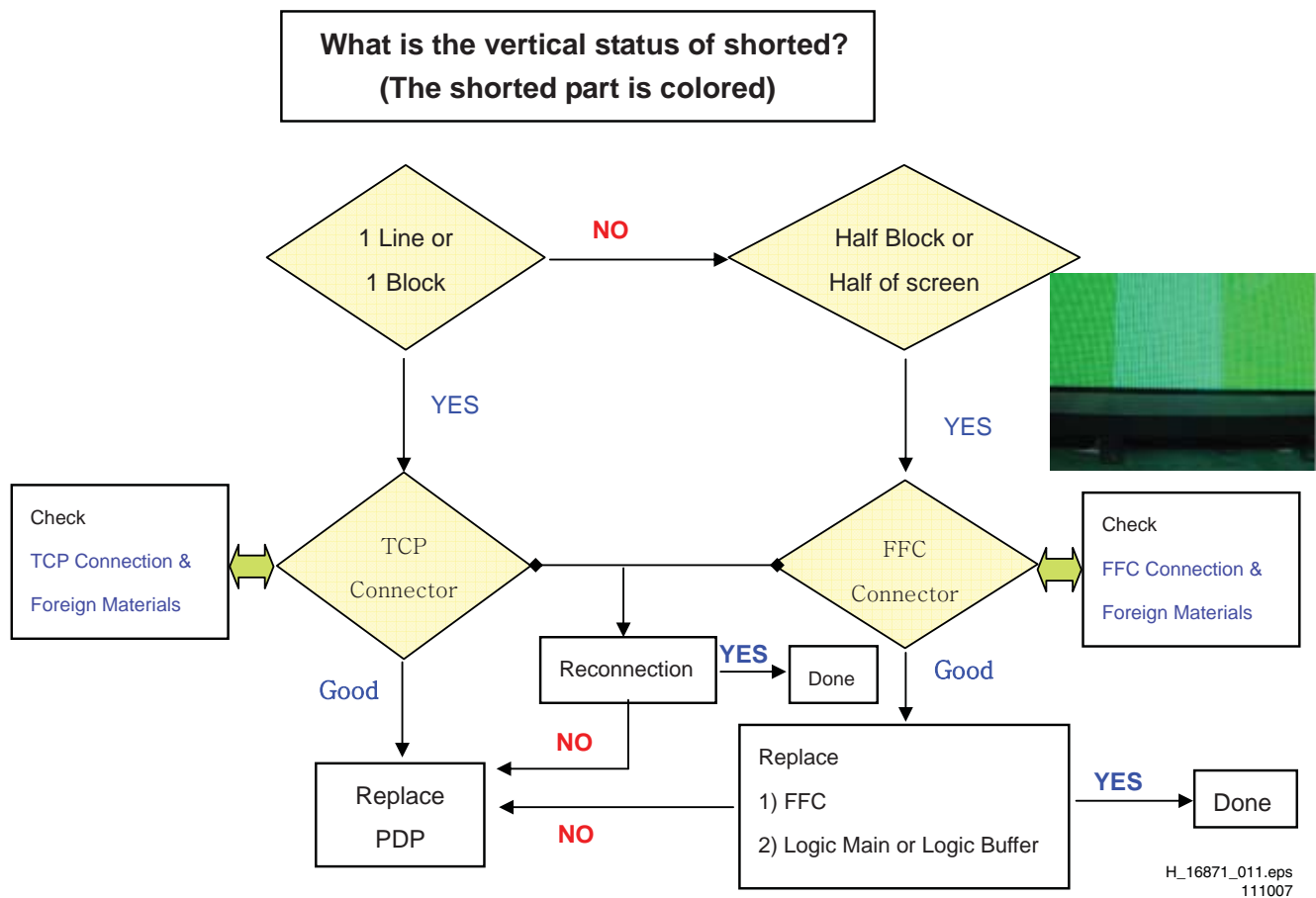


Figure 5-37 Fault symptom: "Address short" [2/2]

5.2.8 Criteria for Panel Replacement, due to Defective Panel Cells

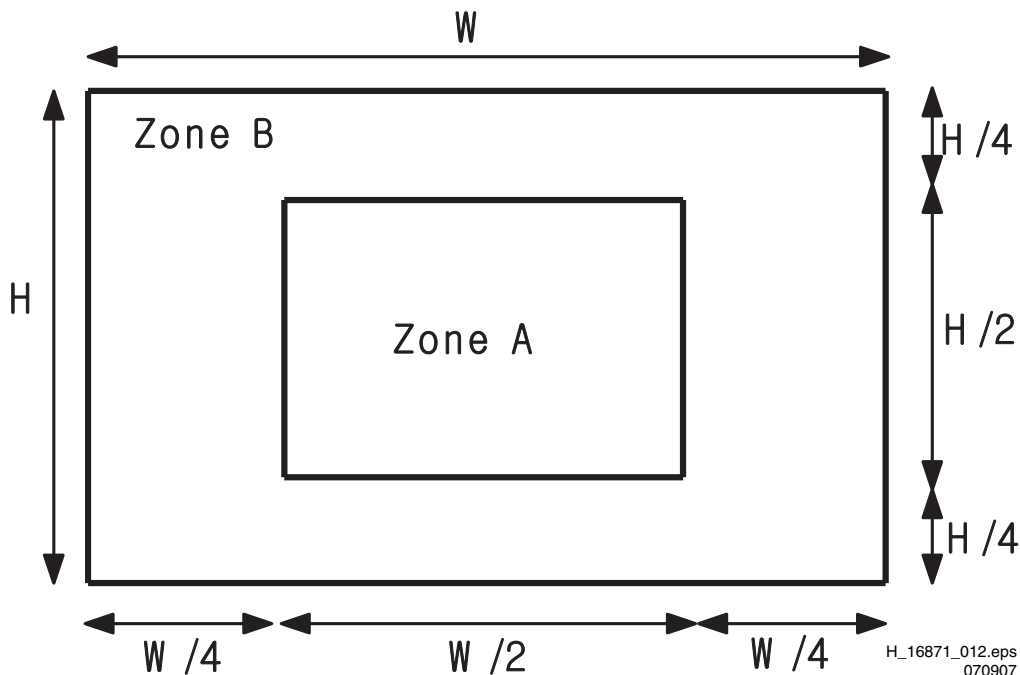


Figure 5-38 Panel zones

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 4 and less Zone B: 8 and less	Regardless of A and B zone, 1 Cell Defect in an area of 50mm*50mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1 and less	
Flickering cell defect	Zone A: 0 Zone B: 1 and less	
High Intensity Cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Adjacent cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Total cell defects	12 and less	

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190606

Figure 5-39 Criteria for panel replacement

5.2.9 Defect Overview

Table 5-2 Defects, symptoms and defective parts

Condition Name	Description	Related Board
No output voltage	Operating voltages don't exist.	SMPS
No display	Operating voltages exist, but no image on screen	Y-MAIN, X-MAIN, Logic Main, Cables
Abnormal display	Abnormal Image (not open or short) is on screen.	Y-MAIN, X-MAIN, Logic Main
Sustain open	Some horizontal lines are missing on screen	Scan Buffer, FPC of X / Y
Sustain short	Some horizontal lines appear to be linked on screen	Scan Buffer, FPC of X / Y
Address open	Some vertical lines are missing on screen	Logic Main, Logic Buffer, FFC, TCP
Address short	Some vertical lines appear to be linked on screen	Logic Main, Logic Buffer, FFC, TCP
Defective panel cells	Some cells seem to be defective	Check criteria for replacement of the panel

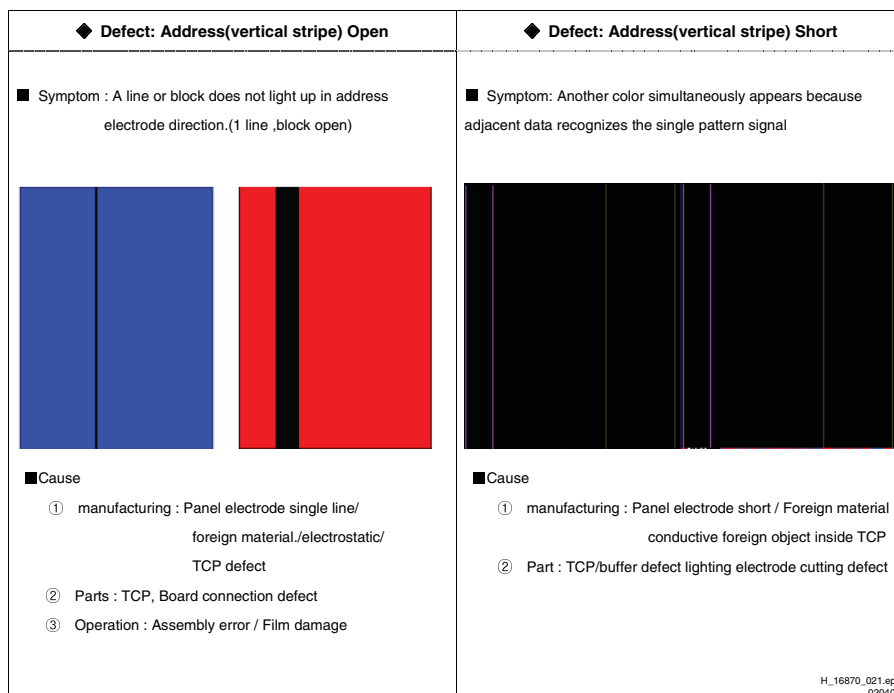


Figure 5-40 Defect overview [1/11]

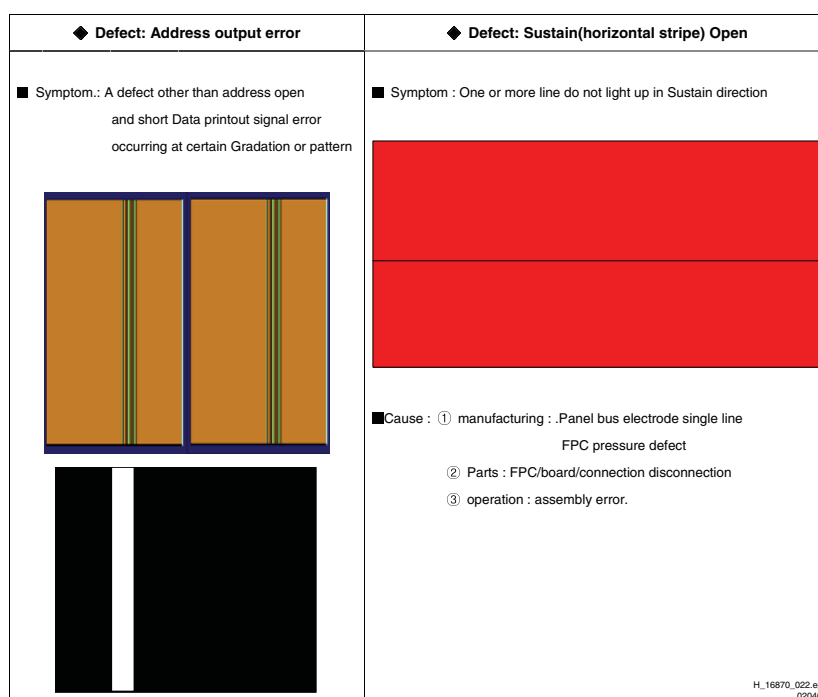


Figure 5-41 Defect overview [2/11]





◆ Defect: Sustain(horizontal stripe) Short	◆ Defect: Dielectric material layer damage
<p>■ Symptom : Combined or adjacent lines are short in sustain direction. The line appear brighter than other at Ramp gradation pattern or low gradation patter</p>   <p>■ Cause</p> <ol style="list-style-type: none"> ① manufacturing : Panel electrode short/Foreign material. ② Parts : Board/ connector/pin error ③ Operation : connector / assembling error 	<p>■ Symptom: Burn caused by the damage of address bus dielectric layer appears in the panel discharge/non discharge area. sustain also open/short occurs by the damage of address sustain printout</p>  <p><Add Block and Line Open></p>  <p><Add and Sustain Open></p> <p>■ Cause : layer uneven / abnormal voltage / foreign material repair failed</p> <p>H_16870_023.eps 020407</p>

Figure 5-42 Defect overview [3/11]





◆ Defect: F/White low discharge	◆ Defect: Weak discharge
<p>■ Symptom : Low discharge caused by unstable cells occurring at full white pattern if high (60 degree) or normal temperature.</p>   <p>■ Cause</p> <ol style="list-style-type: none"> ① Panel : MgO source / dielectric thickness cell pitch/phosphor ② Circuit : drive waveform/ voltage condition 	<p>■ Symptom : Normal discharge but cells appear darker due to weak light emission occurring mainly at low (5 degree) Full white/Red/Green/Blue pattern or gradation pattern</p>   <p>■ Cause</p> <ol style="list-style-type: none"> ① Panel : MgO deposition count and thinckness / aging condition ② Circuit : drive waveform/ voltage condition <p>H_16870_024.eps 020407</p>

Figure 5-43 Defect overview [4/11]

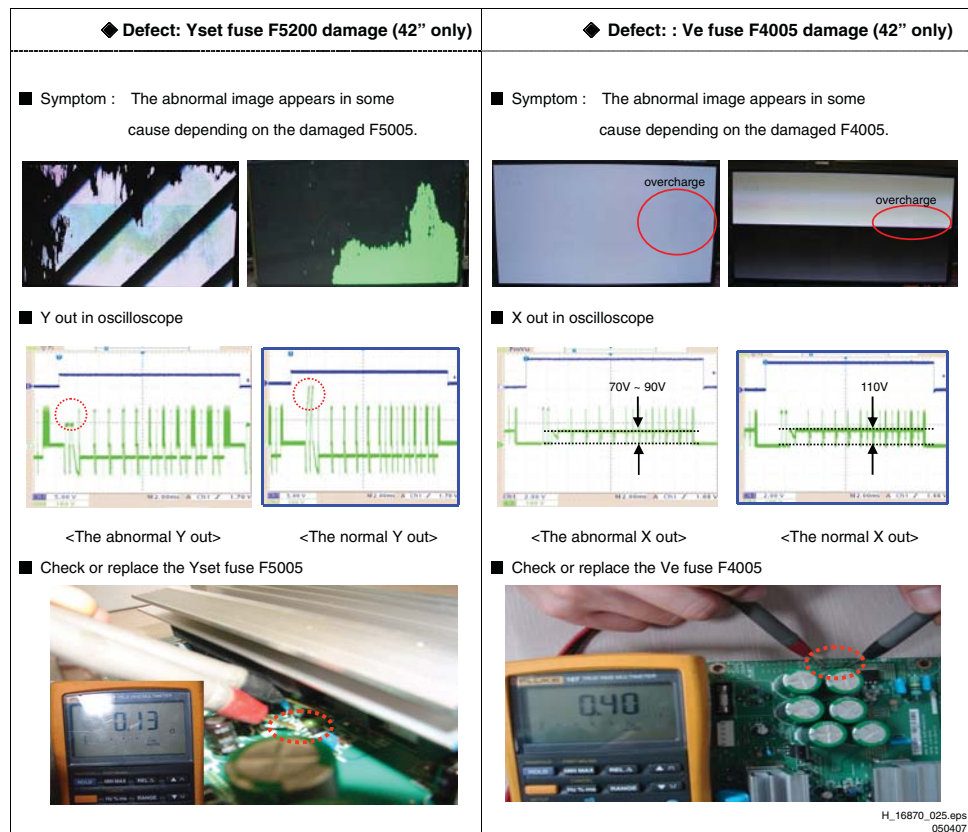


Figure 5-44 Defect overview 42" HD W2 [5/11]

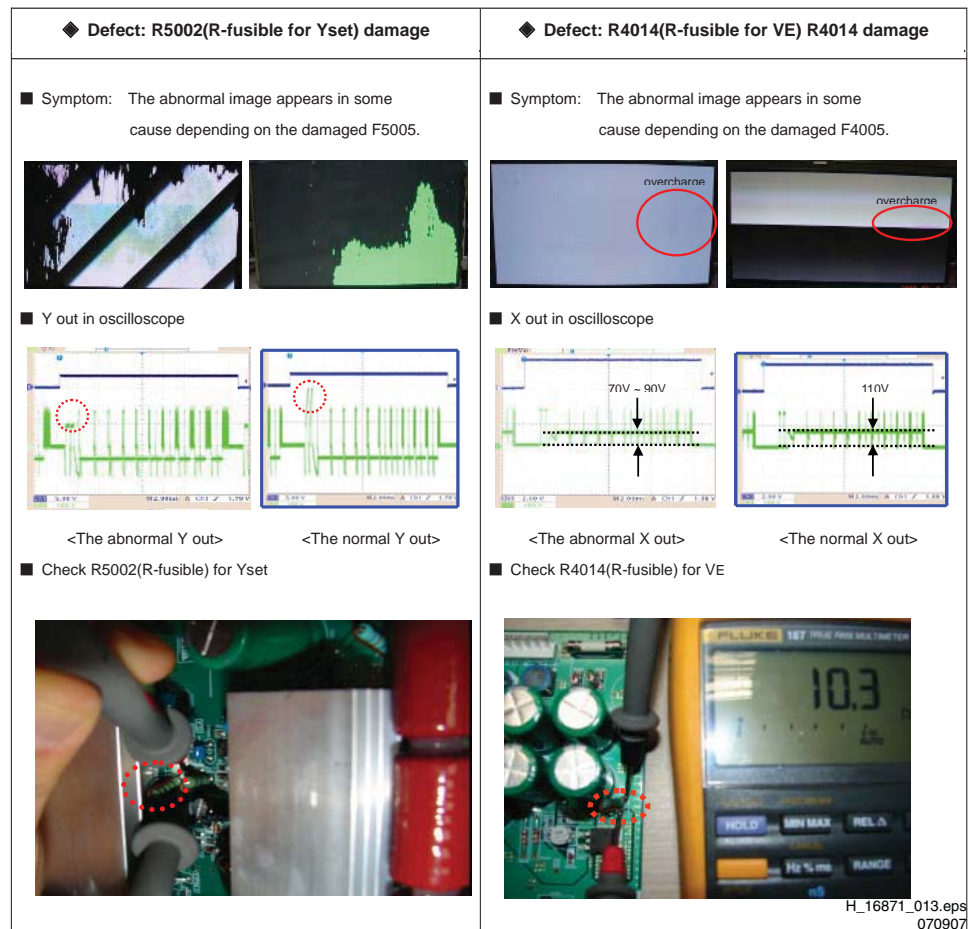

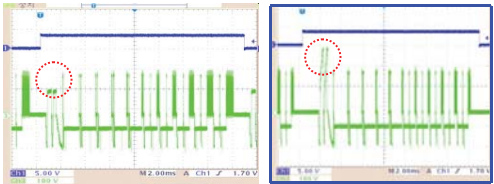

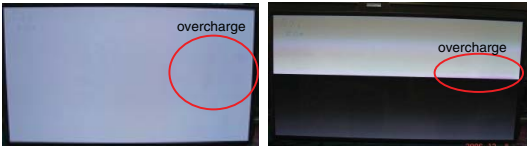
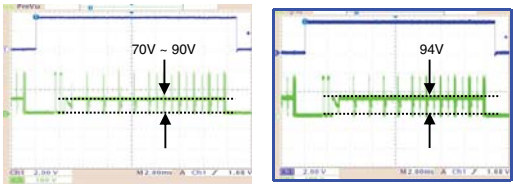
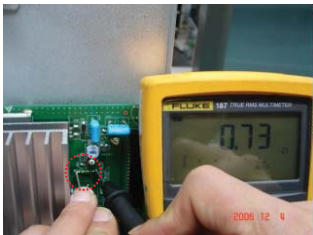
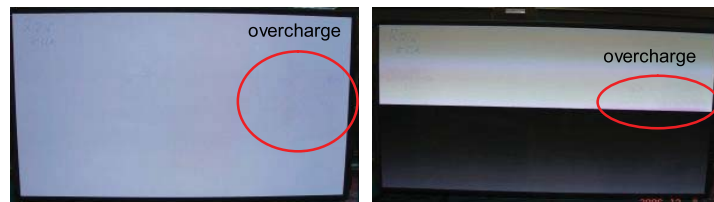


Figure 5-45 Defect overview 42" HD W2 Plus [6/11]

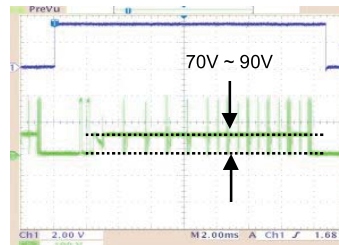
◆ Defect: Yset fuse F5200 damage (50" only)	◆ Defect: : Ve fuse F4800 damage (50" only)
<p>■ Symptom : The abnormal image appears in some cause depending on the damaged F5200.</p>  <p>■ Y out in oscilloscope</p>  <p><The abnormal Y out> <The normal Y out></p> <p>■ Check or replace the Yset fuse F5200</p> 	<p>■ Symptom : The abnormal image appears in some cause depending on the damaged F4800.</p>  <p>■ X out in oscilloscope</p>  <p><The abnormal X out> <The normal X out></p> <p>■ Check or replace the Ve fuse F4800</p> 

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030407

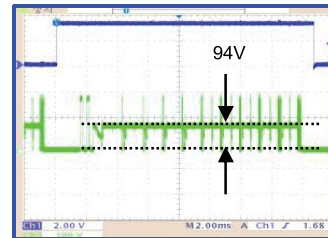
Figure 5-46 Defect overview 50" HD W2 [7/11]



■ X out in oscilloscope



<The abnormal X out>



<The normal X out>

■ Check or replace the Ve fuse F4800

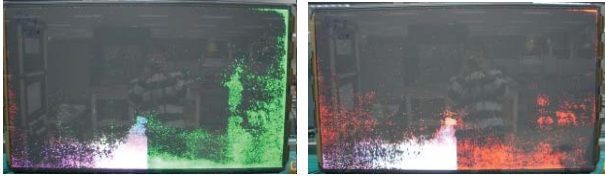


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191007

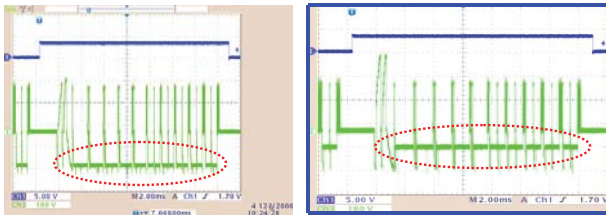
Figure 5-47 Defect overview 50" HD W2 Plus [8/11]

◆ Defect: Vscl voltage output is abnormal (50" only)

- Symptom : The abnormal image appears in some cause depending on abnormal Vscl voltage.



■ Y out in oscilloscope



<The abnormal Y out>

<The normal Y out>

- Check the Vscl voltage or replace the Y-Board



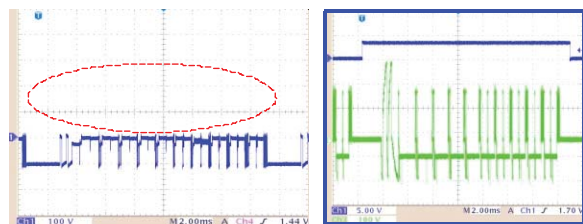
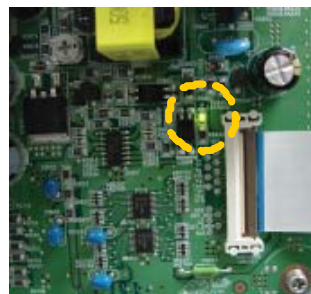
◆ Y-MAIN Protection Check (50" only)

■ Protection circuit

- Voltage Sensing : The important voltage sensing circuit
- Protection : This circuit compares Vref and each voltage using comparator
- Interface : DC/DC circuit which is connected with Photo-coupler, SCR
- Reporting : LED(Green) light on

■ Protection circuit behaviors

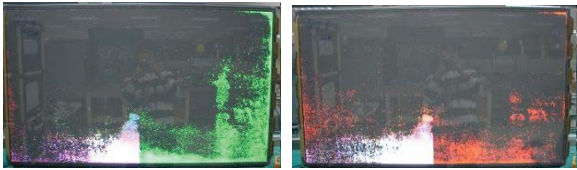
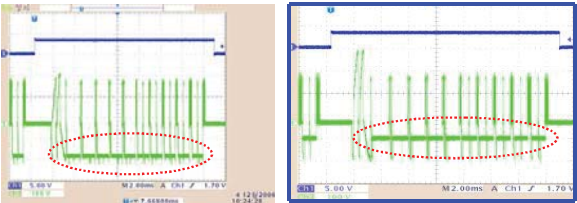
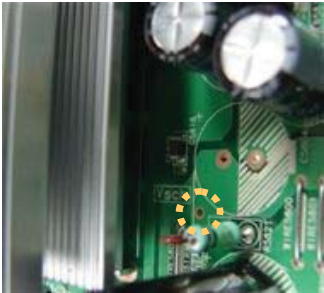

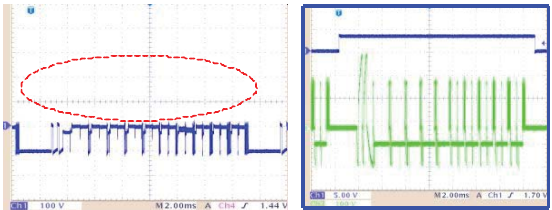
- Enable Circuit : This circuit enables protection circuit using Verc voltage
- Enable : (High, Verc> about 60V)
- Voltage sensing : Verc, Vscl, Vscl voltage sensing
 - Verc>130V(Normal 100V)
 - Vscl>-165V(Normal -190V)
 - Vscl<-100V(Normal -70V)
- Each comparator enables the protection circuit if any voltage is abnormal because this consists with AND Logic
- If SCR is enable DC/DC Controller(MR4710) F/B voltage is low(0.7V) and Vscl, Vscl, Vccf voltage is 0 level.
- Ypn, Ysc, Yfr, Scan I.C's behaviors stops and no display
- Protection reporting through LED lighting



The Protection Y out

The normal Y out

Figure 5-48 Defect overview 50" HD W2 [9/11]

<p>◆ Defect: Vscl voltage output is abnormal</p>	<p>◆ Y-MAIN Protection Check</p>
<p>■ Symptom : The abnormal image appears in some cause depending on abnormal Vscl voltage.</p>  <p>■ Y out in oscilloscope</p>  <p><The abnormal Y out> <The normal Y out></p> <p>■ Check the Vscl voltage or replace the Y-Board</p> 	<p>■ Protection circuit</p> <ul style="list-style-type: none"> - Voltage Sensing : The important voltage sensing circuit - Protection : This circuit compares the Vref and each voltage using comparator - Interface : DC/DC circuit which is connected with Photo-coupler, SCR - Reporting : LED(Green) light on <p>■ Protection circuit behaviors</p> <ul style="list-style-type: none"> - Enable Circuit : This circuit enables protection circuit using Verc voltage - Enable : (High, Verc> about 60V) - Voltage sensing : Verc, Vscl, Vscl voltage sensing <ul style="list-style-type: none"> Verc>130V(Normal 100V) Vscl>-165V(Normal -190V) Vscl<-100V(Normal -70V) - Each voltage comparator enables the protection circuit if any voltage is OVP because this consists with AND Logic - If SCR is enable DC/DC Controller(MR4710) F/B voltage is low(0.7V) and Vscl, Vscl, Vccf voltage is 0 level. - Ypn, Ysc, Yfr, Scan I.C's behaviors stops and no display appears - Protection reporting through LED lighting   <p>The Protection Y out The normal Y out</p>

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Figure 5-49 Defect overview 50" HD W2 Plus [10/11]

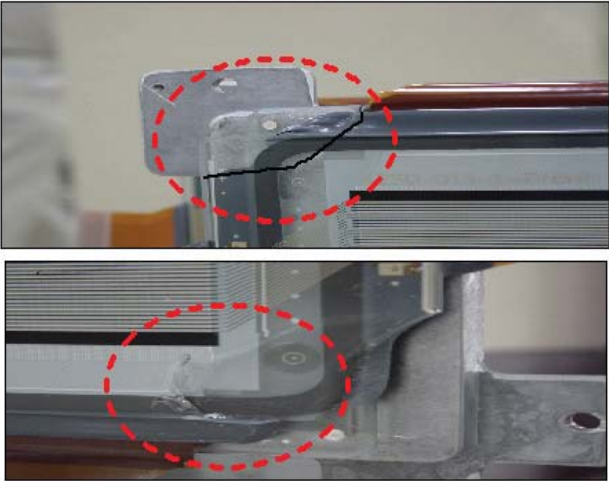
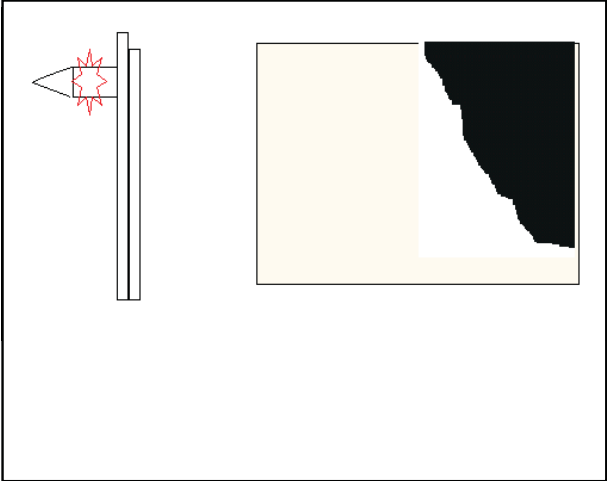
◆ Defect : panel damage	◆ Defect: Exhaust pipe damage
<p>■ Symptom : Panel crack or break. No image appears in some cause depending on the damaged parts and damage level.</p>  <p>■ Cause</p> <ul style="list-style-type: none"> ① Manufacturing : Flatness/palette pin interruption ② Operation : overload of panel corner / careless handling ③ Panel : Flatness / assembly error 	<p>■ Symptom. : Crack in break if exhaust pipe an image is partially lacking or the panel noise occurs depending on the damaged parts and with the passage of time</p>  <p>■ Cause : Careless panel handling</p> <p style="text-align: right;">H_16870_060.eps 130407</p>

Figure 5-50 Defect overview [11/11]

5.3 Defect Description Form

This form must be used by the workshops for warranty claims:

Defect Description Form LCD PLASMA v4.0 final				Date last modified: 28/03/2006	
To be filled in by <u>WORKSHOP / WORK CENTER</u>					
Country:	PHILIPS LCD & Plasma <u>DEFECT DESCRIPTION</u> <u>FORM</u>		Type nr./Model nr. set		
Customer Account nr.:			Serial nr. set		
Job sheet nr.:			Type nr. display		
			Serial nr. display		
		Part nr display (12nc)			
		Return number			
GENERAL REPAIR DATA	Condition	<input type="checkbox"/> Constantly <input type="checkbox"/> Intermittently <input type="checkbox"/> After a while <input type="checkbox"/> In hot environment <input type="checkbox"/> In cold environment Other: <div style="border: 1px solid black; height: 20px; width: 100%; margin-top: 5px;"></div>			
	Symptom(s)	<input type="checkbox"/> No backlight <input type="checkbox"/> No picture <input type="checkbox"/> Picture too bright <input type="checkbox"/> Scratches (LCD only acc. Pixel criteria sheet V4.0) <input type="checkbox"/> Only partial picture <input type="checkbox"/> Unstable picture <input type="checkbox"/> Flickering / flashing picture <input type="checkbox"/> Lines across/down image <input type="checkbox"/> Inactive row(s) <input type="checkbox"/> Inactive column(s) <input type="checkbox"/> Missing colour(s) <input type="checkbox"/> Light leakage Other: <div style="border: 1px solid black; height: 60px; width: 100%; margin-top: 5px;"></div>			
PANEL REPAIR	Pixel Defect(s):	Dark dots Bright dots	<u>Qty of dots:</u>	Mark Defect(s):	
	Symptoms <u>Out of warranty</u>	Following defect symptoms are out of warranty: <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> - Broken glass / Broken polarizer - Scratch(es) on display / polarizer </div> <div style="width: 45%;"> - Number of dark/bright pixels within spec. - Burn in (Plasma TV) / Sticking image (LCD TV) - MURA </div> </div>			These symptoms are not claimable.
BOARD REPAIR	Defect Board		New Board		
	Spare Part Nr.	Serial Nr.	Spare Part Nr.	Serial Nr.	
	1.				
	2.				
	3.				
	4.				
Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected.					
Owner: PHILIPS CE EUROSERVICE					

DE10WEG

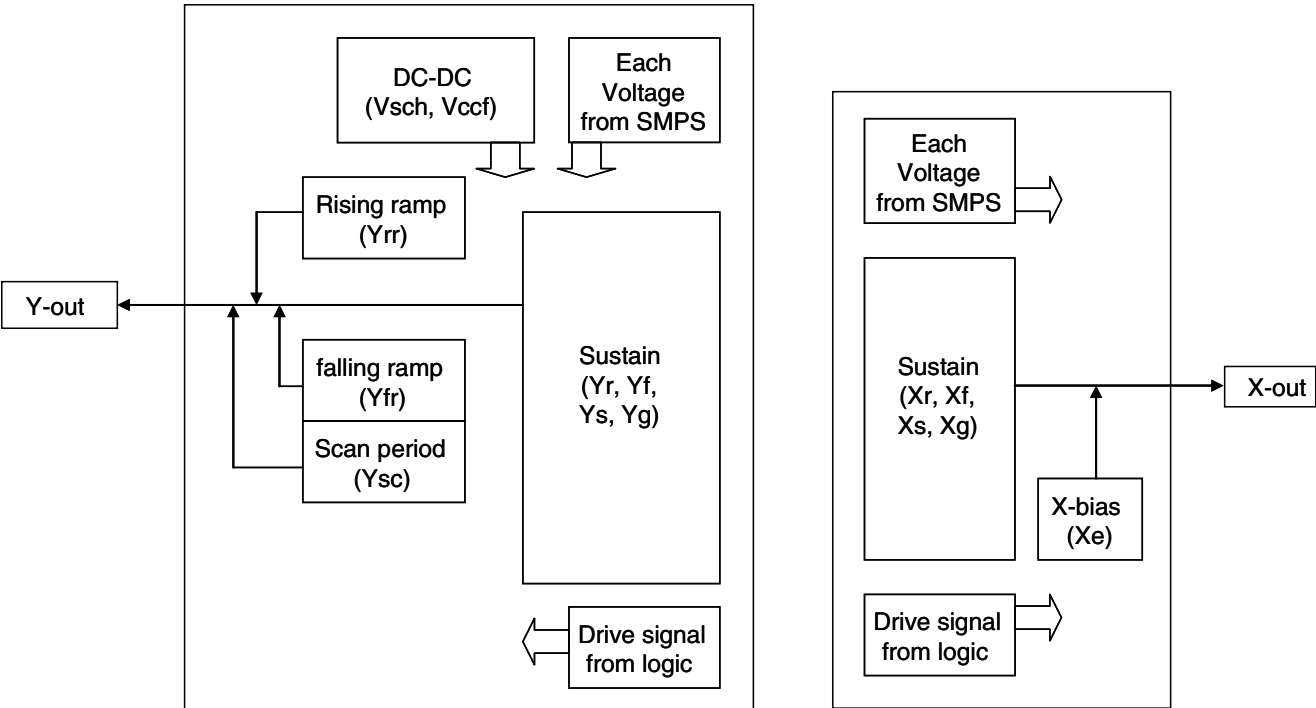
F_15590_115.eps
050407

Figure 5-51 Defect Description Form (DDF)

6. Block Diagrams, Test Point Overview, and Waveforms

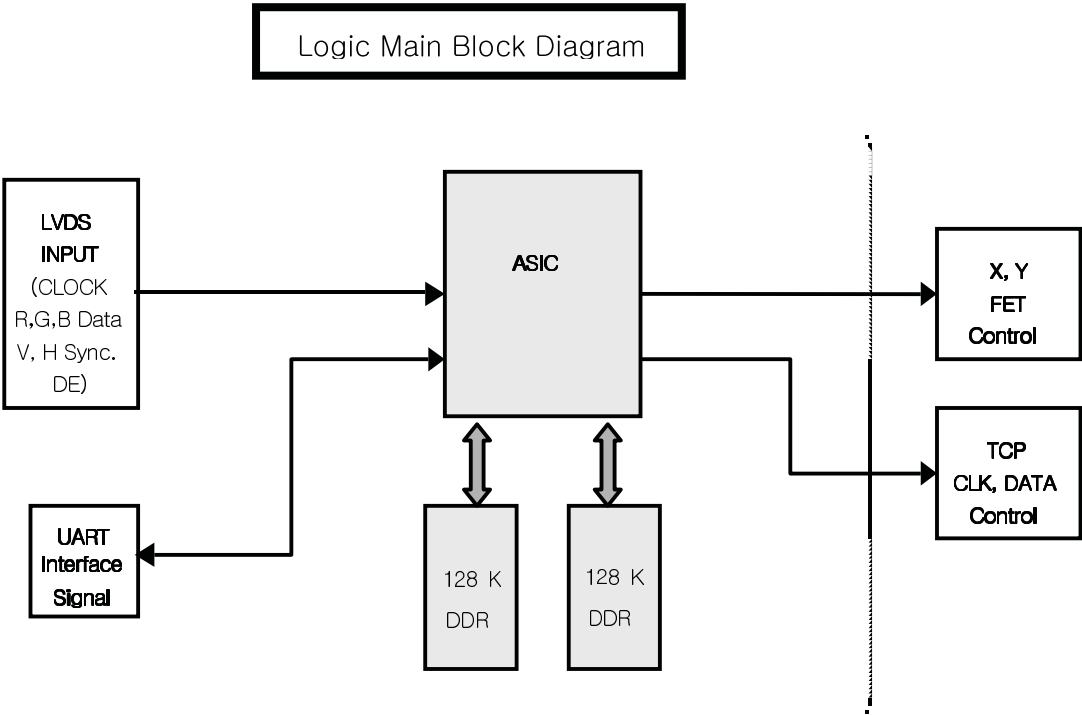
Index of this chapter:
6.1 Block Diagrams

6.1 Block Diagrams



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Figure 6-1 Block diagram “Driver” circuits: Y-Main (left) and X-Main (right)



H_16870_004.eps
050407

Figure 6-2 Block diagram “Logic Main” circuit

7. Circuit Diagrams and PWB Layouts

Not applicable.

8. Alignments

- Index of this chapter:
- 8.1 Power Supply Voltages
 - 8.2 Alignments 42" HD W2
 - 8.3 Alignments 42" HD W2 Plus
 - 8.4 Alignments 50" HD W2 & 50" HD W2 Plus

Note:

- Figures can deviate due to the different model executions.

Important: Remove all non-default jumpers and reset all DIP switches, after the repair!

8.1 Power Supply Voltages

8.1.1 PSU Layout

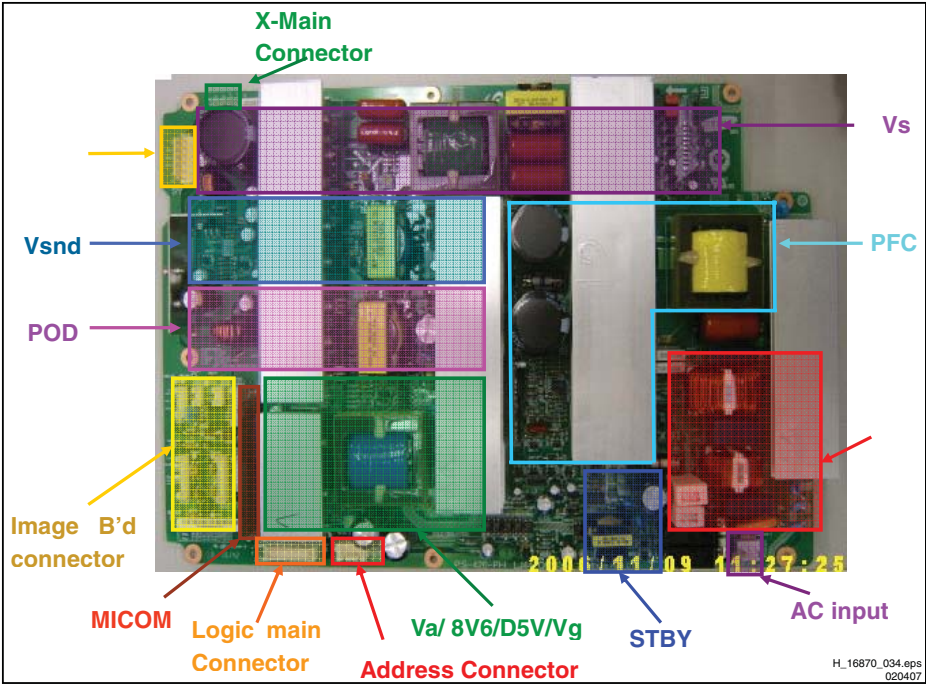


Figure 8-1 PSU layout 42" HD W2

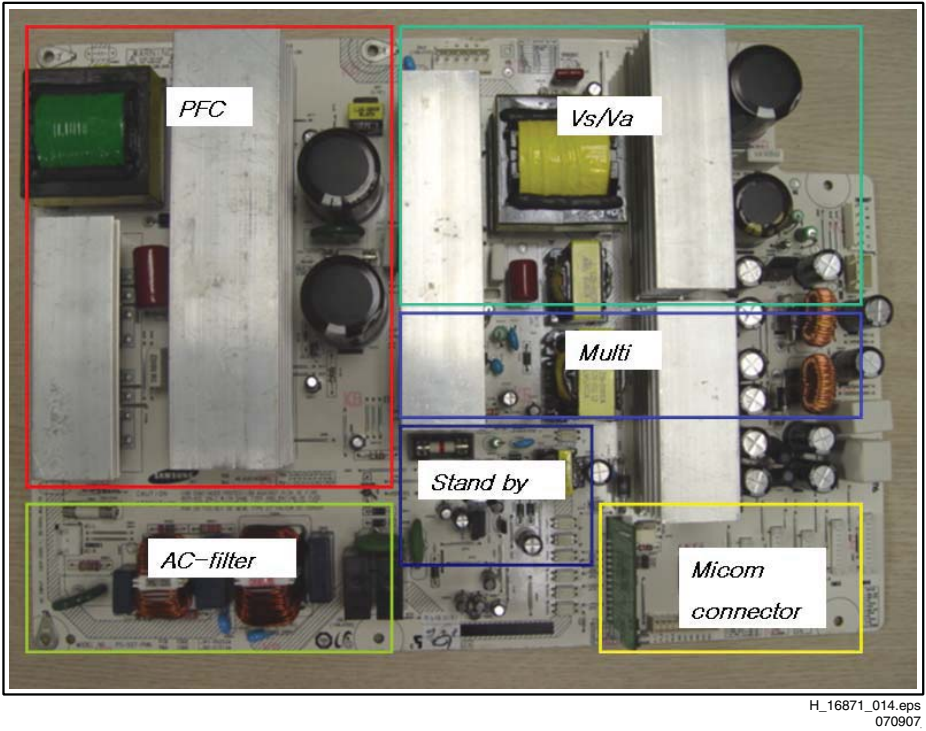


Figure 8-2 PSU layout 42" HD W2 Plus

8.1.2 Adjustment Power Supply Voltages 42" HD W2

Table 8-1 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	205 V ± 1.5%	200 V ~ 207 V
2	VA	63 V ± 1.5%	60 V ~ 65 V
3	VE	110 V ± 1.5%	100 V ~ 120 V
4	VSCAN	-190 V ± 1.5%	-200 V ~ -185 V
5	VG	15 V ± 5%	Fixed
6	D5VL	5.2 V ± 5%	Fixed

Check voltage label on the PDP for correct values.

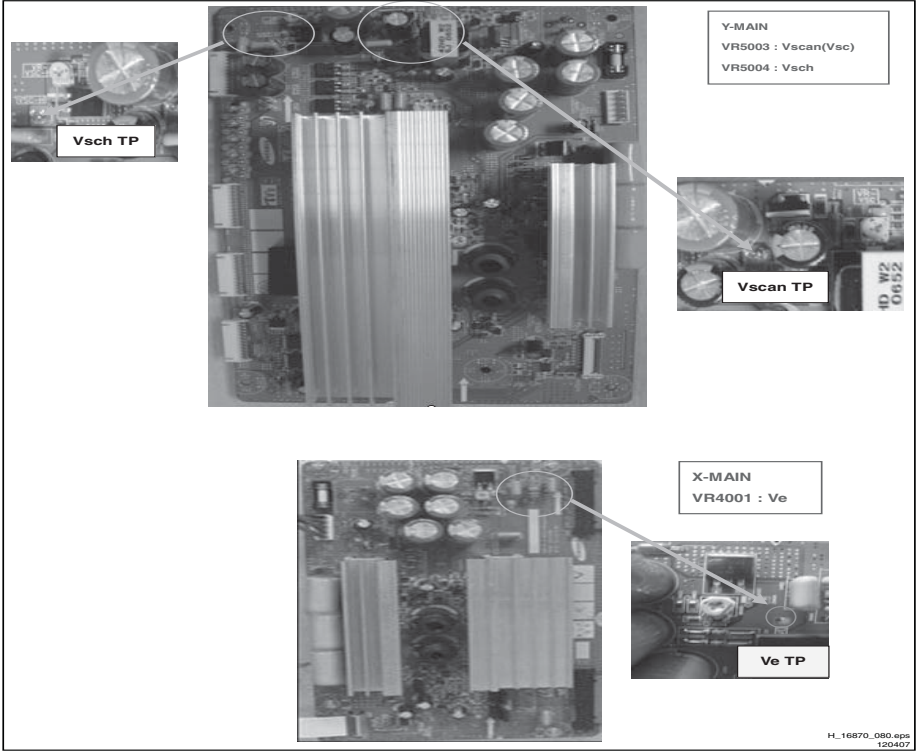


Figure 8-5 Location of voltage check points - 42" HD W2

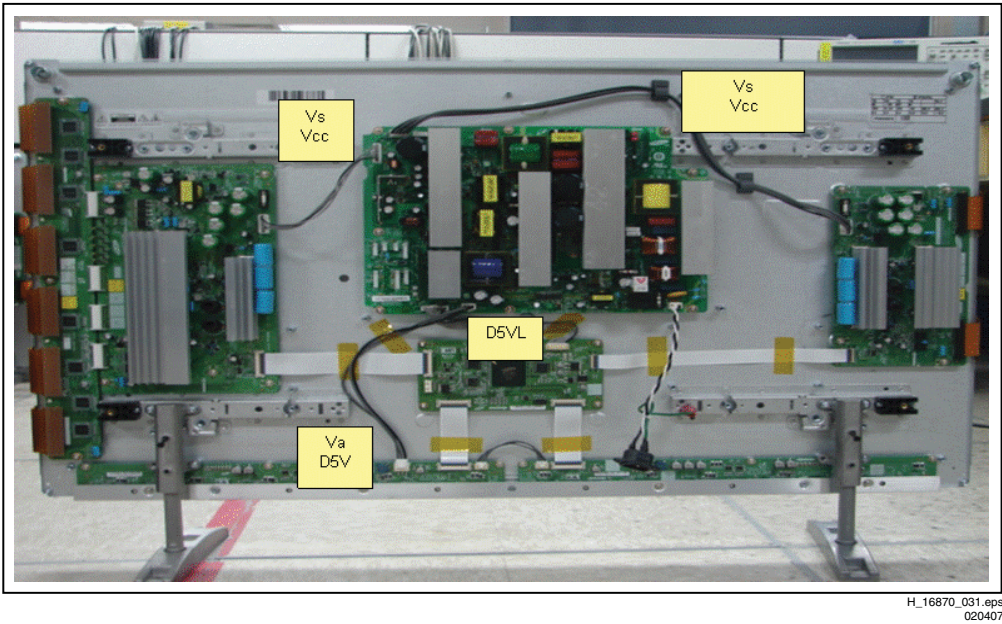


Figure 8-6 Location of the supply lines from the PSU to the boards - 42" HD W2

8.1.3 Adjustment Power Supply Voltages 42" HD W2 Plus

Table 8-2 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	205 V \pm 1.5%	200 V ~ 215 V
2	VA	63 V \pm 1.5%	61 V ~ 65 V
3	VE	99 V \pm 1.5%	95 V ~ 105 V
4	VSCAN	-190 V \pm 1.5%	-195 V ~ -185 V
5	VG	15 V \pm 5%	Fixed
6	D5VL	5.2 V \pm 5%	Fixed

Check voltage label on the PDP for correct values.

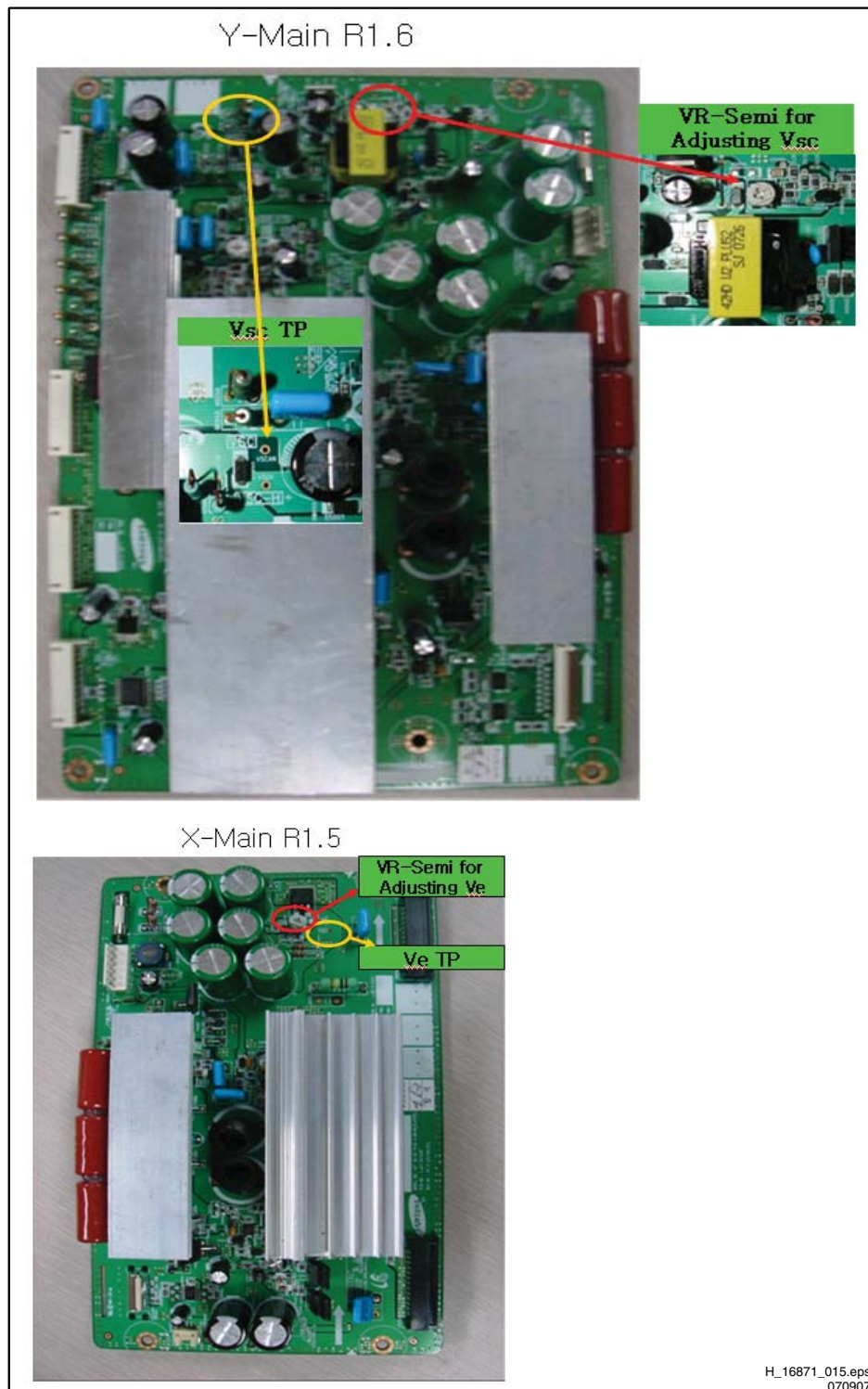
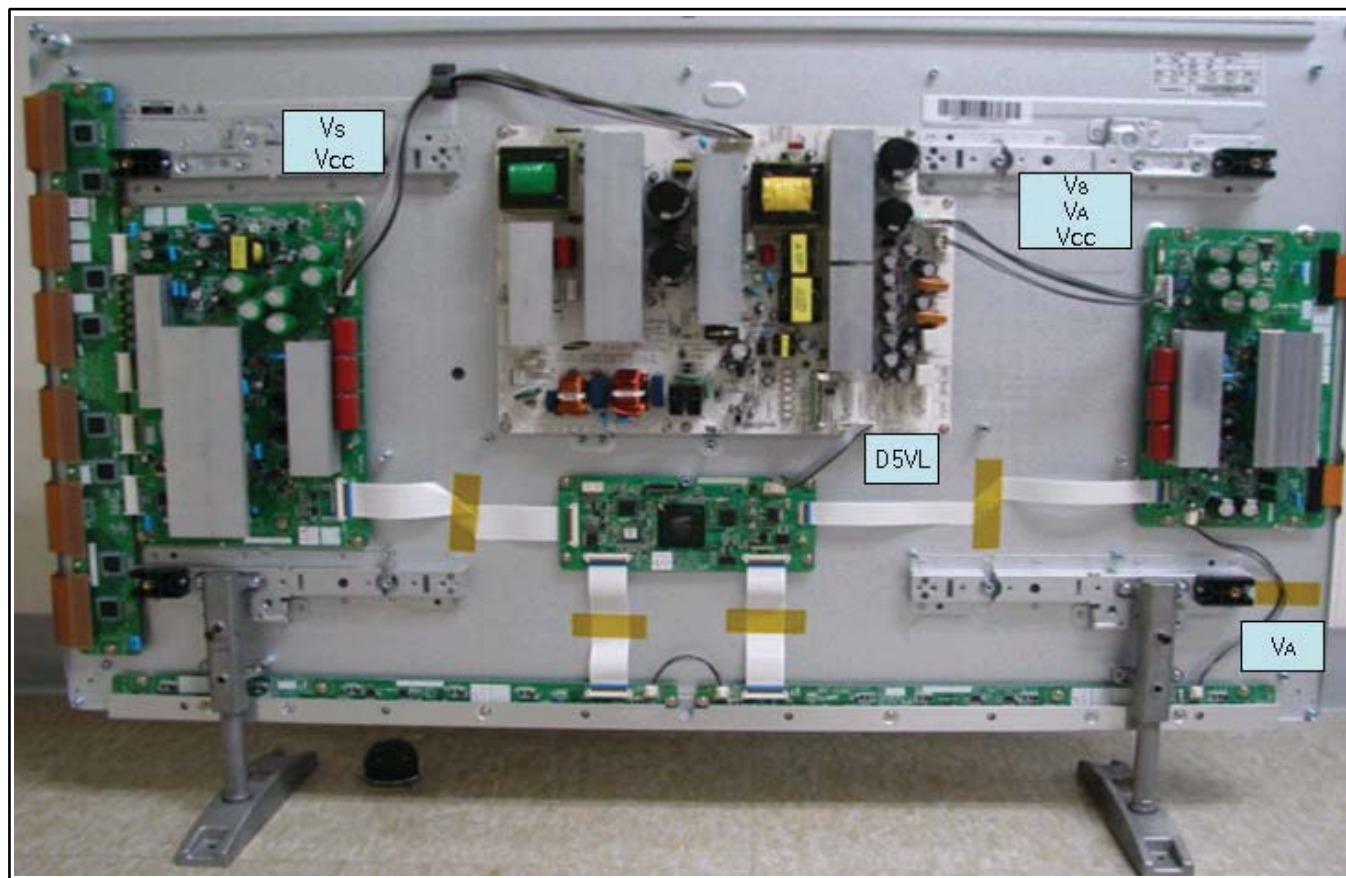


Figure 8-7 Location of voltage check points - 42" HD W2 Plus



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070907

Figure 8-8 Location of the supply lines from the PSU to the boards - 42" HD W2 Plus

8.1.4 Adjustment Power Supply Voltages 50" HD W2

Table 8-3 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	207 V \pm 1.5%	198 V ~ 202 V
2	VA	63 V \pm 1.5%	63 V ~ 67 V
3	VE	94 V \pm 1.5%	105 V ~ 115 V
4	VSCAN	-190 V \pm 1.5%	-192 V ~ -188 V
5	VG	15 V \pm 5%	Fixed
6	D5VL	5.2 V \pm 5%	Fixed

Check voltage label on the PDP for correct values.

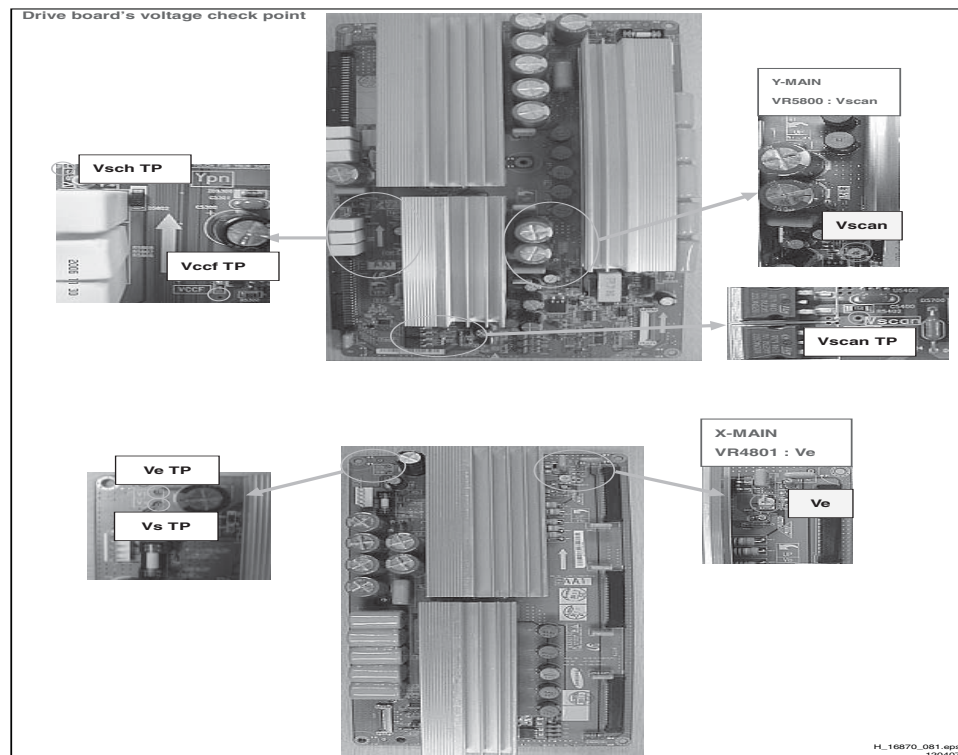


Figure 8-9 Location of the voltage check points - 50" HD W2

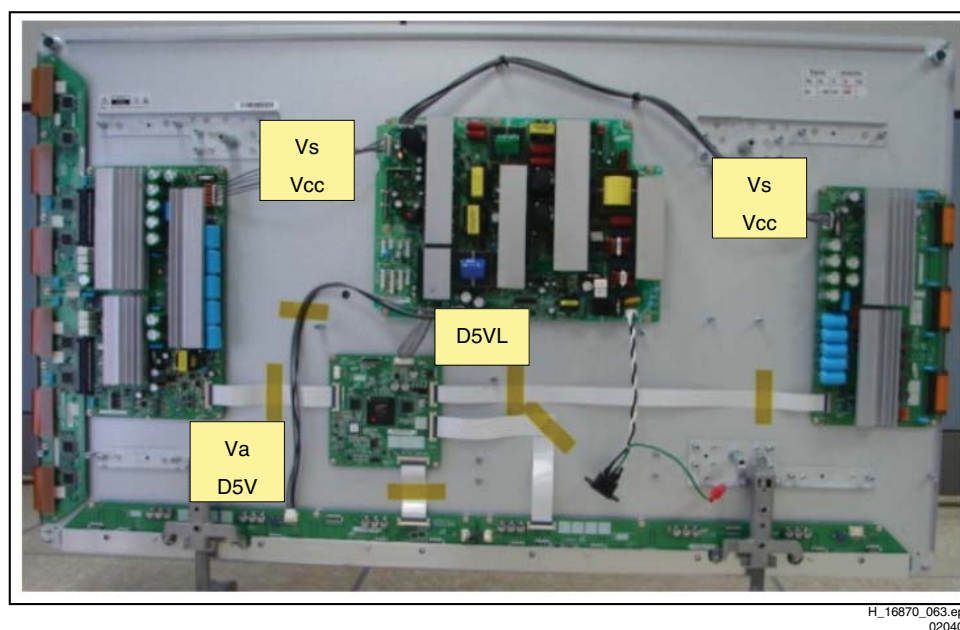


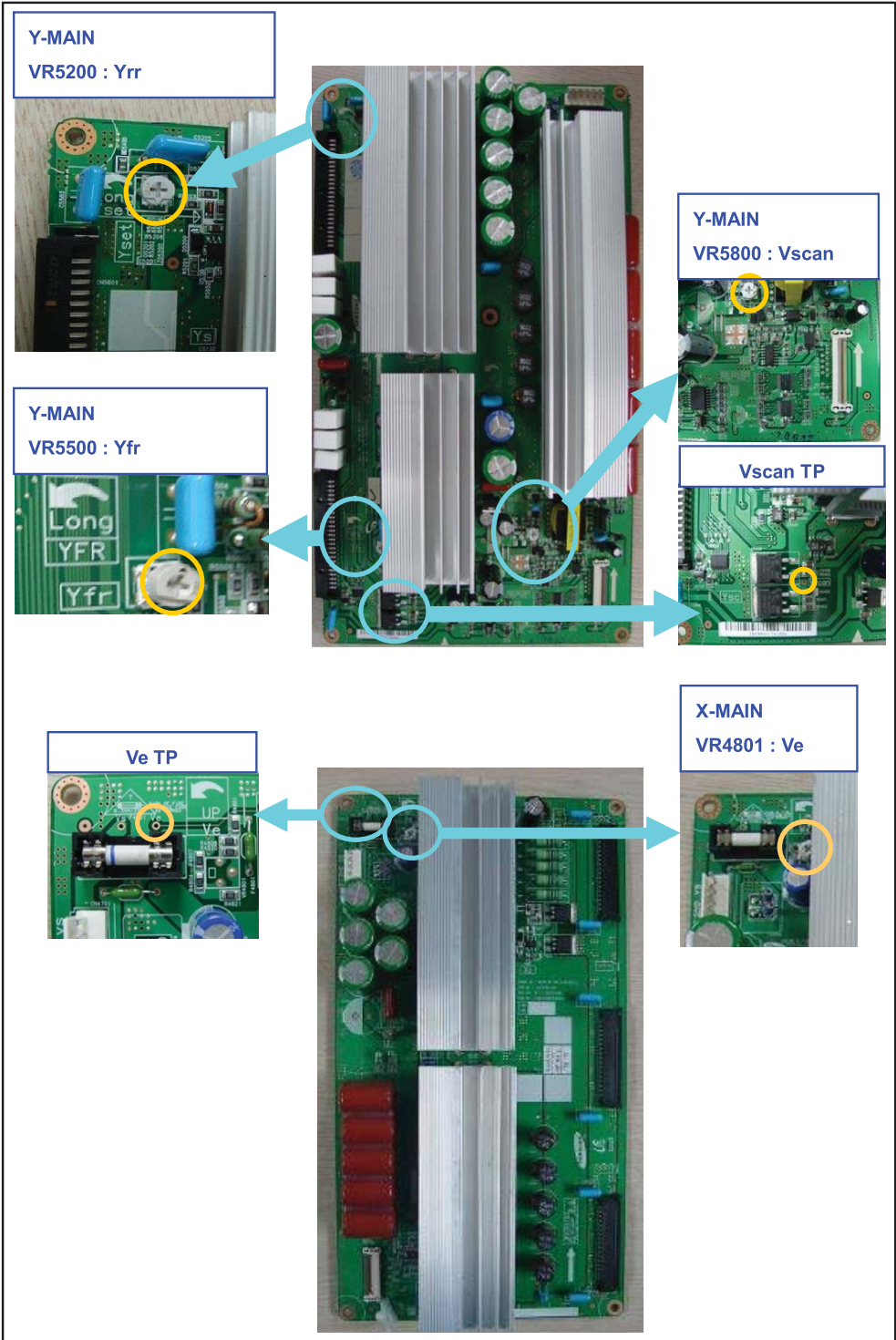
Figure 8-10 Location of the supply lines from the PSU to the boards - 50" HD W2

8.1.5 Adjustment Power Supply Voltages 50" HD W2 Plus

Table 8-4 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

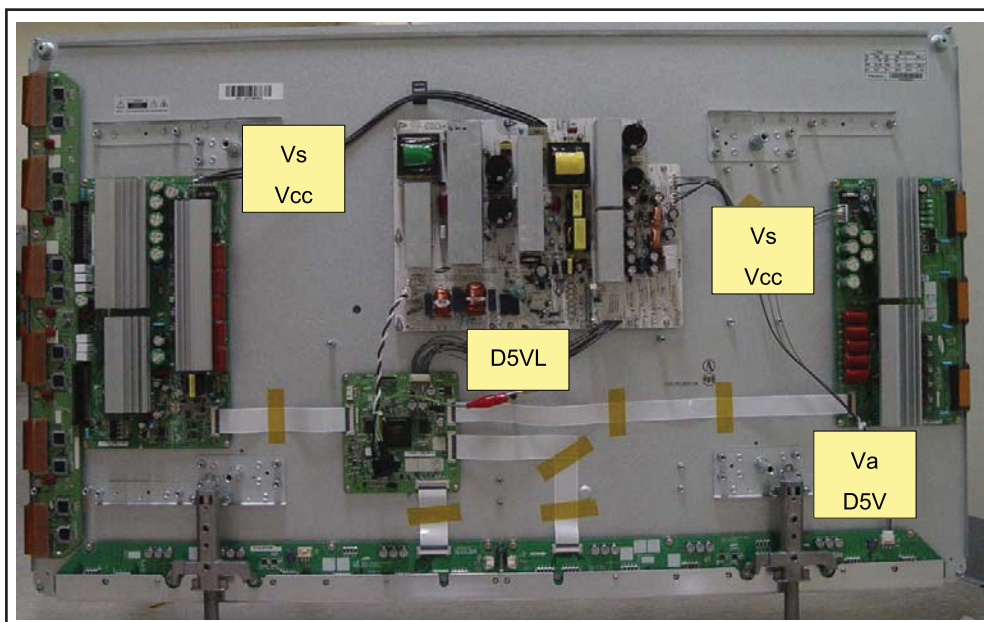
No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	207 V ± 1.5%	200 V ~ 215 V
2	VA	63 V ± 1.5%	Fixed
3	VE	94 V ± 1.5%	105 V ~ 115 V
4	VSCAN	-190 V ± 1.5%	-192 V ~ -188 V
5	VG	15 V ± 5%	Fixed
6	D5VL	5.3 V ± 5%	Fixed

Check voltage label on the PDP for correct values.



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191007

Figure 8-11 Location of the voltage check points - 50" HD W2 Plus



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191007

Figure 8-12 Location of the supply lines from the PSU to the boards - 50" HD W2 Plus

8.2 Alignments 42” HD W2

8.2.1 Quick Check

For a quick check on the correct Y-main waveform alignment, use the following method: Check the position of the potmeter VR5003 [1]. If it points in this direction [2], use a trimmer [3] to return it to the correct position [1].

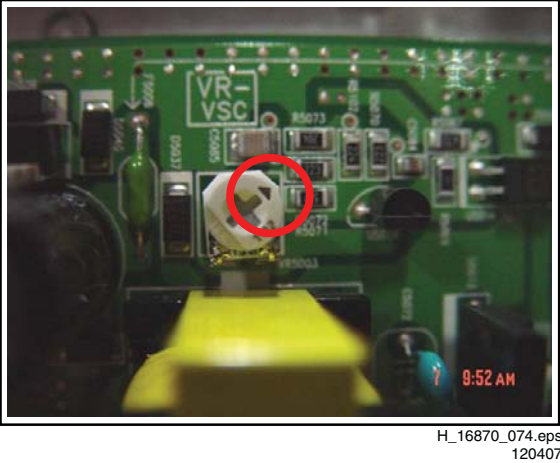


Figure 8-13 Correct position of VR5003 [1]

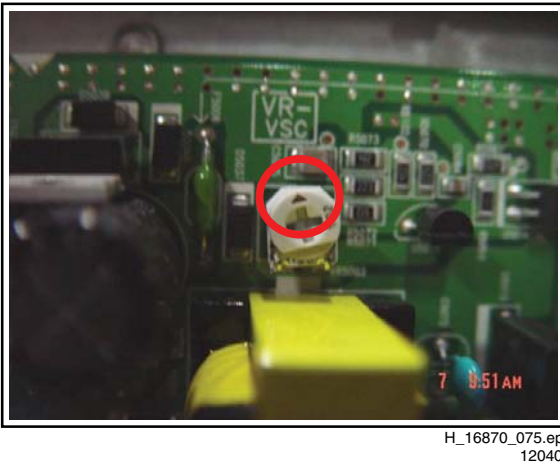


Figure 8-14 Wrong position of VR5003 [2]

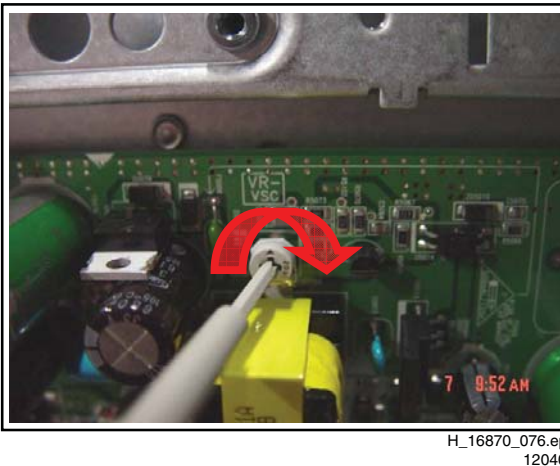


Figure 8-15 Changing of VR5003 [3]

8.2.2 For Reference Only

- If the quick check does not solve the issue, perform the following alignments:
- Set the pattern to “Full White”:
 - Place jumper CN2013 (pins 3 and 4) on the Logic Board
 - The display starts showing a cycle of different patterns. At the moment the “full white” pattern is visible, remove the jumper. Now the display shows a continuous full white pattern. To restart the cycle of different patterns, replace the jumper.
 - Check the waveform using an oscilloscope (see figures “Adjusting waveforms - 42” HD W2”).
 - Trigger via V_TOGG on the LOGIC Board (see figure “Logic PWB 42” HD W2”).
 - Connect the “CN5411” test point, located at the bottom of the Y-buffer PWB, to the other channel, and then check the first SubField (SF) waveform of one TV-Field.
 - Check the waveform by adjusting the “horizontal division” of the oscilloscope.
 - Check the Reset waveform when the V_TOGG level is changed.
 - Adjust the waveform of the rising ramp with VR5001.
 - Adjust the waveform of the falling ramp with VR5002.

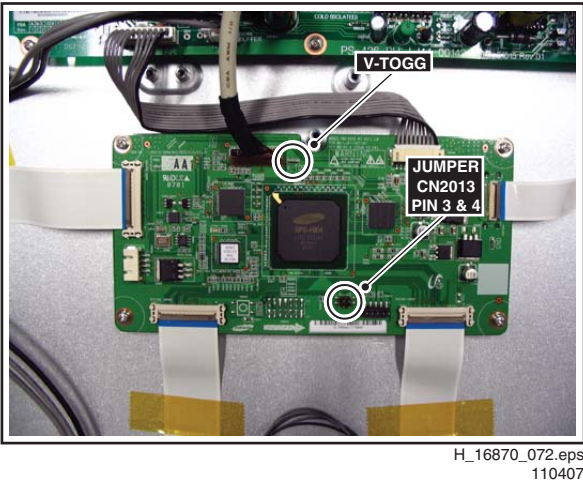


Figure 8-16 Logic PWB - 42” HD W2

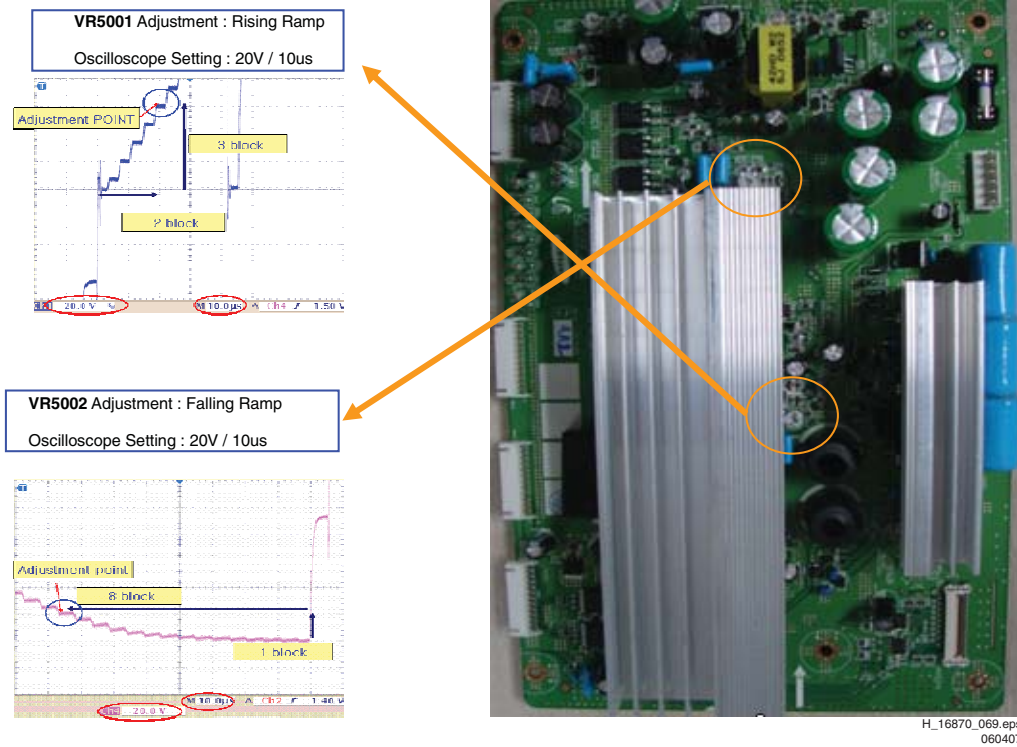
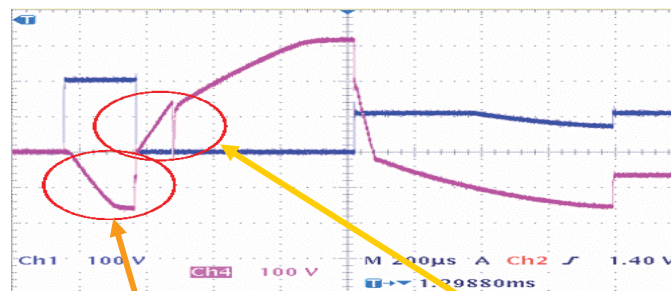


Figure 8-17 Adjusting waveforms - 42" HD W2 [1/2]

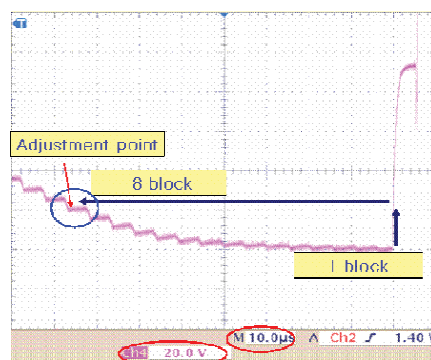


Adjust VR5002 to set the time of Yfr
(Main Reset Falling Ramp) like the
below picture.

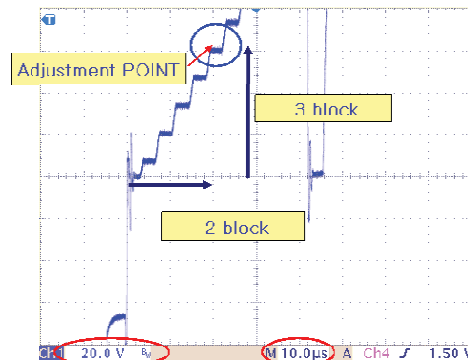
Oscilloscope Setting : 20V / 10us

Adjust VR5001 to set the time of Yrr
(Main Reset Rising Ramp) like the
below picture.

Oscilloscope Setting : 20V / 10us



< Falling Ramp >



< Rising Ramp >

Figure 8-18 Adjusting waveforms - 42" HD W2 [2/2]

8.3 Alignments 42" HD W2 Plus

8.3.1 Quick Check

For a quick check on the correct Y-main waveform alignment, use the following method: Check the position of the potmeter VRsc (scan), see Figure "Correct position of VR for Vsc (scan) on Y-Main". If necessary, use a trimmer to return it to its correct position.

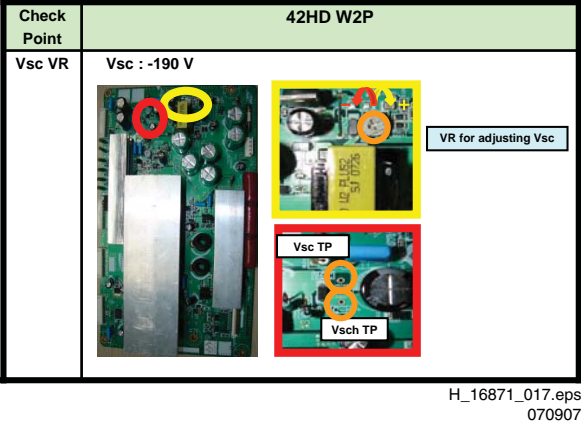


Figure 8-19 Correct position of VR for Vsc (scan) on Y-Main

8.3.2 For Reference Only

If the quick check does not solve the issue, perform the PSU (SMPS) and other alignments, as indicated in alignment pages of the W2 models. The W2 Plus PDP alignments are equivalent to those of the W2 PDP models, but there are some minor differences in the locations of test points and VRs. The differences (locations of test points and VRs) are shown in the photo above and the photos below.

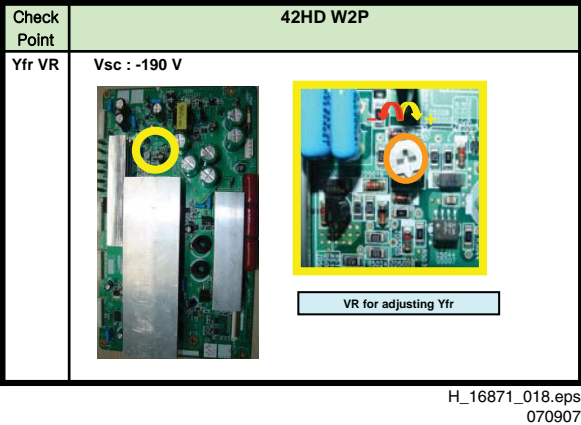


Figure 8-20 Y-Main: Vr for adjusting Yfr

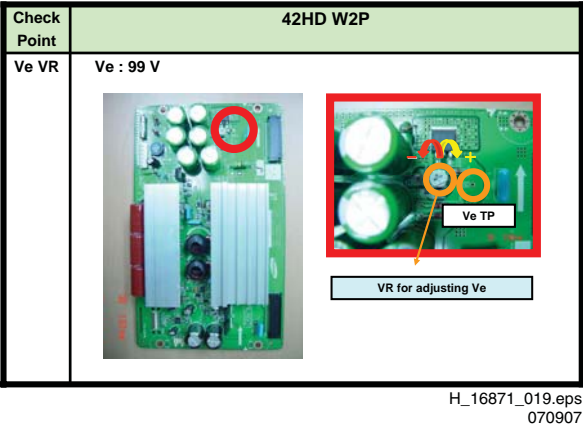


Figure 8-21 X-Main: VR for adjusting Ve

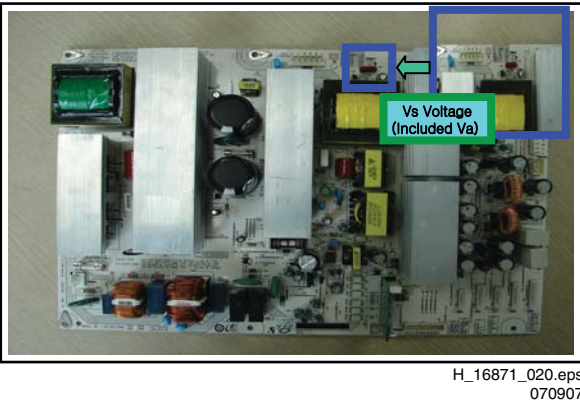


Figure 8-22 SMPS: VR for adjusting Vs

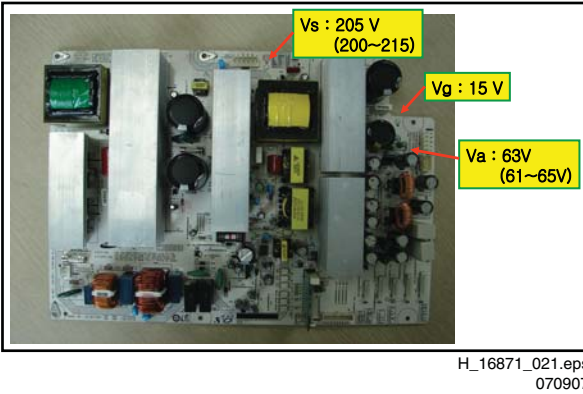


Figure 8-23 SMPS: Voltage measuring points

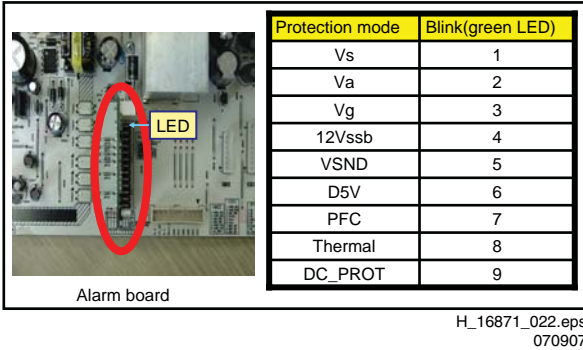
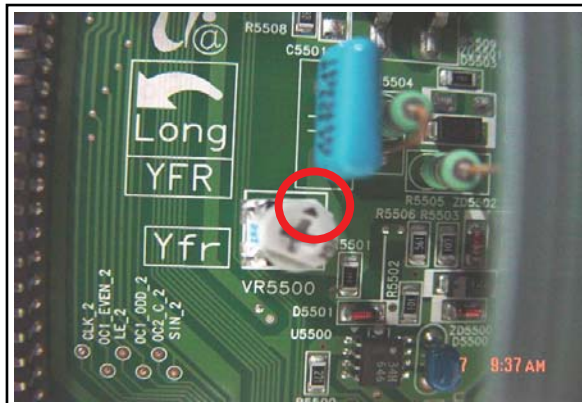


Figure 8-24 SMPS: Protection mode (Display Ramp)

8.4 Alignments 50" HD W2 & 50" HD W2 Plus

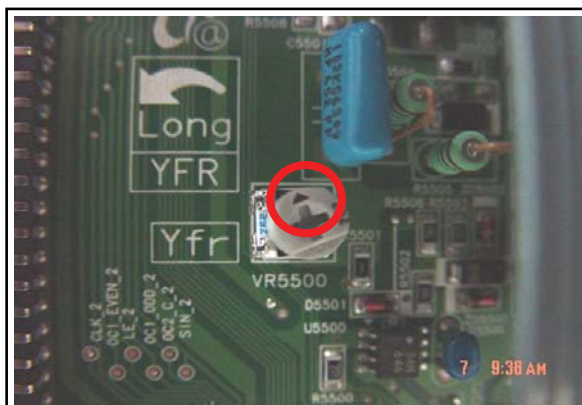
8.4.1 Quick Check

For a quick check on the correct Y-main waveform alignment, use the following method: Check the position of the potmeter VR5500 [1]. If it points in this direction [2], use a trimmer [3] to return it to the correct position [1].



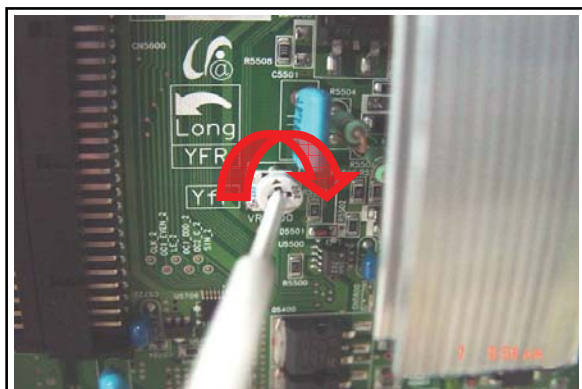
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Figure 8-25 Correct position of VR5500 [1]



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120407

Figure 8-26 Wrong position of VR5500 [2]



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120407

Figure 8-27 Changing of VR5500 [3]

8.4.2 For Reference Only

1. Set the pattern to Full White:
 - Place jumper CN2007 (pins 3 and 4) on the Logic Board
 - When the display starts showing a cycle of different patterns, push button SW2000 for at least one second. Now the display shows a continuous full white pattern. To restart the cycle of different patterns, push the button once more and wait for a few seconds.
2. Check the waveform using an oscilloscope (see figures "Adjusting waveforms - 50" HD W2").
 - Trigger via V_TOGG on the Logic Board (see figure "Logic PWB 50" HD W2").
 - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Sub-Field (SF) waveform of one TV-Field.
 - Check the waveform by adjusting the "horizontal division" of the oscilloscope.
 - Check the waveform when the V_TOGG level is changed.
3. Adjust the waveform of the rising ramp with VR5200.
4. Adjust the waveform of the falling ramp with VR5500.

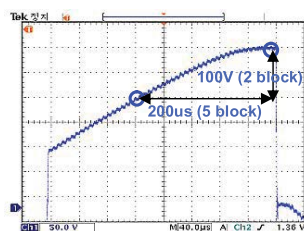


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Figure 8-28 Logic PWB - 50" HD W2

VR5200 Adjustment : Rising Ramp

Oscilloscope Setting : 50V / 40us



VR5500 Adjustment : Falling Ramp

Oscilloscope Setting : 50V / 20us

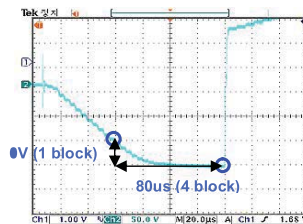
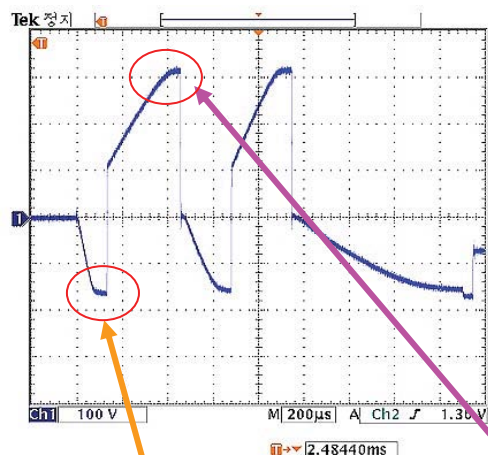


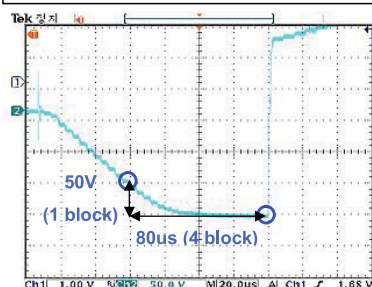
Figure 8-29 Adjusting waveforms - 50" HD W2 & 50 HD W2 Plus [1/2]

W2 Ramp Waveform Inclination Adjustment (Y-Board) - 1st Sub Field



Adjust VR5500 to set the time of Yfr
(Main Reset Falling Ramp) like the
below picture.

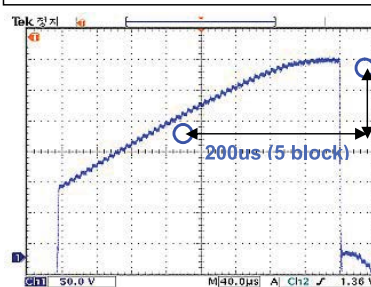
Oscilloscope Setting : 50V / 20us



< Falling Ramp >

Adjust VR5200 to set the time of Yrr
(Main Reset Rising Ramp) like the
below picture.

Oscilloscope Setting : 50V / 40us



< Rising Ramp >

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Figure 8-30 Adjusting waveforms - 50" HD W2 & 50 HD W2 Plus [2/2]

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

- 9.1 Main Function of Each Assembly
- 9.2 Abbreviation List
- 9.3 IC Data Sheets

9.1 Main Function of Each Assembly

9.1.1 X Main Board

The X Main board generates a drive signal by switching the FET and IGBT in synchronization with logic main board timing, and supplies the X electrode of the panel with the drive signal through the connector.

1. Maintain voltage waveforms (including ERC).
2. Generate X rising ramp signal.
3. Maintain Ve bias between Scan intervals.

9.1.2 Y Main Board

The Y Main board generates a drive signal by switching the FET and IGBT in synchronization with the logic Main Board timing and sequentially supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

1. Maintain voltage waveforms (including ERC).
2. Generate Y-rising Falling Ramp.
3. Maintain V scan bias.

9.1.3 Logic Main Board

The Logic Main board generates and outputs the address drive output signal and the X,Y drive signal by processing the video signals. This board buffers the address drive output signal and feeds it to the address drive IC (TCP module, video signal- X Y drive signal generation, frame memory circuit / address data re-arrangement).

9.1.4 Logic Buffer (E, F)

The Logic Buffer transmits the data and control signals.

9.1.5 Y Buffer Board

The Y Buffer board supplies the Y-terminal with scan waveforms. The board comprises eight scan driver ICs.

9.1.6 TCP (Tape Carrier Package)

The TCP applies the Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise one data driver IC. Twelve (42") or sixteen (50") TCPs are required for signal scan.

9.2 Abbreviation List

AC	Alternating Current
COF	Circuit On Foil
DC	Direct Current
ERC	Energy Recovery Circuit
ESD	Electro Static Discharge
FET	Field Effect Transistor
FFC	Flat Foil Cable
FPC	Flexible Printed Circuit
FTV	Flat TeleVision
HD	High Definition
I/O	Input/Output
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LB	Logic Buffer
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signalling
PCB	Printed Circuit Board (same as PWB)
PDP	Plasma Display Panel
PSU	Power Supply Unit
PWB	Printed Wiring Board (same as PCB)
RGB	Red, Green, Blue colour space
SD	Standard Definition
SDI	Samsung Display Industry (supplier)
SMPS	Switched Mode Power Supply
SSB	Small Signal Board
SF	Sub Field
TCP	Tape Carrier Package
VR	Variable Resistor
Vsc	Scan Voltage
YBL	Y Buffer Lower board
YBU	Y Buffer Upper board
YM	Y Main board

9.3 IC Data Sheets

Not applicable.

10. Spare Parts List

Please refer to the Philips Service website, for an actual overview (monthly updated).

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- Information on 42 inch HD W2 Plus PDP (S42AX-YD08) added.

Manual xxxx xxx xxxx.2

- Information on 50 inch HD W2 Plus PDP (S50HW-YD07) added.

SDI overview V2.7

Owners: M. Werff / R. Tromp

[illegible]

[illegible]

42SD v4			42SD v5			42HD v3 *not used in EU sets															
9322 226 37682		9322 226 96682		9322 233 81682		9322 215 25682		8204 000 78191													
S42SD-YD07 / PP42SD-015A		S42SD-YD07 / PP42SD-015B		S42SD-YD07 / PP42SD-015F		S42AX-XD02		S42AX-YD01(*)													
9322 233 81682			9322 233 81682																		
Version number used by SDI: PP42SD015B (SMPS Rev. 0.55). Remarks: New SMPS supply: LJ44-00101C + cables. Service information: tbd.		Version number used by SDI: PP42SD015D (SMPS Rev. 0.65) Remarks: New SMPS supply: LJ44-00101C + cables. Service information: tbd.		Version number used by SDI: PP42SD015F (SMPS Rev.0.7).		Boards from PP42SD-015B and PP42SD-015F compatible?		Boards from PP42SD-015B and PP42SD-015F compatible?		Lead type PCB's. Remarks: Lead type boards being phased out.		Codes for lead-free type PCB's.		Are Lead Free boards compatible with leaded boards?		Remark: No supply of new SMPS LJ44-00092A. Compatibility with LJ44-00101C + cable: tbd (15/2).		(SMPS Rev.0.55) E supply: LJ44-00101C Service info			
LJ92-01026A	Y	LJ92-01026A	Y	LJ92-01026A	Y	LJ92-01026A	Y	LJ92-01026A	Y	LJ92-01026A	Y	LJ92-01026A	Y	LJ92-01054A	Y	LJ92-01054A	Y	LJ92-01054A	Y	LJ92-01054A	
LJ92-01027A	Y	LJ92-01027A	Y	LJ92-01027A	Y	LJ92-01027A	Y	LJ92-01027A	Y	LJ92-01027A	Y	LJ92-01027A	Y	LJ92-01055A	Y	LJ92-01055A	Y	LJ92-01055A	Y	LJ92-01055A	
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LJ92-01031A	Y	LJ92-01031A	Y	LJ92-01031A	Y	LJ92-01031A	Y	LJ92-01031A	Y	LJ92-01031A	Y	LJ92-01031A	Y	LJ92-01117A	Y	LJ92-01117A	Y	LJ92-01117A	Y	LJ92-01117A	
LJ92-01032A	Y	LJ92-01032A	Y	LJ92-01032A	Y	LJ92-01032A	Y	LJ92-01032A	Y	LJ92-01032A	Y	LJ92-01032A	Y	LJ92-01118A	Y	LJ92-01118A	Y	LJ92-01118A	Y	LJ92-01118A	
LJ92-01274D	Y	LJ92-01274D	Y	LJ92-01274D	Y	LJ92-01274D	Y	LJ92-01274D	Y	LJ92-01274D	Y	LJ92-01274D	Y	LJ92-01053A	Y	LJ92-01053A	Y	LJ92-01053A	Y	LJ92-01053A	
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LJ92-01336A	Y	LJ92-01336A	Y	LJ92-01336A	Y	LJ92-01336A	Y	LJ92-01336A	Y	LJ92-01336A	Y	LJ92-01336A	Y	LJ92-00980B	Y	LJ92-00980B	Y	LJ92-01115A	Y	LJ92-01115A	
LJ92-01337A	Y	LJ92-01337A	Y	LJ92-01337A	Y	LJ92-01337A	Y	LJ92-01337A	Y	LJ92-01337A	Y	LJ92-01337A	Y	LJ92-00981B	Y	LJ92-00981B	Y	LJ92-01116A	Y	LJ92-01116A	
LJ44-00101A	tbd	LJ44-00101B	N	LJ44-00101C	Y	LJ44-00101D	Y	LJ44-00101E	Y	LJ44-00101F	Y	LJ44-00101G	Y	LJ44-00058A	Y	LJ44-00058A	Y	LJ44-00082A	Y	LJ44-00082A	
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50HD				50HD v3		50HD v4				50HD W1		50HD					
42HD W2		42HD W2P		9322 215 26682		9322 226 54682		9322 226 97682		9322 233 79682		9322 240 25682		9322 245 67682			
S42AX-YD04 / PP42AX-021A		S42AX-YD08 / PP42AX026A		S50HW-XD03 / PP50HW-004C		S50HW-XD04 / PP50HW-005A		S50HW-XD04 / PP50HW-005B		S50HW-XD04 / PP50HW-005E		S50HW-YD01 / PP50HW-010A		S50HW-YD01 / PP50HW-012B			
9322 242 85682 (42HD W1)						9322 233 79682		9322 233 79682				9322 245 67682					
This panel is compatible with the 42HD W1 and 42HD v4 panels for Service. Information is based on: - Application investigation of Philips. - Confirmation of SDI that panels are mechanical compatible. Armin Latz, 07-11-2007.		LJ92-01396A	9965 000 45380	LJ92-01497A	9965 100 10200	Codes for PCBs from 9322 226 54682 PP50H-005A. Remark: New SMPS supply: LJ44-00108C + cables. Service information: tbd.	Codes for PCBs from 9322 226 97682 PP50H-005B and PP50HW-005A compatible?	Codes for PCBs from 9322 233 79682 PP50H-005E and PP50HW-005B compatible?	Remark: The 9322 245 67682 (using PSU 0.2) is fully compatible with the 9322 240 25682 (using PSU 0.3). The PDP module is the same and the only change is the PSU change from rev. 0.3M to rev. 0.2 PSU. Both PSUs are one to one interchangeable without any change in cable. (Tan Siong Tee).		9322 245 67682		S50HW-YD01 / PP50HW-010A		S50HW-YD01 / PP50HW-012B		
		LJ92-01397A	9965 000 45381	LJ92-01498A	9965 100 10201												
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LJ92-01394A	9965 000 45382	LJ92-01495A	9965 100 10202														
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LJ92-01395A	9965 000 45383	LJ92-01502A	9965 100 10203														
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LJ92-01392A	9965 000 45384	LJ92-01493A	9965 100 10204														
LJ92-01393A	9965 000 45385	LJ92-01494A	9965 100 10205														
LJ44-00143A	9965 000 45386	LJ92-01513A	9965 100 10206														
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5W2			63HD		
63HD V4			63HD V4		
9322 257 09682			9322 246 18682		
PP50HW-021B	S50HW-YD07 / PP50HW-028A		S63HW-XD05 / PP63HW-005A		
<p>The S50HW-YD07 (9322 257 09682) is backward compatible with PDP S50HW-YD05 (9322 246 81682). But, PDP S50HW-YD07 have to use the new longer cable CBLE PH 13P/480~480/10+11P FER (3139 171 00041) on pos 8,02 and CBLE KR 7P/480/7P KR WH UL (3104 311 03811) on pos 8M02 due to the new structure of the PSU connector (Tan Siong Tee).</p>					
9965 000 44491	LJ92-01522A	-	LJ92-01193A	9965 000 42586	
9965 000 44492	LJ92-01523A	-	LJ92-01194A	9965 000 42587	
-	-	-	LJ92-01195A	9965 000 42588	
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-	-	-	-	-	
-	-	-	LJ92-01375A	9965 000 42591	
-	-	-	LJ92-01376A	9965 000 42592	
-	LJ92-01524A	-	-	-	
9965 000 44493	-	-	LJ92-01437A	9965 000 42589	
9965 000 44494	-	-	LJ92-01438A	9965 000 42590	
9965 000 44495	LJ92-01402C	-	LJ92-01289C	9965 000 42593	
-	-	-	-	-	
-	-	-	-	-	
9965 000 44496	LJ92-01489A	-	LJ92-01385A	9965 000 42594	
9965 000 44497	LJ92-01490A	-	LJ92-01386A	9965 000 42595	
9965 000 44498	LJ92-01513A	-	LJ44-00123A	9965 000 42596	
-	-	-	LJ44-00124A	9965 000 42597	
-	3809-001912	-	3809-001695	9965 000 42800	
-	3809-001911	-	3809-001546	9965 000 42799	
-	3809-001909	-	-	-	
-	3809-001910	-	-	-	
-	-	-	3809-001743	9965 000 42801	
-	-	-	3809-001742	9965 000 42802	
-	-	-	3809-001745	9965 000 42803	
-	-	-	3809-001744	9965 000 42804	
-	-	-	3809-001741	9965 000 42805	
-	-	-	3809-001768	9965 000 42806	
9965 000 37627	-	-	LJ39-00215A	9965 000 42807	
-	-	-	LJ39-00215A	9965 000 42807	
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-	-	-	LJ39-00234A	9965 000 42808	
-	-	-	LJ39-00184A	9965 000 42809	
-	LJ39-00356A	-	LJ39-00293A	9965 000 42810	
-	LJ39-00353A	-	LJ39-00185A	9965 000 42812	
-	LJ39-00354A	-	LJ39-00239A	9965 000 42811	
Chassis	CTN	Chassis	CTN	Chassis	
EJ3.0U PA			63PF9631D/37	BJ3.0U PA	
LC7.2E PA					
LC7.2E PA					

