RCA

CTC 131/132 Color Chassis Service Education Program

Training Manual

Contents

All integrated circuits and many other semiconductors are electrostatically sensitive and therefore require the special handling techniques described under "Electrostatically Sensitive (ES) Devices" in the Servicing Precautions section of the 1984 CTC 131 or CTC 132 Service Data.

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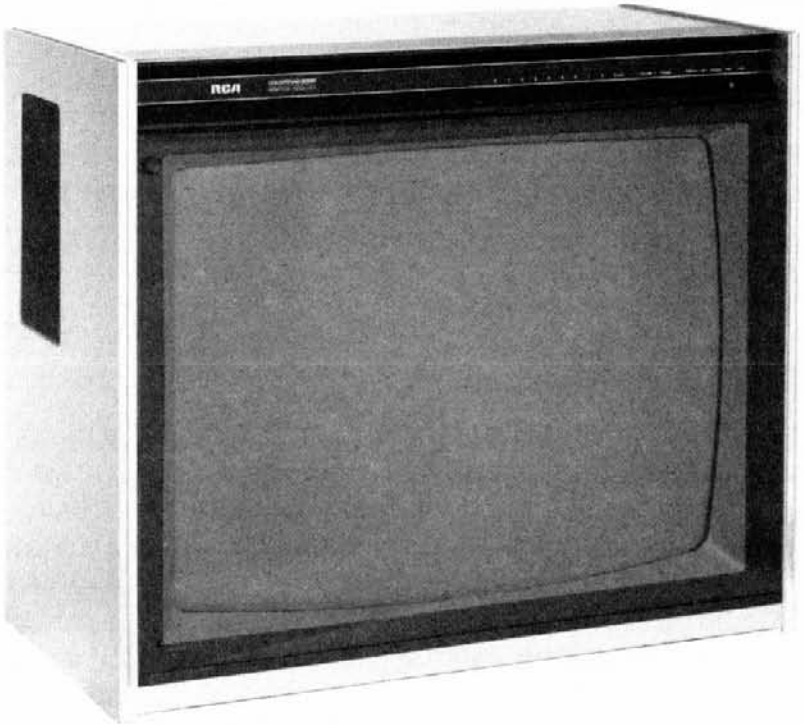
Foreword

This workshop manual is arranged in an operation/servicing sequence and covers those areas of circuit design and servicing which have not been addressed in previous RCA Technical Training Publications. In addition to specific service procedures, block diagrams and simplified schematics are used to illustrate the overall functions. As each major circuit area is introduced, a brief operational discussion precedes the service procedure. An initial understanding of the major operating parameters of the circuit area outlined in this manual prepares the technician for optimum use of the service techniques. In those areas requiring detailed discussion, circuit operation and associated diagrams are separated from the service information.

Product Safety Information

Product safety information is contained in the appropriate RCA Service Data (1984 CTC 131 for Video Monitor and 1984 CTC 132 for Projection Television). All specific product safety requirements and testing shall be complied with prior to returning equipment to the consumer. Servicers who defeat safety features or fail to perform safety checks may be liable for any resulting damages.



FKC 2023 ColorTrak 2000 Monitor-Receiver

Introduction

The CTC 131 and CTC 132 Color Chassis are the newest additions to the RCA unitized chassis family. The CTC 131 chassis appears in all 1985 (K-line) RCA ColorTrak 2000 25-inch "Monitor-Receivers." A variation of the CTC 131 chassis, the CTC 132, is utilized in RCA's Projection Television models.

The ColorTrak 2000 "Monitor-Receivers" incorporate "full spectrum" audio/video performance and either a 6-connection or 29-connection rear "patch" panel for direct hook-up of stereo and video devices. In addition, all ColorTrak 2000 "Monitor-Receivers" come equipped for broadcast stereo and with the Digital Command Center infrared remote (except FKR 2018).

The CTC 131/132 chassis utilize several **new circuits.** Among these are **Chroma/Luminance Wide "I" Processing, Automatic Kine Bias, Broadcast Stereo Audio System** and Dynamic Noise Reduction (DNR® — trademark of National Semiconductor Corp.), **Chopper Power Supply, Video Noise Reduction** and **Video/Audio Switching Circuitry.**

RCA's CTC 131/132 Color Chassis standard features are outlined below:

- 25-inch, 110-degree Deflection COTY-29 Picture Tube (not included in Projection TV)
- Video Noise Reduction
- Automatic Color Balance (Auto-Kine Bias)
- Automatic Peaking
- Wideband Full Resolution Color (Wide "I")
- Automatic Fleshtone Correction
- On-screen Display (Time/Channel)
- FS (Frequency Synthesis) 127-channel Multiband Tuning
- Broadcast Stereo (BTSC System)
- Audio Dynamic Noise Reduction (DNR)
- Video/Stereo Audio 1 and 2 Inputs (6-connection Back Panel)

Additional CTC 131/132 features found in RCA's "Maxi" (top-of-the-line) Monitor-Receivers, including Projection TV models, are:

- Video/Stereo Audio 1 Inputs (Bridged)
- Video/Stereo Audio 2 Inputs
- Video/Stereo Audio 3 Inputs with Digital R/G/B
- Bridged outputs from Video/Audio 1
- Video/Stereo Audio Outputs (Selected Source)
- TV Video/Stereo Audio In/Out
- Stereo Audio-to-Hi-Fi Outputs
- External Speaker Connections
- 29-connection Back Panel

Full-Resolution Color

Due to the unique characteristics of human vision, certain colors are perceived more readily at low light levels. These critical colors center on orange and cyan (blue-green). Less sensitive colors are those centering on magenta and yellow-green. The NTSC color system recognizes this characteristic by transmitting the orange/cyan (or "I") spectrum with a higher resolution than the magenta/yellow-green (or "Q") colors. However, the "I" signal, because of its wide bandwidth, has the potential to intermingle with luminance (detail) information during processing and cause picture detail interference. As a result, conventional color televisions process only a fraction of the available "I" color signal.

FKC 2023 Monitor-Receiver – Back Removed

ColorTrak 2000 Monitor-Receivers (CTC 131/132 chassis), including Projection Television, now include "full resolution" color circuitry to process 100% of the NTSC broadcast signal. These sets process the **entire luminance bandwidth** for full detail performance, the **entire "Q" bandwidth** for those more brilliant colors, **and** the **entire "I" bandwidth** for reproduction of more subtle color detail. RCA's CCD (Charge Coupled Device) comb filter (Detail Processor) virtually eliminates any interference caused by luminance and color intermingling. And the new chroma/luminance integrated circuit solves the complex problem of converting the "I" and "Q" signals into basic red, blue and green colors used to drive the picture tube. More details concerning signal processing are covered later in this manual.

Video Noise Reduction

Associated with full-resolution color is the video noise reduction circuitry, which is designed to minimize snow and graininess in the dark picture areas. Video "noise" (snow or graininess) is most noticeable in the dark areas of the television picture. The new video noise reduction system recognizes this by automatically reducing the degree of peaking for small signal transitions (sharpness) in darker picture areas where noise is most noticeable. At the same time, sufficient peaking is maintained in brighter areas where detail is important, but noise is not as apparent. As an added feature, the video noise reduction system is a **"dynamic" system** which senses and selectively adjusts peaking to match brightness.

Automatic Kine Bias

The emission between the three guns in a picture tube must be optimally balanced in order for correct whites to be produced. Therefore, if tube set-up is improper, a loss of color fidelity occurs, which can cause an overall red, green, or blue tint in extreme cases. With a conventional color television, picture tube set-up tends to drift during the time it takes for the set to fully warm-up (typically, about six minutes). Tube set-up also deteriorates over the years as a television ages.

The new automatic color balance system dynamically senses color imbalance due to picture tube warm-up and automatically maintains true color tracking. A bias circuit actually samples the current from each tube gun sixty times per second. This current is compared to a stable reference, and when errors are detected, they are instantly corrected. Warm-up and aging drift are eliminated along with the low light set-up screen controls).

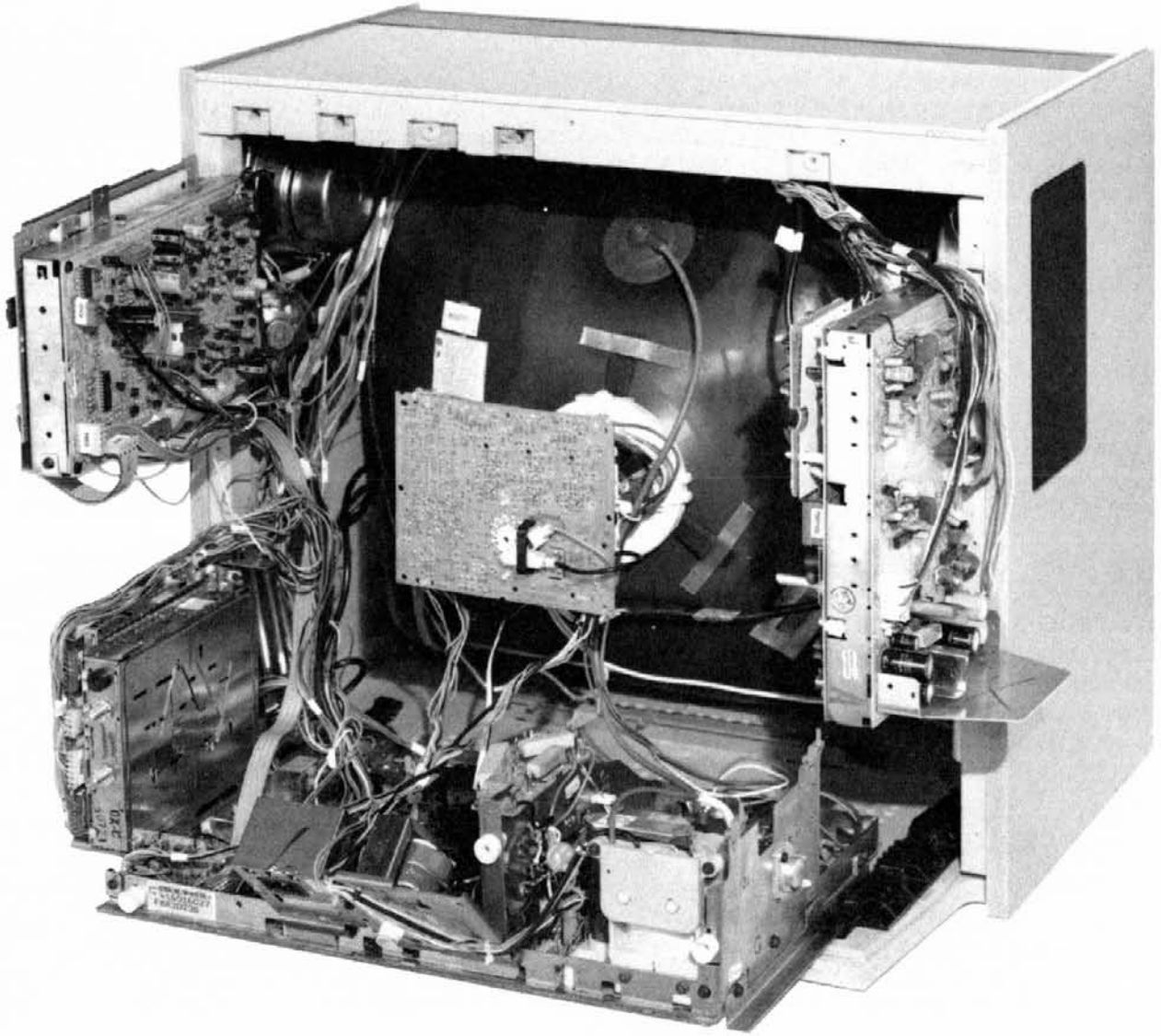
Comb Filter (Detail Processor)

As in previous ColorTrak chassis, the CTC 131/132 series incorporate a charge-coupled device (CCD) comb filter circuit. If you will recall, in a conventional color television, the black and white detail information (luminance) can activate the color circuitry, causing annoying interference patterns. The comb filter virtually eliminates this problem. A CCD comb filter accurately separates color from fine detail portions of the picture to permit individual processing. The result is virtual elimination of edge crawls and "rainbow" effects on complex patterns.

The comb filter also utilizes a vertical peaking circuit to enhance outlines and add more dimension to the picture. Finally, a "noise coring" system works to prevent small picture irregularities from being exaggerated into annoying disturbances. More details concerning signal processing are covered later in this manual.

Broadcast Stereo Audio System

As mentioned previously, all CTC 131/132 chassis are equipped for stereo broadcast reception. Each set provides full performance stereo sound from stereo television broadcasts (where available) with no set modifications or special equipment required. A built-in dbx™ (dbx is a trademark of dbx, inc.) decoding system reduces noise from specially encoded broadcasts. An LED indicator on the set lights during stereo programming, and a stereo/mono selector switch is available to disengage the television's stereo processing circuitry in fringe areas where the stereo signal may not be strong enough for quality reception.



FKC 2023 Monitor-Receiver Chassis and Subassemblies in Full Service Position

Alternate Audio Channel Reception (Audio-B)

ColorTrak 2000 Monitor-Receivers can also receive the alternate audio channel many television stations may transmit for bilingual programming or other applications. A switch on the Monitor (labeled AUDIO B) can be set for automatic selection of the alternate audio channel when such broadcasts are transmitted. Separate LED's signal when Audio B programming is available and when the Audio B switch is set for alternate channel processing. The Digital Command Center also includes an Audio A/B switch, allowing remote activation of the Audio B circuit.

Stereo Sound from External Component/DNR Noise Reduction

ColorTrak 2000 Monitor-Receivers (CTC 131/132 chassis) can provide two-channel sound from stereo video components when a VCR is connected to the set's audio input jacks. The Dynamic Noise Reduction (DNR) system works to automatically reduce background noise and audio hiss on all program sources — off-air or VCR — without affecting the audio. The DNR system is switchable via a front panel control. An LED indicator lights when the circuitry is active.

High-Compliance Speaker System/ Separate Bass and Treble Controls/ Loudness Compensated Volume

High-compliance speakers are an integral part of the audio system in all ColorTrak 2000 (CTC 131/132 chassis) models. These speakers provide excellent reproduction and high efficiency, even at higher-than-average volume levels. Speakers are driven by separate left and right amplifiers for channel separation during stereo programming. Separate bass and treble controls permit TV audio to be tailored to match room acoustics. In addition, when volume is lowered, a built-in loudness contour circuit automatically boosts both bass and treble so that highs and lows are not lost as the sound level decreases.

27-Channel Multiband Quartz Tuning

RCA's familiar "ChanneLock" frequency synthesis system (MST 027 Tuner and MSC 027 Control Modules) utilizes a quartz crystal oscillator (phase lock loop) to generate a frequency reference for all available broadcast and cable channels.

All sets with this feature include access to all 82 VHF/UHF channels or up to 57 cable television channels. A "cable/normal" switch lets the viewer choose between broadcast and cable channel reception. With the switch in the CABLE position and a CATV cable connected to the set's 75-ohm input, any of the following unscrambled cable channels can be tuned:

- 12 regular VHF channels
- 9 midband channels
- 14 superband channels
- 17 hyperband channels

RCA's ChanneLock system also automatically compensates for cable system which use offset techniques up to 2 MHz from standard carrier frequencies.

Digital Command Center Remote Control

The Digital Command Center is a digitally-encoded remote system included with all ColorTrak 2000 (except FKR 2018) and Projection Television models. As with J-line sets, it provides complete control of an entire RCA Video System — Monitor-Receiver and VCR — from a single hand unit. Compatible VCR's include models VJP900, VJT700, VJT500, VKT650, and VKT400.

Pressing the "TV" button turns "on" the Monitor-Receiver and prepares the Command Center to activate any of the following television functions:

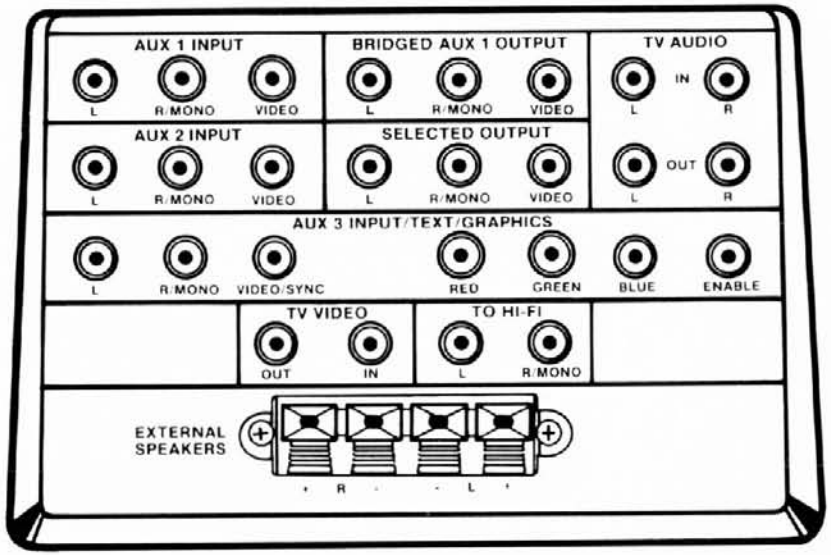
- Direct Channel Access
- Previous Channel Recall
- Video Input Selection
- Volume Up/Down
- Volume Mute
- Channel/Time Display
- Audio B Channel Selection

Clock Set and Channel Scan Memory function are also accessible from the Command Center; controls are located under an auxiliary panel at the top of the unit.

29-Connection ColorTrak 2000
Monitor-Receiver Panel ("Maxi" Monitor)

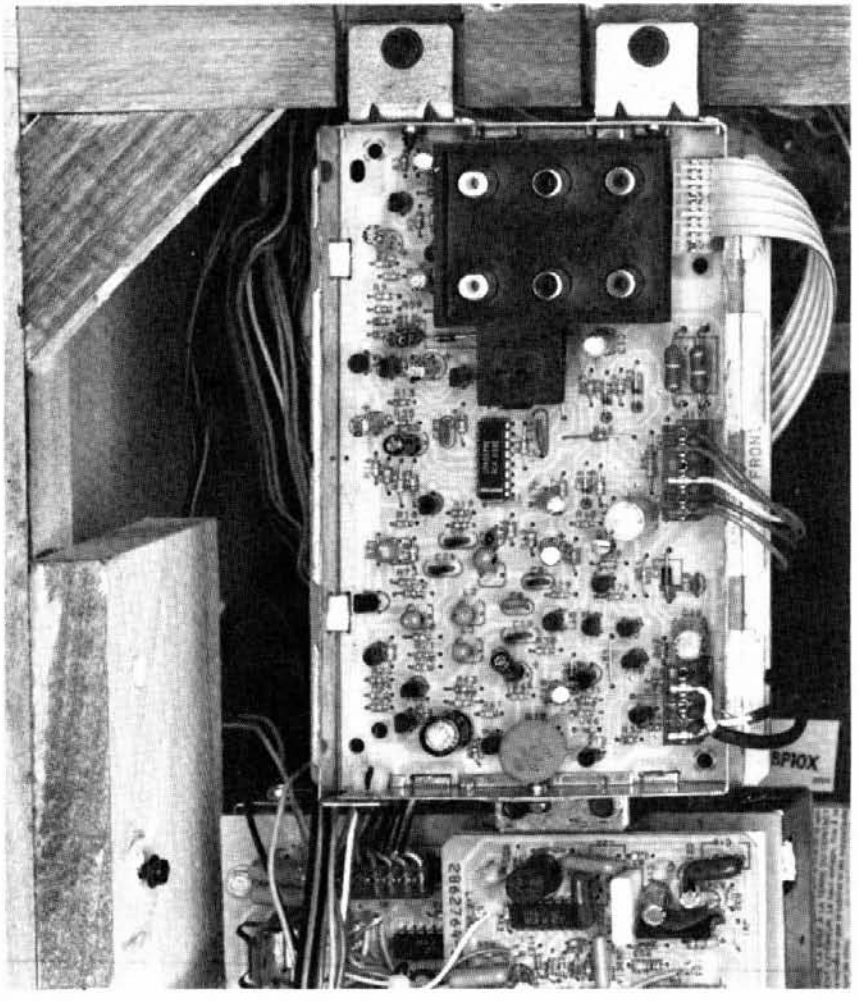
The 29-connection back panel permits direct hook-up of up to three stereo video peripherals (including compatible digital R/G/B device), plus numerous audio/video output applications.

- **Auxiliary 1 Source (Stereo Video/Audio 1 Inputs)** — Allows direct connection of standard NTSC video/audio source — VCR, VideoDisc player, etc. Auxiliary 1 input appears on Monitor when "91" is entered on the Digital Command Center or at the set. Input is bridged so signals can be supplied to the Monitor for display and coupled out to another monitor or VCR.
- **Auxiliary 2 Source (Stereo Video/Audio 2 Inputs)** — Allows direct connection of second video/audio source. Auxiliary 2 input appears on the Monitor when "92" is entered on the Digital Command Center or at the set.
- **Auxiliary 3 Source (Stereo Video/Audio 3 Inputs and R/G/B)** — Provides third video/audio source called to screen by entering "93" at the set or by remote control. Can also accept computer or graphics input from compatible digital R/G/B computer via SYNC-R/G/B-ENABLE jacks. Produces enhanced resolution display up to 80 characters wide.
- **Auxiliary 1 Out (Bridged Out from Video 1)** — Permits direct connection of video device to receive output from Auxiliary 1 source. Can be used for home tape copying, monitor "stringing" etc. Viewer can periodically monitor Auxiliary 1 without disturbing source signal. To prevent image ghosts, signal termination is automatic when jacks are not used.
- **Selected Out (Video/Audio Outputs)** — Delivers video/audio signals from whatever program source is displayed on monitor. Audio output levels are fixed in volume and tone and are suitable for recording.



29–Connection ColorTrak 2000
Maxi Monitor Rear Patch Panel

- **TV Video and TV Audio In/Out** — Provides a potential bypass point in monitor's tuner for insertion of peripheral device, such as video processor. Also useful for simulcasts.
- **Audio-to-Hi-Fi Outputs (Stereo)** — Feed dual audio signals to external stereo amplifier. Output may be broadcast stereo (if available), stereo from video components or monaural. Audio output level is volume controlled by the set to allow remote adjustment of sound level.
- **External Speaker Terminals** — Permit connecting a pair of accessory speakers directly to Monitor to enhance stereo separation.



PWVI Board (Mini Monitor)

Six-Connection ColorTrak 2000 Monitor-Receiver Panel ("Mini" Monitor)

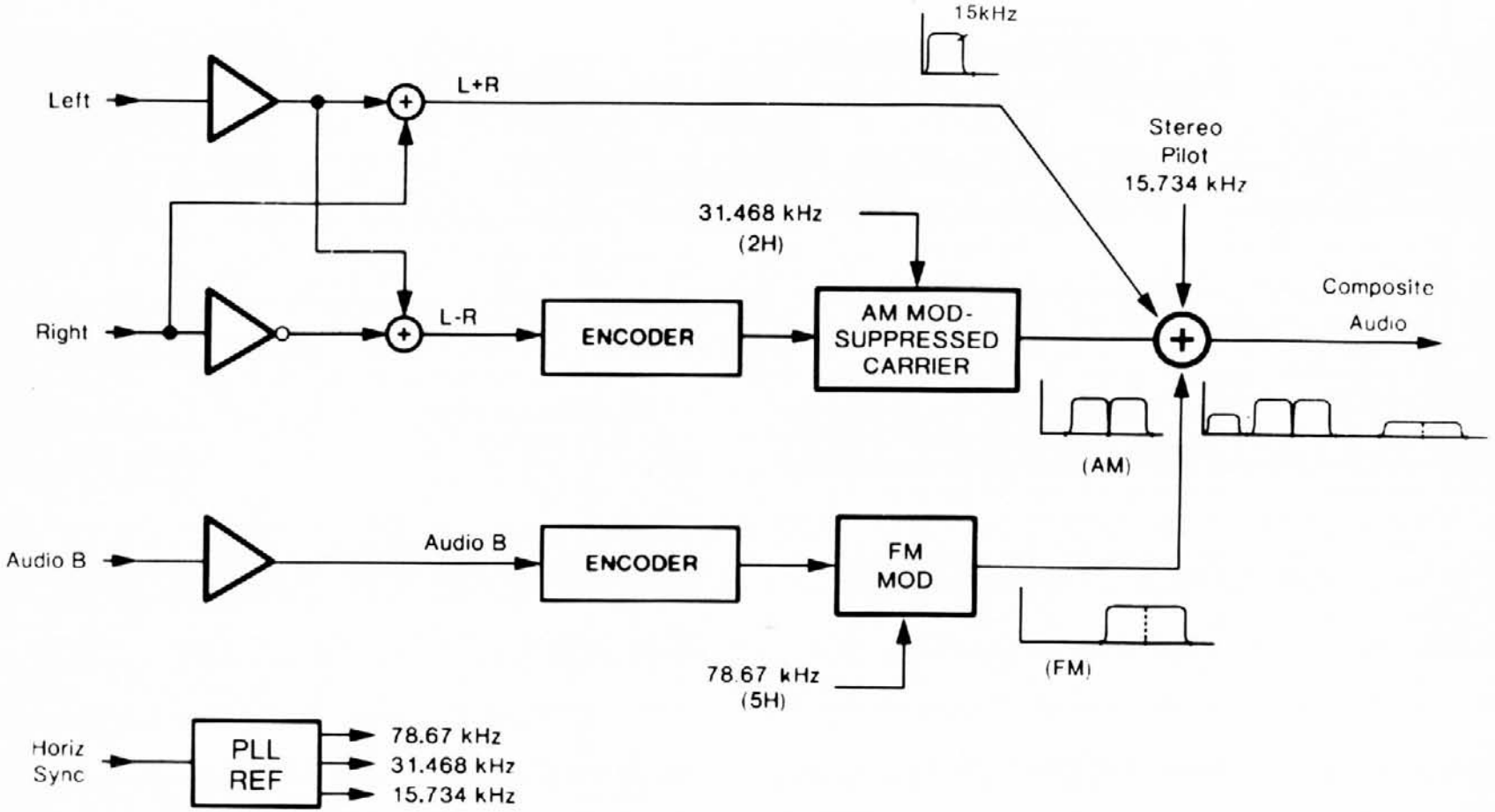
The 6-connection back panel found on standard ColorTrak 2000 Monitor-Receivers permits direct hook-up of up to two stereo video devices. Standard ColorTrak 2000 Monitor-Receivers include direct audio/video inputs for up to two peripheral stereo video components. Auxiliary 1 and 2 inputs can be displayed on the Monitor by entering "91" and "92" respectively at the set or via the Digital Command Center.

Projection Television

As mentioned previously, the CTC 132 color chassis is utilized in RCA's K-line projection television receivers (also referred to as ColorTrak 2000 "Maxi" Monitor-Receivers). All of the features discussed previously for the high-end 25-inch ColorTrak 2000 "Monitor-Receiver" are incorporated into the projection television line. The two models are the PKC500 and PKC600R. In addition, the liquid-cooled tubes/liquid-coupled lenses are carried over from RCA's J-line series.

The CTC 131/132 chassis is 85% "COLD" grounded. The power supply, however, is "HOT" grounded and it is highly recommended that an isolation transformer be utilized during servicing.

PKC 500 Projection Television Receiver

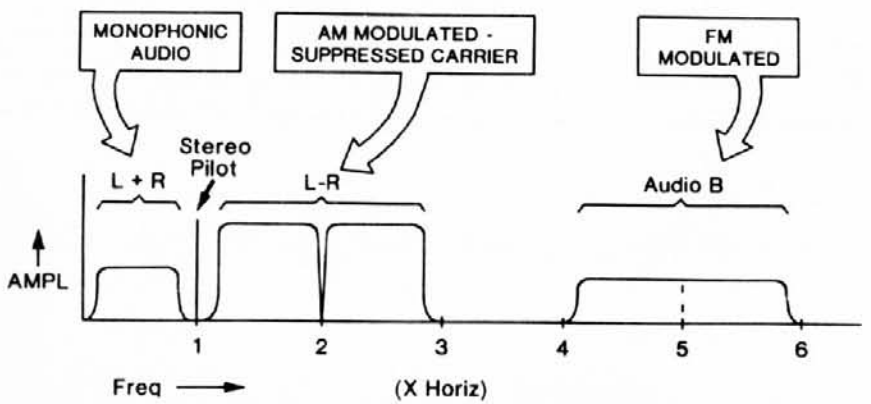


TV Stereo Composite Audio Generation

TV Broadcast Stereo Overview

The CTC 131/132 chassis incorporate the new TV Broadcast Stereo/Audio B multichannel receiver circuitry. With the incorporation of this new stereo receiver circuitry, the television viewer can now enjoy stereo audio off-the-air reception as with stereo audio during playback of prerecorded information from stereo VCR's (on Video Monitor series only). Additionally, the television viewer can select a secondary audio channel (Audio B) that may be transmitted by the station containing bilingual information (another language or possible background music to accompany the video portion of the program).

The stereo/Audio B audio transmission standard is comprised of a wideband **composite audio signal** containing several subcarriers. They are the conventional **monophonic L + R** channel, the **stereo difference** information **L – R** (left minus right audio), and the second audio channel program (Audio B). The stereo subcarrier is twice the horizontal scanning frequency and is AM modulated with suppressed carrier. The second audio program channel is an FM signal centered at 5 times the horizontal frequency. Both the stereo difference channel (L – R) and the second audio channel (Audio B) signal are compressed at the transmitter in accordance with the dbx television noise reduction system. A pilot CW tone signal is transmitted at the horizontal scanning frequency to indicate the presence of stereophonic material.



TV Broadcast Stereo — Composite Audio

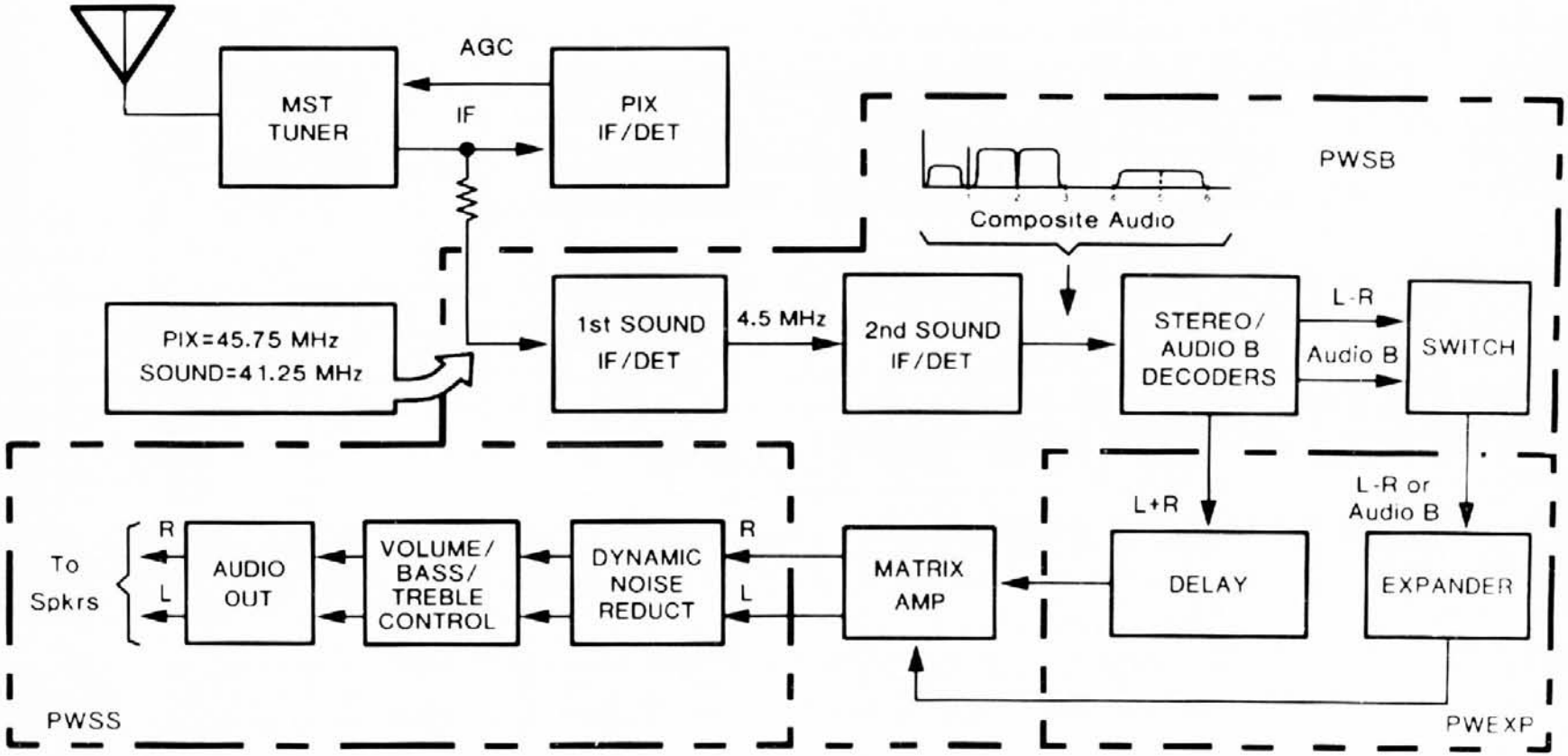
TV Stereo Composite Audio Generation

The simplified block diagram indicates the broadcasting station's generation of the composite audio signal. The left and right audio signals are added together to form the L + R (monophonic) signal. This signal is rolled off at 15 kHz and passed to the input of the adder circuit along with a variety of other signals required to develop the **composite audio signal.** To generate the L – R audio channel, the right channel signal is inverted and added to the noninverted left channel to form the L – R signal. The L – R signal is processed by a dbx encoder circuit to dynamically pre-emphasize the signal characteristics. This encoded audio information is then applied to an AM modulator with suppressed carrier output. The carrier frequency for this modulator is 31.468 kHz (2 times horizontal). The AM modulated signal is applied along with the L + R signal to the output adder circuit and combined with the 15.734-kHz pilot signal and the Audio B information.

The Audio B signal source is amplified and applied to the input of an identical dbx encoder, as discussed previously. The encoded Audio B signal is then applied to the input of an FM modulator circuit whose center frequency is 78.67 kHz (5 times horizontal). This FM modulated signal source is applied to the output adder circuit and combined with the previously developed signals, forming the composite audio signal. The frequency range of the composite audio signal is from a very low audio frequency of 50 Hz to 94.404 kHz (6 times horizontal).

The various carrier frequencies and pilot signal utilized in this composite audio signal are derived from a reference system that is phase locked to video's horizontal sync. This is done in order to minimize problems in the receiver that might cause spurious radiation and beats.

The composite audio signal is then passed to the conventional video/audio modulator similar to the type used in a VCR to generate the RF signal that is transmitted in the air to the receiver. The receiver in turn must tune the proper channel, recover the RF signal, convert it back to baseband audio, individually demodulate the various subcarriers, and switch the appropriate audio source to the audio processing system in the receiver.



Stereo Sound System Block Diagram

TV Stereo Sound System

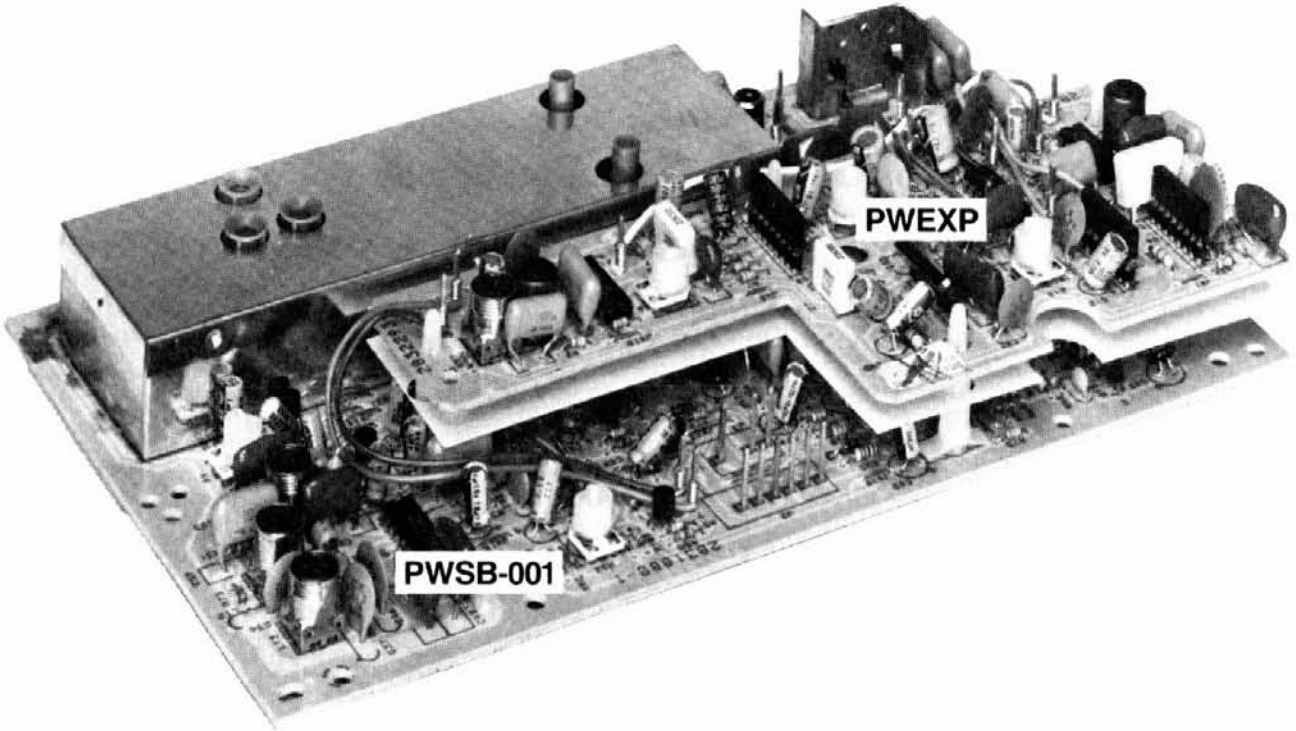
The **complete** sound system for the CTC 131/132 chassis is contained on one separate subassembly, separated from the television chassis. The CTC 131/132 chassis contains **no** audio processing circuitry. The audio processing is contained on a separate assembly that contains three circuit board assemblies. The circuit board assemblies are the PWSB (sound IF, demodulators, and matrix), the PWEXP (dbx expander), and the PWSS (audio volume/tone control, audio output) circuit boards.

Because of the wide baseband audio, the sound IF signal cannot be processed within the same IF circuitry utilized for the pix IF signal, as in conventional television receivers. As a result, the IF signal output from the tuner assembly is divided into **two paths,** the **pix IF circuitry,** and the **new sound IF system.**

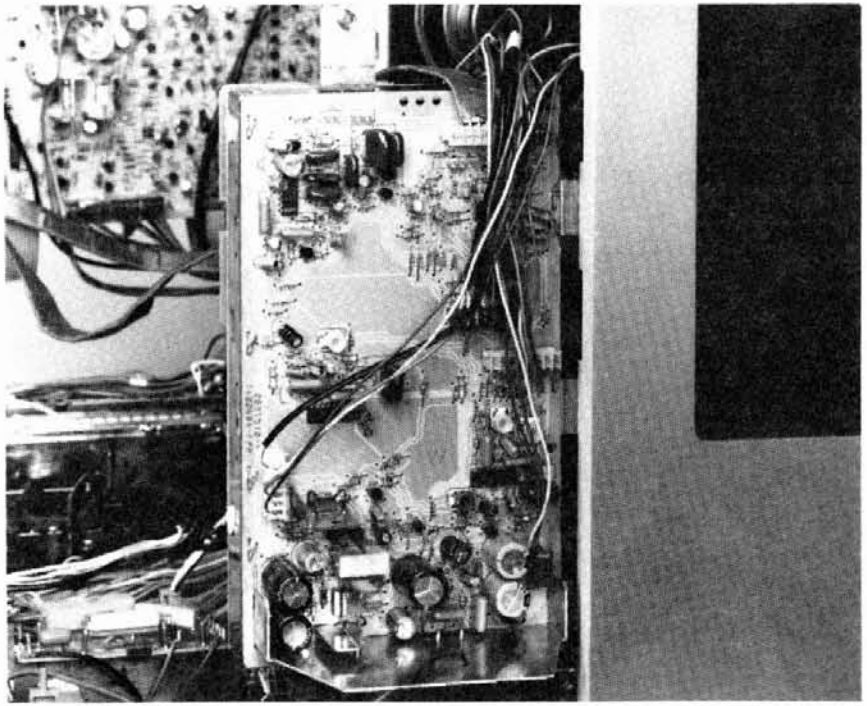
The pix IF output from the tuner assembly routes the signal through the IF link cable to the CTC 131 mother board. Next to the RF jack on the mother board is an additional RF jack that is utilized to route the signal to the audio subassembly in the receiver. The 45-MHz IF signal is input to the first IF amplifier and detector network which operates at the same frequency as the pix IF system (45 MHz). The detector circuitry in the first sound IF stage generates a difference frequency between the pix and the sound carrier developing a 4.5-MHz sound IF signal.

The 4.5-MHz sound signal is then input to the second sound IF amplifier and demodulator circuit, which consists of a wide bandwidth 4.5-MHz IF and demodulator. The 4.5-MHz signal is demodulated, therefore, the recovered audio becomes the baseband composite audio containing the monophonic audio, L – R stereo information, and Audio B signals. The composite audio is then routed to the Stereo/Audio B decoder circuitry which recovers the L – R, the Audio B, and L + R information. The L – R and the Audio B information is input to a switch circuit to select the Audio B signal source or the stereo broadcast information.

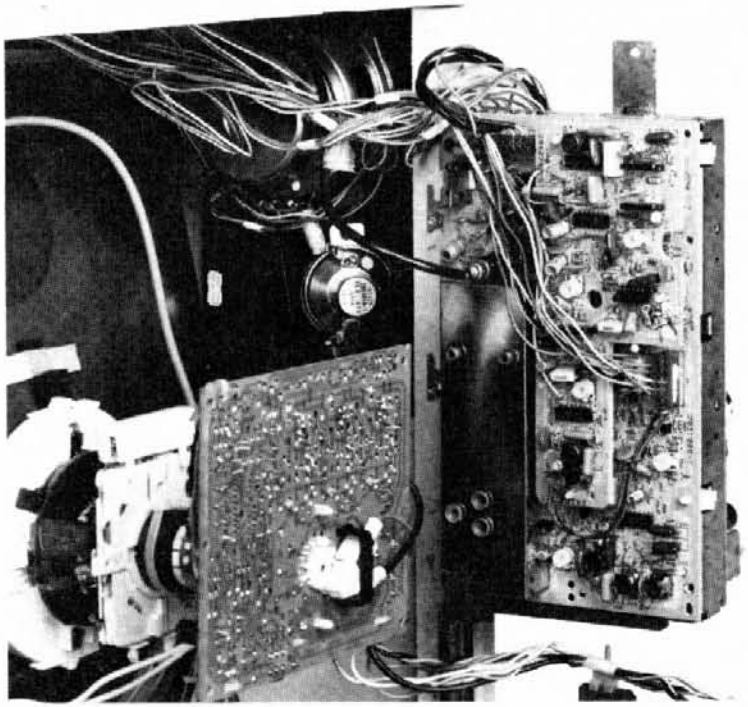
Since the transmitter performs only dbx companding of the L – R and the Audio B signals, the receiver must expand only those two signals and **not** the characteristics of the L + R signal. As a result, the switched audio source of the L – R or Audio B signal is output from the signal switch to the input of the expander circuitry on the expander board. The appropriate signal is then dbx expanded to its normal audio spectrum characteristics. The L + R is also routed to the expander board, passed through an audio delay circuit to maintain the proper phase of these two signals. The delay must precisely match the expander board's circuit delay of the L – R or Audio B signals in order to optimize the channel separation in the stereo mode of operation. The L + R and L – R/Audio B signals are routed back to the PWSB board to the matrix amplifier. The matrixed output signals are then passed to the PWSS board assembly. The signal is input to a dynamic noise reduction (DNR) amplifier, which reduces background noise in the audio during a low amplitude, high frequency condition. The output of the audio system dynamic noise reduction is then passed to the volume/bass/treble control circuitry to characterize the frequency response of the signal per the consumer's preference. The audio is then sent to the audio output circuitry on the PWSS board to drive the internal speakers in the television receiver or external speakers.



PWSB and PWEXP Assembly



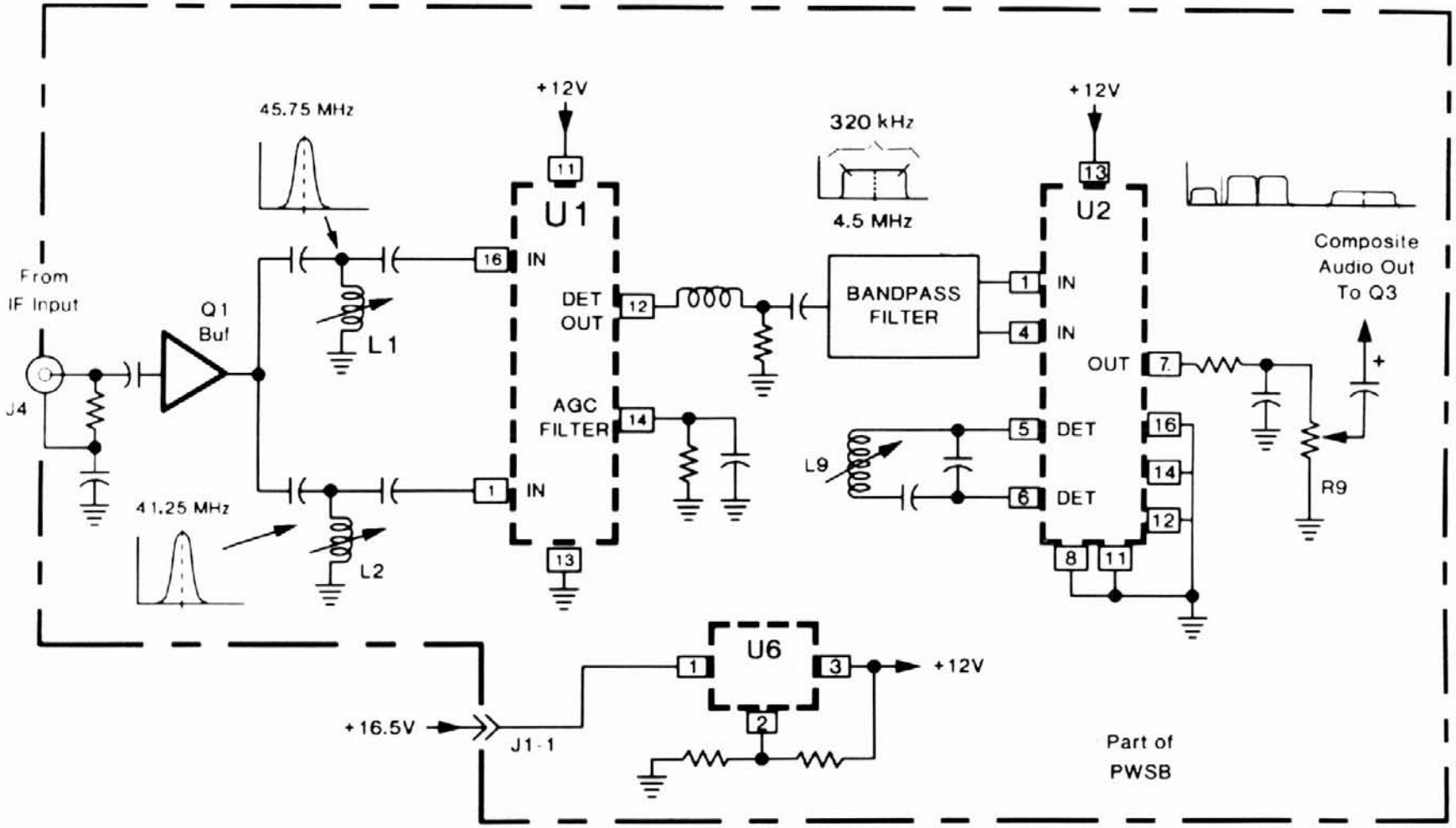
PWSS Audio Process Board Service Position



PWSB and PWEXP Board Service Position (Shield Removed)

Servicing the CTC 131/132 Sound System

Since all the television sound circuitry is contained on a separate subassembly. Servicing sound problems in the CTC 131 does not require pulling the television chassis. Because of the types of signals utilized in the television stereo broadcasting area, field equipment does not allow the technician to easily repair the sound IF/decoder circuitry or expander circuitry. As a result, these two circuit boards (PWSB and PWEXP) are considered a single module and during servicing all that is required is to confirm for the proper inputs and the outputs of the assembly. If the output signals are missing, replace both circuit boards. The expander circuit board along with the PWSB circuit board must be married together and replaced as a pair. Both boards are electrically aligned together after they are married in the factory. Any repairs performed on either board without proper alignment greatly degrades the stereo separation and overall performance. It is recommended that if a defect is found on either the PWSB board or the PWEXP board that the two-board assembly be exchanged under warranty and replaced as a complete unit. The PWSS board contains conventional audio processing circuitry and can be discretely serviced.

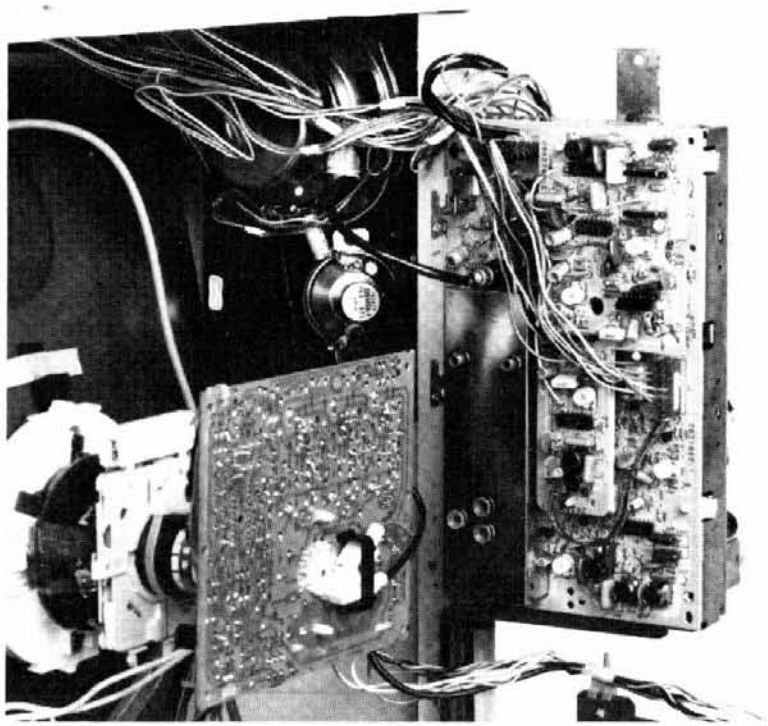


Sound IF Amps and Detectors

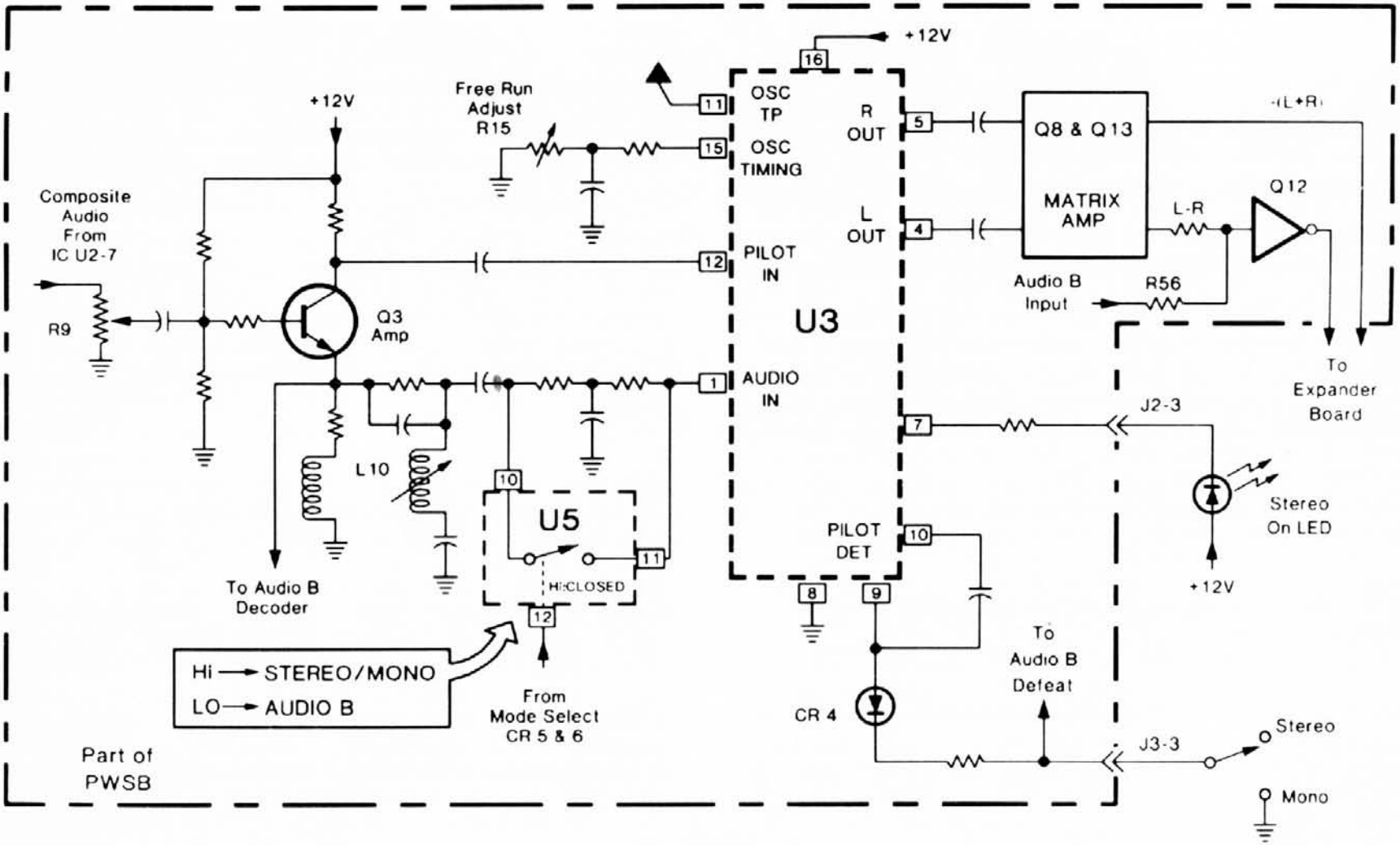
Sound IF Amplifiers and Detectors

With the added bandwidth of the composite audio signal, the sound IF signal must be processed separately from the picture IF signal. As a result, the IF output from the MST tuner module is routed to both the CTC 131 chassis for picture IF processing and the sound system assembly (input of the PWSB board at connector J4). At this point, the IF frequency for the sound carrier is 41.25 MHz and the picture carrier frequency is 45.75 MHz. These two signals are processed in the IF amplifier stages within U1. Inductors L1 and L2 tune the pix and sound carriers respectively. The two signals are internally amplified and detected by U1.

The detection stage is similar to the picture detector in the pix IF circuitry of the television chassis. The detector generates the difference signal between the pix and sound carrier which is 4.5 MHz. This difference frequency (4.5 MHz) is now the second stage sound IF signal, which is passed through a bandpass filter into IC U2. Integrated circuit U2 is identical to previous sound IF amplifier/detector integrated circuits utilized in various RCA color television chassis. The 4.5-MHz sound signal is amplified and demodulated by an internal quadrature detector and the recovered audio from pin 7 of U2 is passed through output level adjustment R9 to transistor Q3 (located on the PWSB board) and to the FM demodulator circuitry. All the circuitry on the PWSB board is powered from a 12-volt source derived from an on-board regulator integrated circuit, U6. The integrated circuit receives its power through pin 1 of connector J1 from the 16.5-volt source delivered by the chopper power supply.



PWSB and PWEXP Board Service Position (Shield Removed)



Stereo Demodulator

Stereo Demodulator

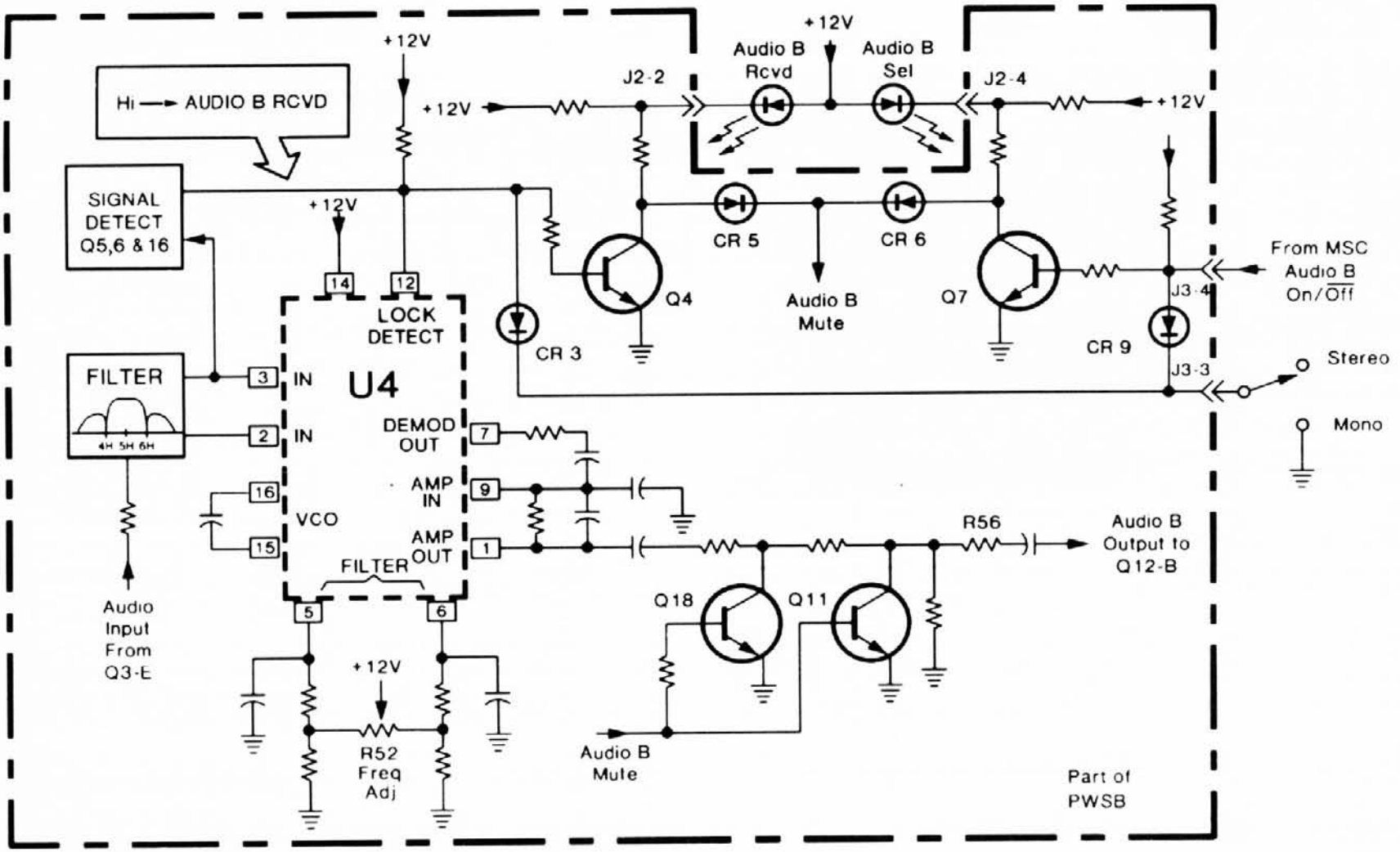
The composite wideband audio output from pin 7 of IC U2 is applied to level control R9. The selected level of audio signal is passed into buffer transistor Q3. The composite audio signal contains **four areas of audio information:** L + R signal, L − R signal, 15,734-Hz pilot signal, and the Audio B signal. In the emitter circuit of Q3 is a series tuned circuit utilizing L10 and C57. This series resonant circuit is adjusted to 15,734 Hz. As a result, the composite audio signal appearing across the trap circuit has the 15,734-Hz pilot signal greatly attenuated. The composite audio signal across the trap circuit is applied to switch integrated circuit U5, pin 10. If the user has placed the Stereo/Mono switch into the STEREO position and Audio B is not active, a logic "Hi" is applied to pin 12 of IC U5. As a result, the internal switch of IC U5 is in a closed position routing the signal out pin 11 to pin 1 of IC U3. If the user places the control panel switch to select the Audio B signal source and Audio B is being received, the logic condition at pin 12 of IC U5 is then logic "Lo," opening the internal switch and forcing the audio through the R/C filter to pin 1. As a result, this network attenuates the signal to pin 1 eliminating the audio signal into pin 1.

The composite audio signal at the emitter of transistor Q3 is also routed to the Audio B detector integrated circuit. The signal is then processed in the Audio B mode of operation to supply the audio signal to the output amplifiers. The Audio B processing is discussed later in this publication. In the Stereo mode of operation, with the achievement of the composite audio signal being applied to pin 1 of IC U3, the action of the trap circuit in the emitter of Q3 reduces the impedance in the emitter circuit, allowing Q3 to have a large amount of gain at the signal frequency of 15,734 Hz.

The amplified pilot signal is applied to pin 12 of IC U3. The composite audio signal's L − R signal (input at U3, pin 1) is an AM modulated signal with a suppressed carrier. The suppressed carrier is 2 times the horizontal frequency. Internal to IC U3 is a phase lock loop (PLL) system that is phase locked in frequency to the pilot input signal at pin 12. The PLL system inside U3 then generates the required 2 times horizontal carrier signal in order to detect this L − R signal.

The frequency of the voltage controlled oscillator within IC U3 is determined by the R/C time constant connected to pin 15. During alignment, with no signal input to IC U3, the freerun adjust control (R15) is adjusted while monitoring the signal at pin 11 of IC U3. With no input signal, this frequency should be 15,734 Hz. After the stereo demodulator integrated circuit detects and recovers the L − R signal, the L − R and L + R signals are combined or matrixed internally to generate the right and left output signals at pins 5 and 4 respectively. Because the transmitter has dbx companded the L − R signal, the outputs at pins 4 and 5 of IC U3 cannot be directly utilized by the audio output system. The right and left channel output signals from pins 4 and 5 are coupled into a matrix circuit consisting of transistors Q8 and Q13 regenerating the L − R and L + R signals. The L + R signal from the matrix amplifier has been inverted. For reference purposes, it is referred to as the −(L + R). The L − R signal from the matrix amplifier is applied to the input of transistor Q12 along with the Audio B input signal from the Audio B detector circuitry. Dependent upon the mode of operation, only one of these two signals is present at the input of Q12. The selected signal is then amplified and output at the collector of Q12 and along with the −(L + R) signal is applied to the expander circuit board assembly.

When IC U3 detects the pilot signal input and determines that the internal phase lock loop is properly locked to the pilot signal, the integrated circuit outputs a logic "Lo" at pin 7 turning "on" the front panel stereo LED indicator. In the event of weak signal conditions, the user may wish to process the audio signal as a monophonic signal by placing the Stereo/Mono switch in the MONO position, grounding connector J3, pin 3. This pulls the Audio B defeat circuitry "Lo" and also pulls pin 9 of IC U3 "Lo" forcing IC U3 to W turn "off" the internal phase lock loop system and process only the L + R input signal. The monophonic audio is output at pins 4 and 5 and applied to the matrix amplifier, Q8 and Q13, which generates the monophonic audio at the −(L + R) output **only.** The L − R output contains no signal because the L and R signals cancel each other. The selected audio is then routed to the expander board for dbx expansion.



Audio B Demodulator

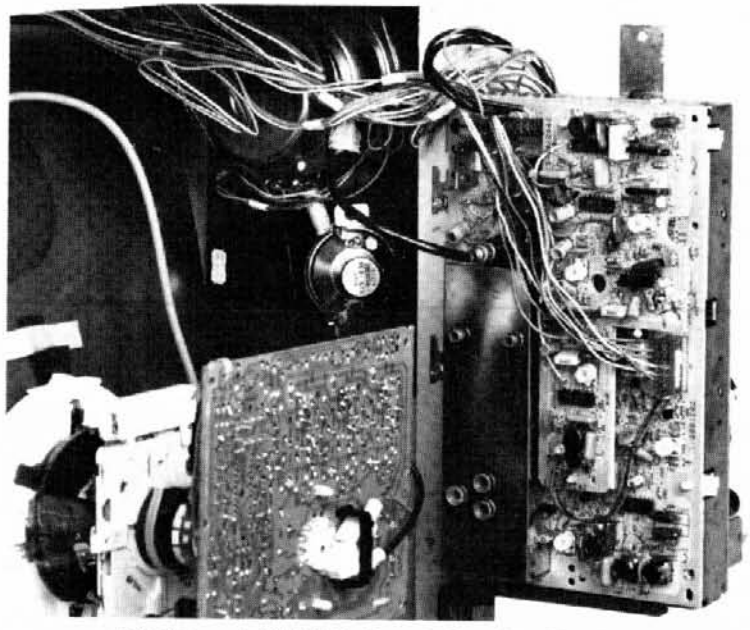
Audio B Demodulator

The composite audio signal from the emitter of transistor Q3 is applied through an L/C filter to input pins 2 and 3 of IC U4. The filter circuit passes only the Audio B signal which occurs at the high end of the composite audio band, (4H to 6H). Within the filter circuit are two traps that attenuate signals at 4 times and 6 times horizontal minimizing the possibility of harmonic signal interference from the deflection and video circuitry. The signal input to pin 3 of IC U4 is also routed to signal detect circuitry consisting of Q5, Q6, and Q16. The signal detect circuitry determines if the Audio B signal is present. If so, it generates a logic "Hi" signal which is output to pin 12 of IC U4 and to the base of transistor Q4.

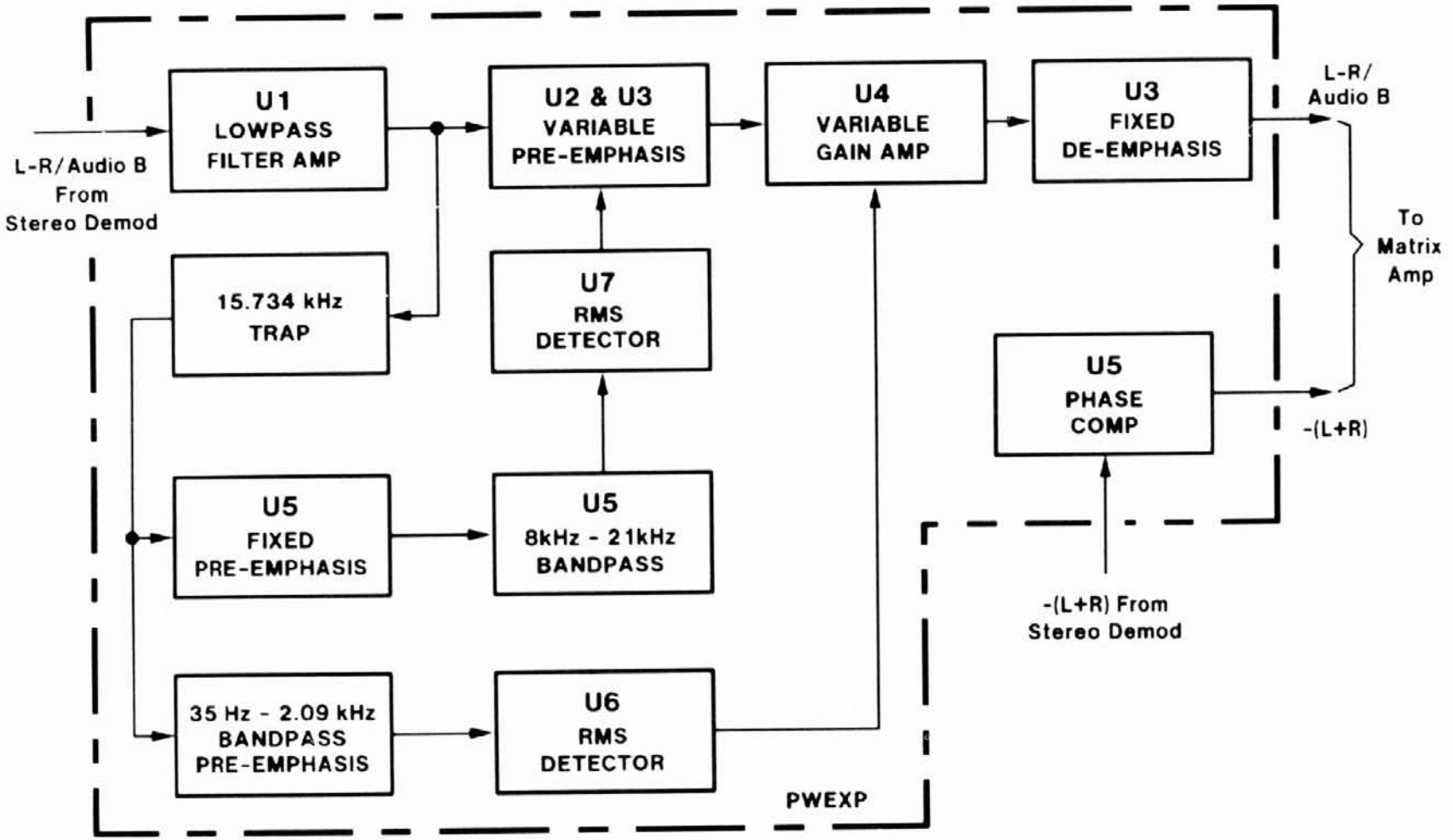
The composite audio signal containing the Audio B information that is input to IC U4 is demodulated by the internal FM demodulator system. The frequency of the internal oscillator is determined by the capacitor connected between pins 15 and 16 of IC U4 and the correction voltage determined by the frequency adjust control, R52, connected in the loop filter circuitry between pins 5 and 6 of IC U4. With the presence of an Audio B signal, IC U4 demodulates the FM modulated Audio B signal generating an output audio signal at pin 7. The audio output signal is then passed to input pin 9 of IC U4, an internal audio amplifier. The output of this amplifier at pin 11 is then routed through an R/C coupling network through R56 and then capacitively coupled to the base of transistor Q12. The output signal is grounded during Audio B mute operation by transistors Q11 and Q18. The Audio B mute signal is logic "Hi" during the period when stereo or mono is received.

During Audio B operation, the Audio B mute signal is logic "Lo" keeping Q11 and Q18 turned "off." The Audio B mute signal is developed from transistors Q4 and Q7. Transistor Q4 is turned "on" when the output of the signal detect circuit at Q5, Q6, and Q16 develops a logic "Hi." The logic "Hi" turns transistor Q4 "on" pulling both the collector and the cathode of the Audio B received LED (J2 pin 3) "Lo," turning "on" the LED. When the signal detect circuitry does not detect an Audio B signal, a logic "Lo" is applied to the base of Q4 turning "off" the transistor, placing the collector at logic "Hi," thus turning "off" the Audio B received LED. The base of transistor Q4 can also be pulled "Lo" by the activation of the Stereo/Mono switch. With the Stereo/Mono switch placed in the MONO position, a logic "Lo" is applied to pin 3 of connector J3 pulling the cathode of CR 3 logic "Lo." This forces the Audio B demodulator IC U4 into the inoperative state and also applies a logic "Lo" to transistor Q4 to turn "off" the Audio B received LED. During the period when the Audio B circuitry is inactive, the collector of transistor Q4 being logic "Hi" applies the logic "Hi" signal through diode CR 5 to the Audio B mute line. The Audio B mute line turns "on" transistors Q11 and Q18, grounding the Audio B output line.

The Audio B signal circuitry can be selected by an on-panel Audio B switch or also by the Audio B signal source switch on the Digital Command Center. Because of the remote access to this function, the signal from the front panel switch is first routed to the tuner control module (MSC) as well as the remote control signal. The Audio B "on/off" signal is routed to connector J3, pin 4, and applied to the base of transistor Q7. When the user selects the Audio B mode of operation, a logic "Hi" is applied to the base of Q7 pulling the collector "Lo." This turns "on" the **Audio B set** LED, which is connected at connector J2, pin 4. If the user selects the Audio B signal source or places the Stereo/Mono switch in the MONO position, a logic "Lo" is applied to the base of transistor Q7 allowing the collector to go "Hi." The logic "Hi" at the collector of Q7 turns "off" the **Audio B set** LED and also passes the logic "Hi" through diode CR 6 to the Audio B mute line to turn "off" the audio output from IC U4, pin 11.



PWSB and PWEXP Board Service Position (Shield Removed)

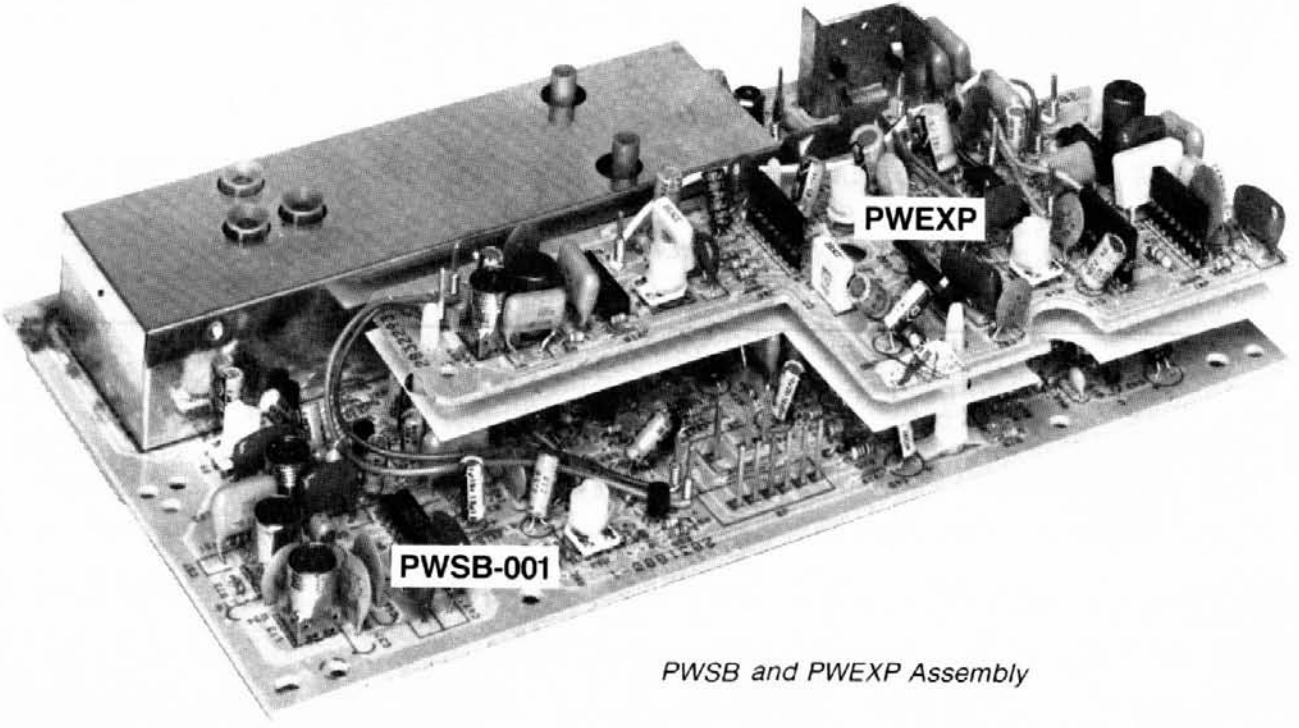


Expander Board (dbx Noise Reduction)

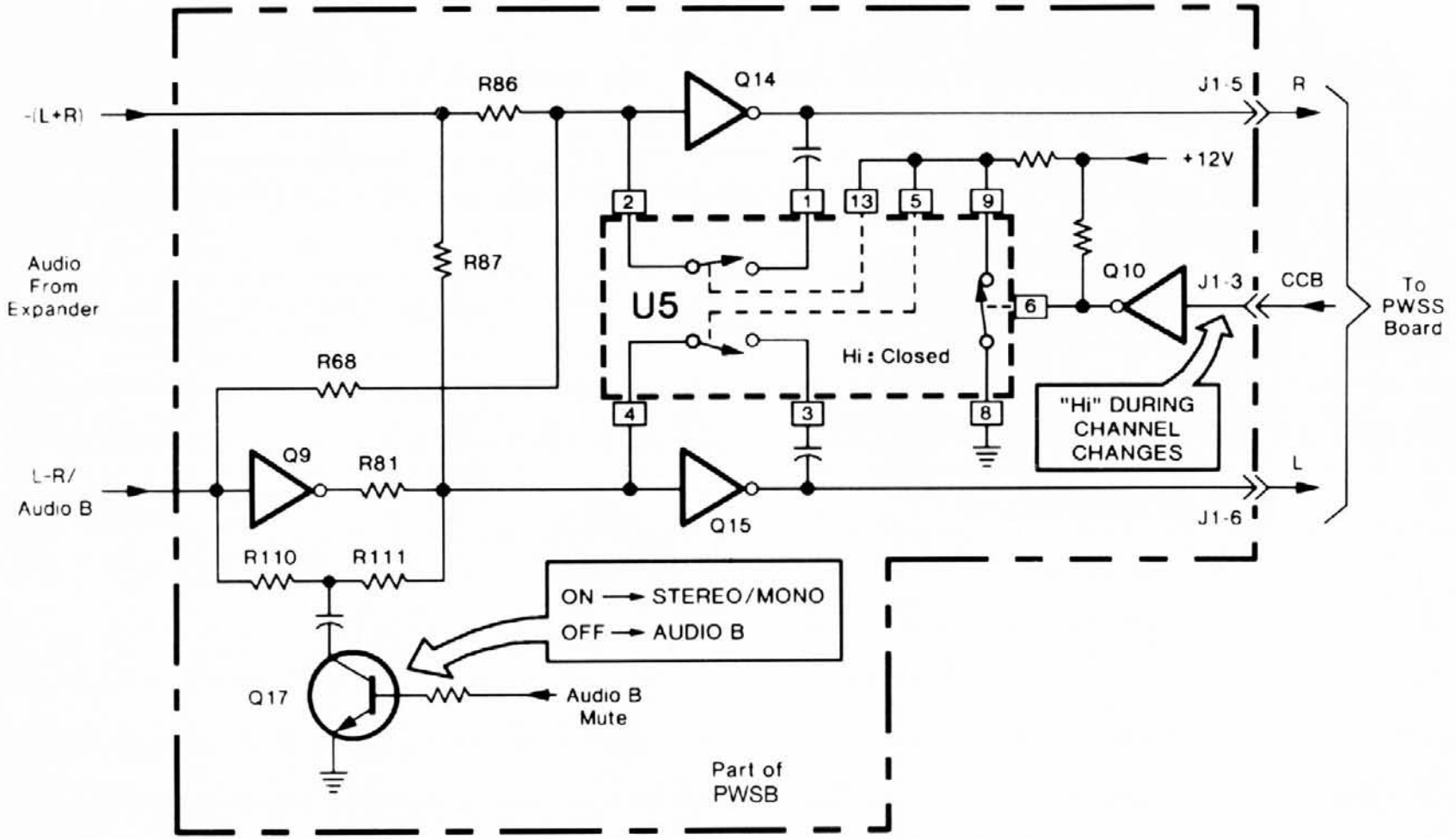
Expander Board (dbx Noise Reduction System)

The demodulated audio signal, −(L + R), L − R, or Audio B signal, is routed from the PWSB board to the expander circuit board. Contained on the expander circuit board are seven integrated circuits that process the L − R or Audio B signals in the dbx noise reduction process. Since the station transmitter compands only the L − R and Audio B signals, the expander board must also process and expand the selected L − R or Audio B signal. The dbx noise reduction system is a registered process for noise reduction encoding and decoding optimizing the signal-to-noise of the audio information.

The expander board processes the audio input signal from the L − R Audio B source through lowpass filter IC U1. The output of IC U1 is passed through a 15,734-Hz trap and applied to the input of U5, a fixed pre-emphasis amplifier, and also to a bandpass network with a bandwidth of 35 Hz to 2.09 kHz. The output of U5 (fixed network) is applied to an 8-kHz to 21-kHz bandpass circuit whose output is applied to U7, an RMS (root-mean-square) detector. The RMS detector output is applied to the control input of a variable pre-emphasis circuit consisting of IC's U2 and U3. In essence, the purpose of IC's U2 and U3 is to vary their gain characteristics as per the frequency of the signal content contained within the 8-kHz to 21-kHz band. The audio component within the 35-Hz to 2.09-kHz band is output to RMS detector IC U6. The output of U6 is applied to the control input of IC U4, a variable gain amplifier. As a result, the gain of IC U4 is controlled by the component of the audio signal within the 35-Hz to 2.09-kHz region. The resultant audio signal is then applied to U3, the fixed de-emphasis amplifier, and output at the L − R or Audio B output line, which is then coupled back to the PWSB board. The −(L + R) signal is passed through the expander board through IC U5. The signal processing performed by U5 delays the audio signal to match the delay of the L − R or Audio B signal processed by the expander board. This delay must be matched in order to achieve the **optimum separation** in the Stereo mode of operation. These two signals, −(L + R) and L − R/Audio B, are then reapplied back to the PWSB board to the matrix amplifier circuitry.



PWSB and PWEXP Assembly



Stereo Matrix Amplifier

Stereo Matrix Amplifier

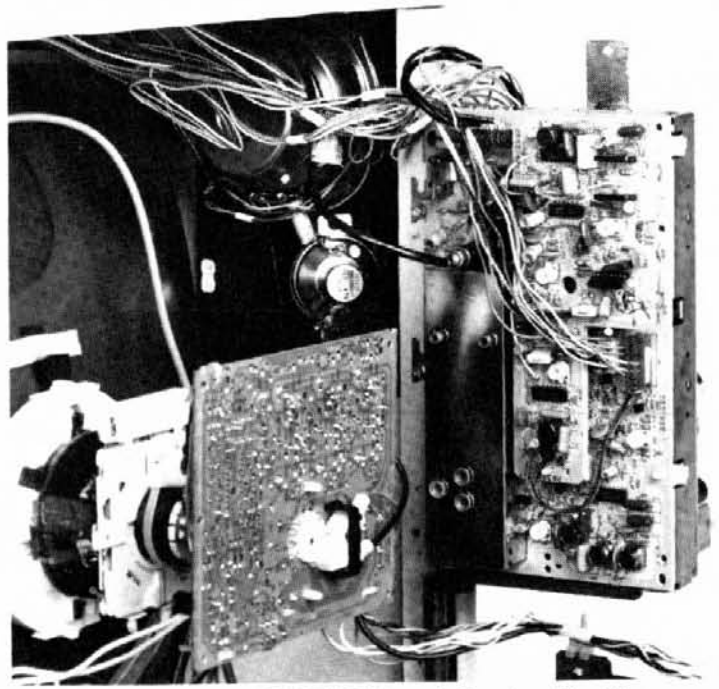
The recovered audio from the PWEXP circuit board is input to the stereo matrix circuitry. The stereo matrix amplifier operates in **three modes of operation — Monophonic, Stereo, or Audio B.**

In the Monophonic mode of operation, the −(L + R) audio signal input is the only signal appearing at the input of the matrix circuit. This signal is coupled through R86 into the base of transistor Q14 and through R87 to the base of Q15. In Mono operation, no signal is present at the L − R/ Audio B input. Transistors Q14 and Q15 amplify and invert the −(L + R) signal generating the L + R signal (mono signal) output at connector J1, pins 5 and 6, which is routed to the PWSS board for volume and tone control processing and output amplification to the speakers.

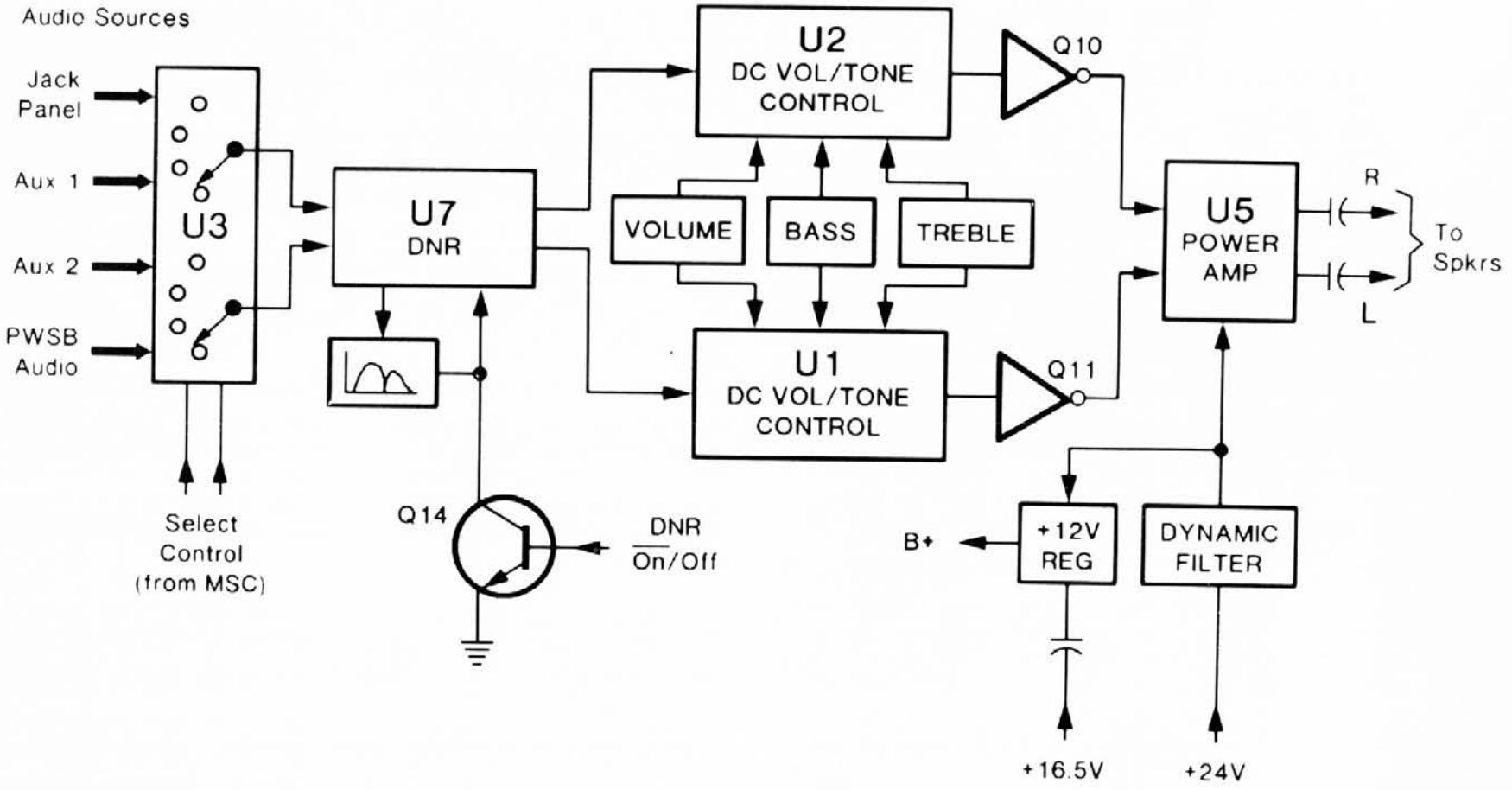
To minimize audio noises during channel change operations, IC U5 — a solid state switch integrated circuit — is connected through capacitors across transistors Q14 and Q15. When the tuner system changes from one channel to another, a channel change blanking (CCB) signal is applied through connector J1, pin 3, to the base of transistor Q10. The signal is logic "Hi" during the time the tuning system is changing channels. This logic "Hi" is inverted by Q10 and applied to pin 6 of IC U5. The logic "Lo" input at pin 6 causes the internal switch between pins 8 and 9 to open. With the switch between pins 8 and 9 open, the voltage at pin 9 is pulled logic "Hi" which is applied to pins 5 and 13 of IC U5. The logic "Hi" at pins 5 and 13 place two internal switches within IC U5 in the closed position. These two switches capacitively couple the output signal of both Q14 and Q15 to the respective inputs reducing the gain of the amplifiers. As a result, the audio output from this matrix amplifier is quite small during channel change operations and returns to normal gain status when channel change has been completed.

In the Audio B mode of operation, the signal at the −(L + R) input is **zero** and the state of transistor Q17 is "off." The L − R or Audio B signal is input to R68 into the input of transistor Q14. With Q17 "off," the Audio B input signal is input to Q9 and R110. The gain of Q9 is less than "1" with the signal inverted. The inverted output from Q9 develops a current through R81 to the input of Q15. The Audio B signal at R110 also develops a noninverted signal current through R110 and R111 (Q17 is "off") to the input of Q15, but twice the amplitude as the current through R81. As a result, the input current to the input of Q15 is the same phase and amplitude as the current through R68 to Q14. The Audio B signal is then amplified by Q14 and Q15 and output to connectors J1, pins 5 and 6, which is then routed to the PWSS board audio output amplifiers.

In the Stereo mode of operation, Q17 is turned "on" resulting in an AC ground at the junction of R110 and R111 preventing the noninverted signal from getting around transistor Q9. The L − R signal is inverted and amplified by Q9, generating a −(L − R) component which is applied through R81 to the base of Q15. Also applied to the base of Q15 is a −(L + R) component. In this instance, the R components cancel and the L components add together generating a left channel output (Q15 at connector J1, pin 6). The −(L + R) is routed through R86 to the input of Q14. The L − R signal is routed through R68 to the base of transistor Q14. The L components cancel, the − R components add together generating a − R component. This component is amplified and inverted by Q14, which then outputs the right channel output signal.



PWSB and PWEXP Board Service Position (Shield Removed)



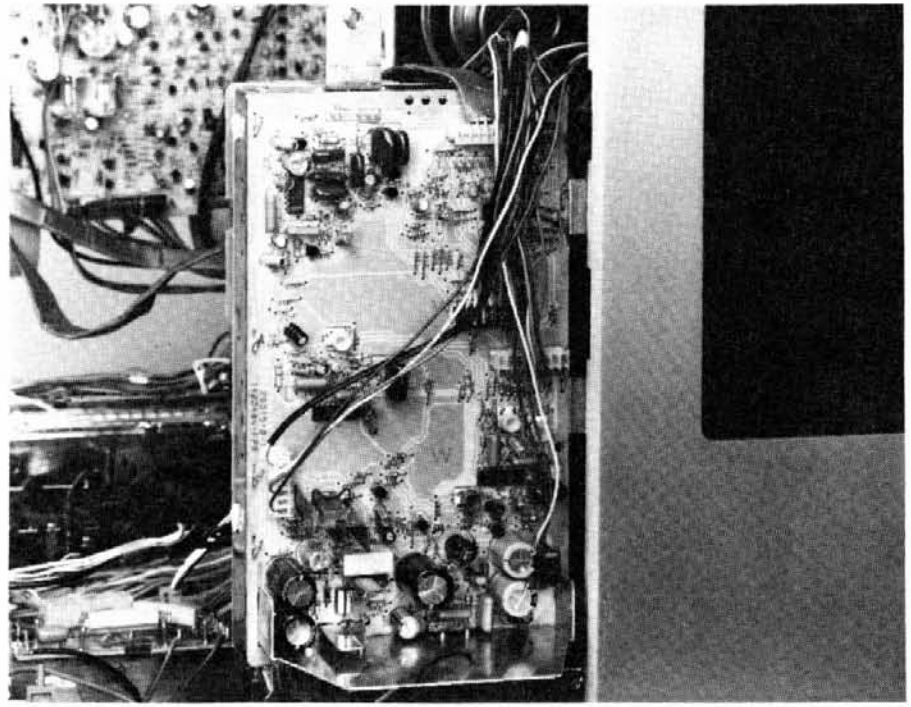
PWSS Board Block Diagram

The PWSS Board

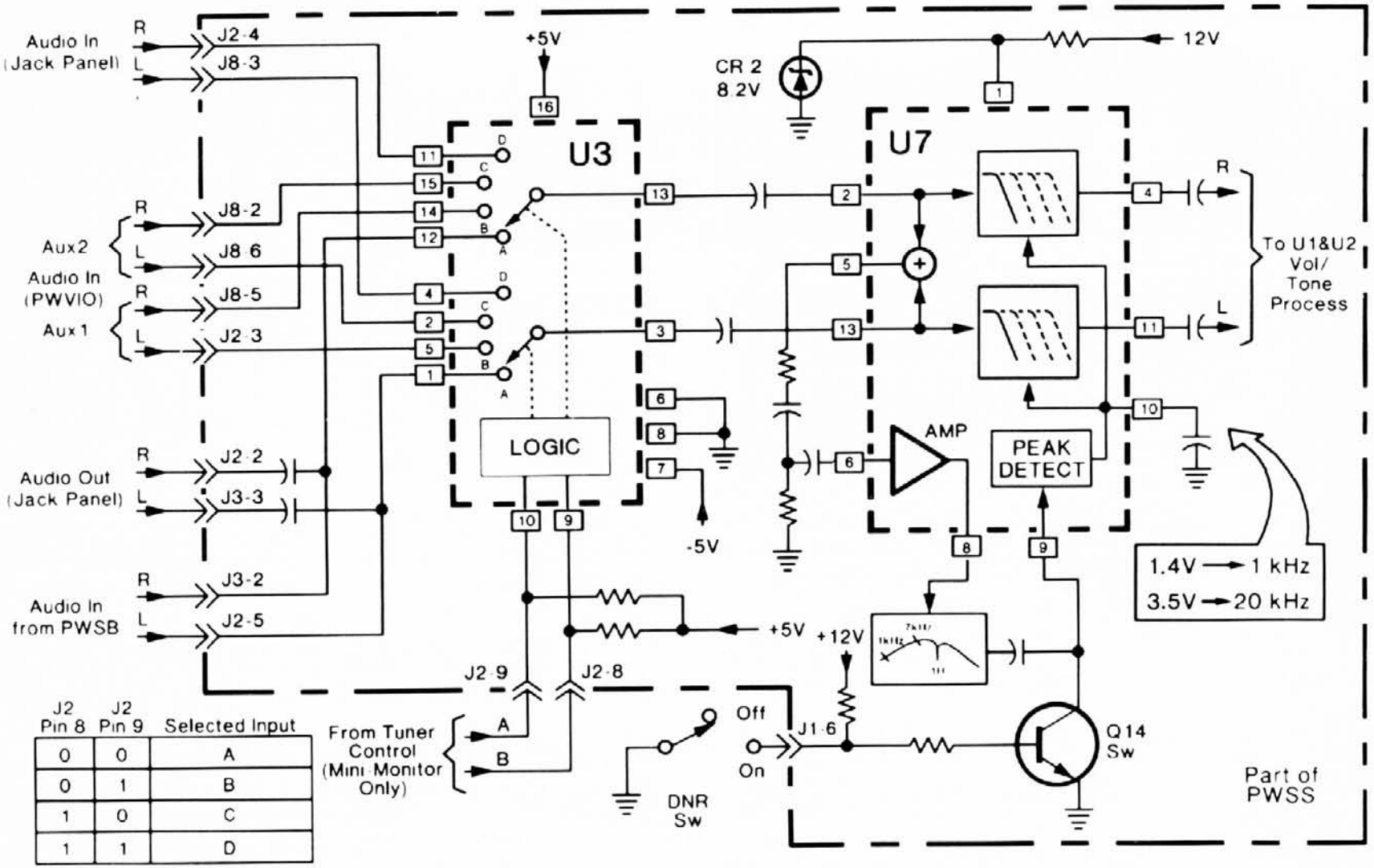
The PWSS circuit board assembly contains multiple circuit operations to select and process the audio signal and apply the output to the internal or external speakers of the television receiver. The audio select function is contained within IC U3 which can select one of four possible audio sources. The right and left channel selected audio is then processed by the dynamic noise reduction (DNR) IC U7. However, the dynamic noise reduction circuit can be disabled by turning "on" transistor Q14.

The processed audio from the DNR circuit is applied to DC control/tone control process integrated circuits U1 and U2. The processed audio signals are then passed through buffer transistors Q10 and Q11 to the input of the power amp IC U5. The output from U5 is passed through to the front panel speaker "on/off" switch and then to the internal or external speaker connections.

B+ power for the PWSS board is derived from the +24-volt and +16.5-volt chopper power supply outputs. A dynamic filter circuit (consisting of transistors Q1 and Q12) performs a B+ filtering action and also determines the speed at which the B+ comes up at turn "on" for the output amplifier integrated circuit and circuitry on the PWSS board. The output of the dynamic filter is also passed to the 12-volt regulator circuit (consisting of Q8 and Q18) which has a slow-down network allowing the B+ to raise slowly when power is first applied to prevent annoying audio noises and pops at turn "on."



PWSS Audio Process Board Service Position



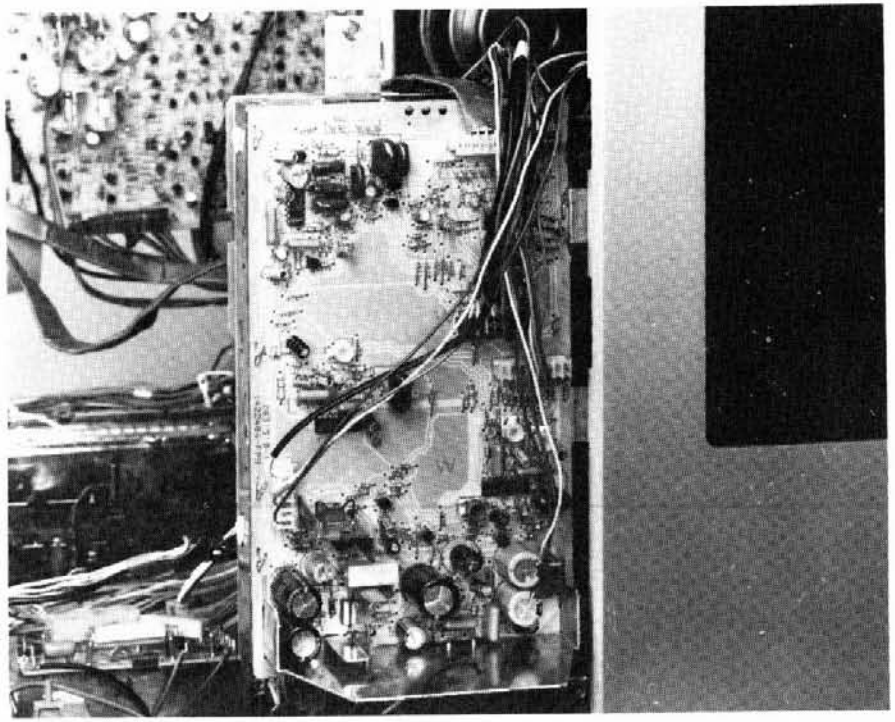
J2 Pin 8	J2 Pin 9	Selected Input
0	0	A
0	1	B
1	0	C
1	1	D

Audio Select/DNR Operation

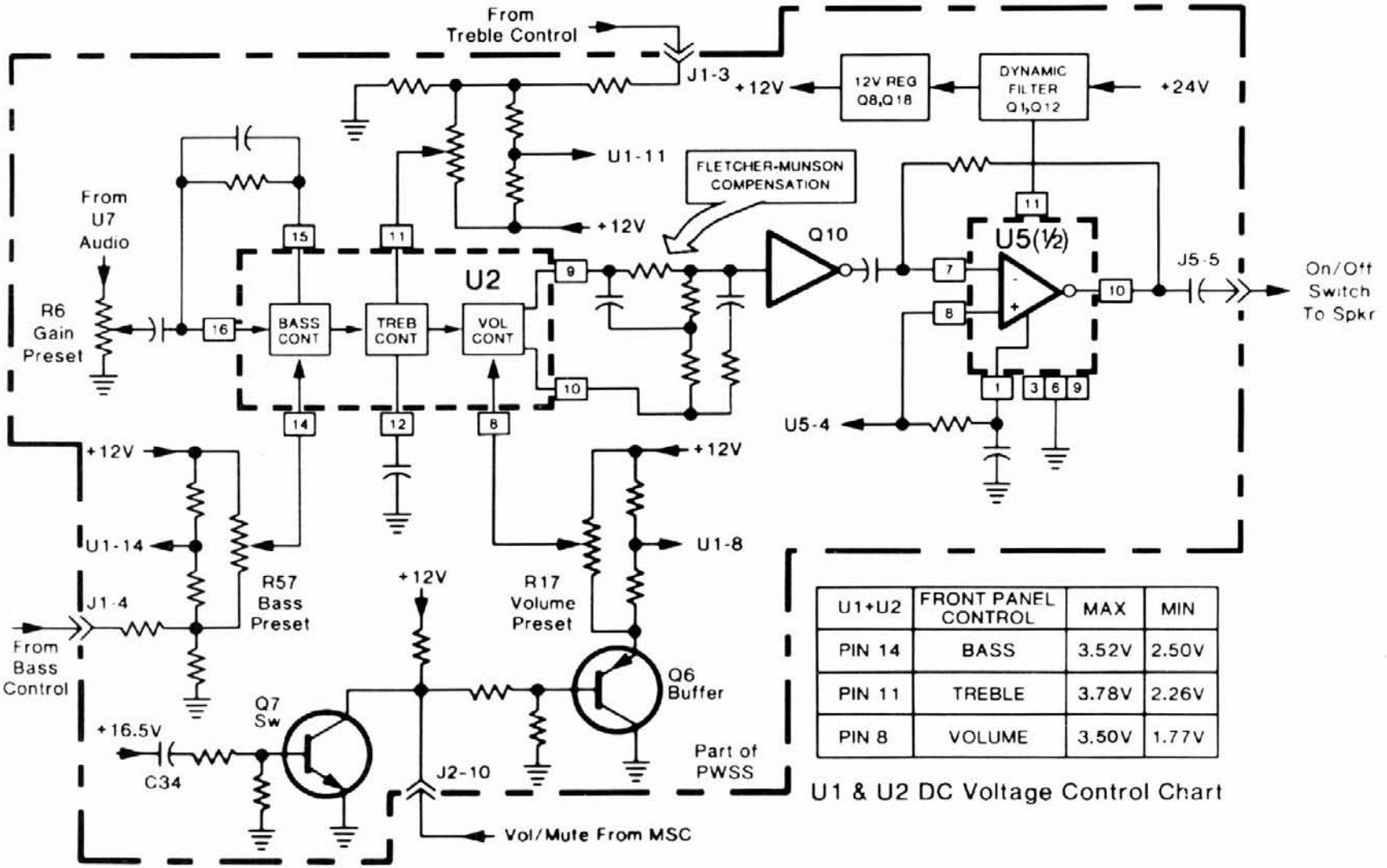
Audio Select/DNR Operation

The source of audio signal is selected by IC U3 from one of four possible stereo input sources: The audio input from the rear jacks panel, the auxiliary 1 or auxiliary 2 signal from the PWVIO circuit board assembly found in RCA's "Maxi" monitors or the audio input from the PWSB board, which was previously discussed. The audio input from the PWSB board, considered to be the selected television audio, is capacitively coupled to the audio output rear panel jacks on the rear of the monitor units. Integrated circuit U3 is a solid-state four-position two-pole switch. The switching position is a function of the control inputs at pins 9 and 10 of IC U3. In the "Mini" Monitor series of receivers, the control information is derived from the tuner control module. The appropriate "Hi's" and "Lo's" at pins 8 and 9 of J2 select the appropriate input source that is output at pins 3 and 13. In the case of RCA's ColorTrak 2000 "Maxi" series, there is no connection made to the MSC control module at connector J2. As a result, pins 8 and 9 are pulled up to B+ or logic "1" condition selecting the input signal at the "D" input of U3, which is derived from the audio input signal from the rear jacks panel.

In order to maintain minimum distortion of the audio signal, B+ for IC U3 is derived from a split power supply consisting of +5 volts at pin 16 and −5 volts at pin 7. The selected audio output is then routed from pins 3 and 13 of IC U3 to pins 2 and 13 of IC U7, the dynamic noise reduction integrated circuit. The audio signal input at pins 2 and 13 of IC U7 are added together and output at pin 5. This signal is routed through a filter circuit to pin 6, the input to an internal amplifier within U7. The output of the amplifier at pin 8 is passed through a bandpass filter circuit whose slope response characteristic generates a low output from 20 Hz to 1 kHz and a higher output signal at 7 kHz. The signal from the filter is then routed back to pin 9 of IC U7 where it is peak detected. As the signal frequency increases from low to a higher audio frequency, the signal level appearing at pin 9 of IC U7 increases. Therefore, the increase in signal level at pin 9 is peak detected, generating a DC voltage output proportional to the input level, which can be monitored at pin 10. The detected voltage is then input to two internal filter amplifiers within U7 whose bandwidth capabilities vary with the amount of control voltage. With an input signal between 20 Hz and 1 kHz, the control voltage at pin 10 is approximately 1.4 volts. To reduce audio noise, the frequency response of U7's internal amplifiers are at a low frequency and bandwidth, reducing background noise within the 3- to 7-kHz region. As the frequency of the incoming signal reaches a higher level, the peak detected audio develops a higher control voltage increasing the bandwidth of the amplifiers within IC U7, allowing the higher frequency signals to pass through to the output amplifiers.



PWSS Audio Process Board Service Position



U1+U2	FRONT PANEL CONTROL	MAX	MIN
PIN 14	BASS	3.52V	2.50V
PIN 11	TREBLE	3.78V	2.26V
PIN 8	VOLUME	3.50V	1.77V

U1 & U2 DC Voltage Control Chart

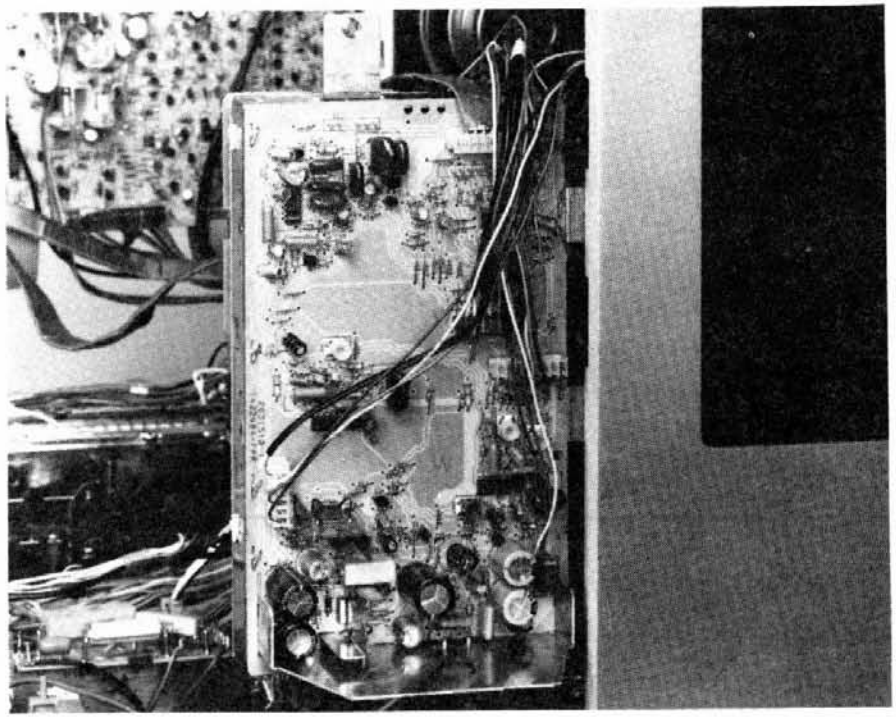
Volume/Tone Control/Output Amplifier Operation (Right Channel)

Volume/Tone Control/Output Amplifier Operation (Right Channel Only)

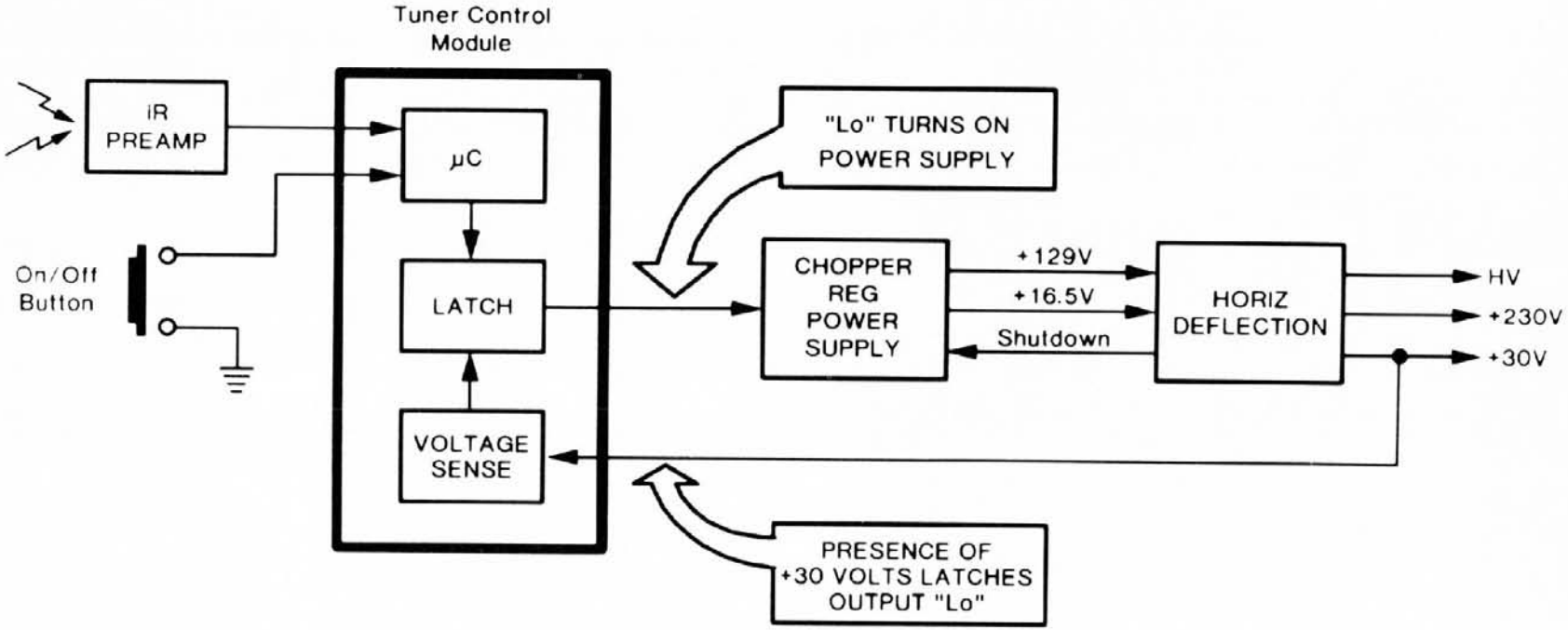
The audio output tone control circuitry on the PWSS circuit board contains identical circuitry for both right and left channels; therefore, only one channel (right channel) is discussed. The audio from the dynamic noise reduction circuitry is applied to gain preset control R6 and then to pin 16 of IC U2. The signal is then processed by the bass control circuitry within IC U2. The bass control circuitry is controlled by the DC voltage applied to pin 14. This voltage is derived from voltage divider control R57, the bass preset control. R57 is part of the voltage divider network that is controlled by the front panel bass control. Across R57 is a fixed voltage divider which passes a predetermined voltage to the left channel (U1, pin 14) proportional to the bass control voltage from the front panel. This supplies a fixed control voltage to the left channel process integrated circuit U1. As the front panel bass control is rotated, the amount of resistance in the voltage divider varies, causing a proportional change in the control voltage to both U2 and U1. The circuitry within IC U2 then alters its frequency characteristics, in the low frequency area of the audio spectrum, to adjust the bass response accordingly.

The output of the bass control circuitry with IC U2 is then internally passed to the treble control circuitry, which is controlled in a similar manner. The DC treble control voltage, input at pin 11 of IC U2, is derived from a voltage divider network whose output voltage is adjusted by the control voltage applied from the front panel treble control at connector J1, pin 3. The output of the treble control circuit within IC U2 is then passed to the volume control circuitry, which is gain controlled by the DC voltage applied at pin 8. The ground return for the voltage divider consisting of R17 is derived through Q6 and Q7. Transistor Q7 is "on" when power is first applied until capacitor C34 has completed the charge cycle. At this time, Q7 gradually turns "off," allowing Q6 to gradually turn "on," minimizing noises during a power "on" condition.

The audio output signal from IC U2, pins 9 and 10 is applied through the Fletcher-Munson compensation network to the input of buffer transistor Q10. The output of Q10 is then capacitively coupled to the input of audio output integrated circuit U5, pin 7. Within IC U5 is an internal reference voltage which is output at pin 1, filtered, and then routed to pins 4 and 8 of IC U5. The reference voltage biases the noninverting input stage of both output amplifiers, maintaining the output voltage of the output amplifiers at approximately 1/2 Vcc. The audio output signal from IC U5, pin 10, is then capacitively coupled to the speaker system of the receiver.



PWSS Audio Process Board Service Position



On/Off Control Operation

CTC 131 PWM Chopper Power Supply

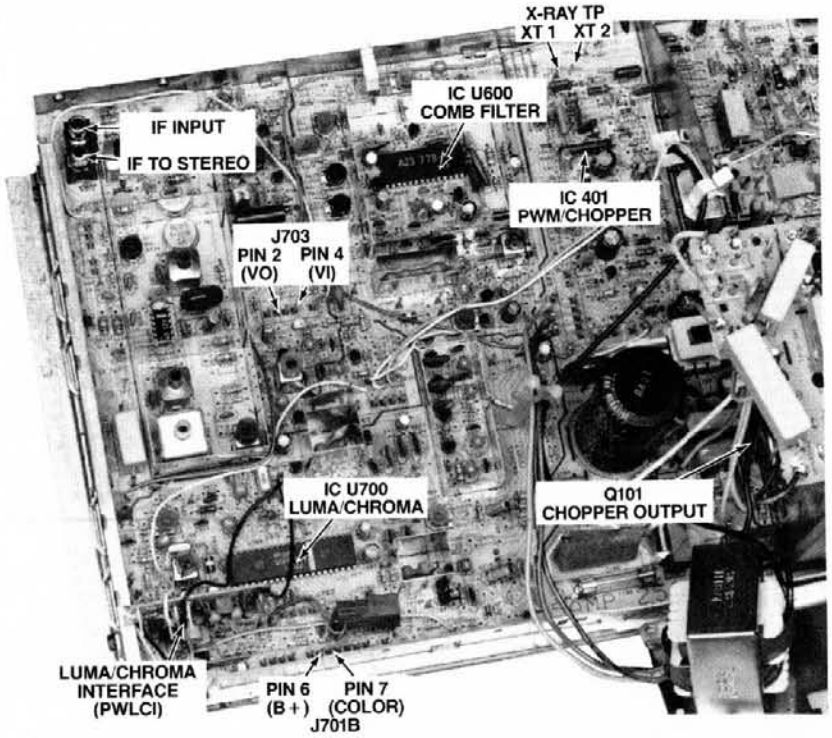
On/Off Control Operation

The CTC 131/132 television chassis utilizes an electronic latching type of power on/off control system. The tuner control module (MSC) controls the "on/off" condition of the chopper regulator power supply. With an "on/off" instruction from either the IR hand unit or the manual On/Off switch, the microcomputer within the tuner control module activates a latch (within the microcomputer) pulling the control line to the chopper regulator logic "Lo." The chopper regulator then outputs a variety of B+ power sources; two of which power the horizontal deflection system in the television receiver. The deflection system in the receiver then develops a variety of scan derived B+'s; one of which, the +30 volts, is routed back to the tuner control module and sensed by an internal circuit. This causes the MSC module to latch the control line in the logic "Lo" state keeping the power supply turned "on."

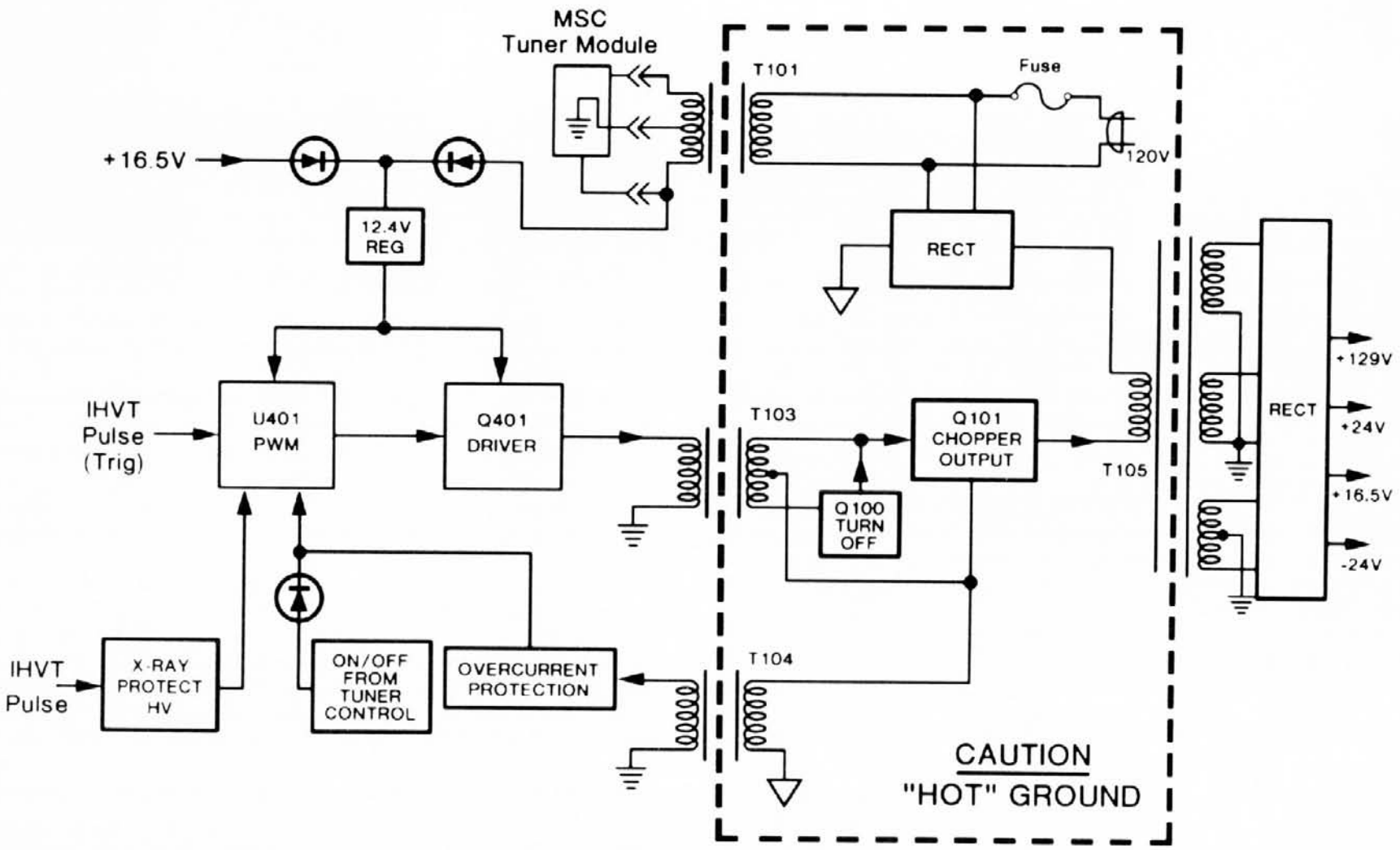
If in the event that some problem exists in the chopper regulator supply or the deflection system of the receiver, the +30 volts from the output of the IHVT would never be present, allowing the latch system within the tuner control module to keep the control line at a logic "Lo" state. As a result, the logic line would immediately go logic 'Hi' turning "off" the power supply. This operation takes only a few hundred milliseconds.

Because of the feedback loop to latch the on/off control system to the chopper regulator, servicing this circuitry becomes difficult. It is very important that the service technician recognize the feedback loop required to turn "on" the receiver, keeping the receiver in the "on" condition. Any failure in the chopper power supply or horizontal deflection system that causes loss of the +30 volts to the tuning control module causes the power supply to be turned "off." **Under no circumstances should the chopper regulator be forced into an "on" state without this protection mechanism of sensing the +30 volts from the output of the IHVT, unless a controlled state exists within the system,** as is described later in this publication.

Notice that the horizontal deflection system outputs a shutdown signal to the chopper regulator circuitry. As a result, if excessive high voltage exists, a shutdown command is applied back to the chopper regulator circuit turning "off" the output of the regulator. When the output of the regulator is turned "off," the B+ to the deflection system drops to zero. As a result, the output of the deflection system also drops to a safe level. At this time, the power supply turns "on," again applying power to the chassis. If excessive high voltage continues to exist, the power supply is toggled "off" and "on" until the problem has been resolved.



CTC 131 Television Chassis (Left Half)



PWM/Chopper Regulator Block Diagram

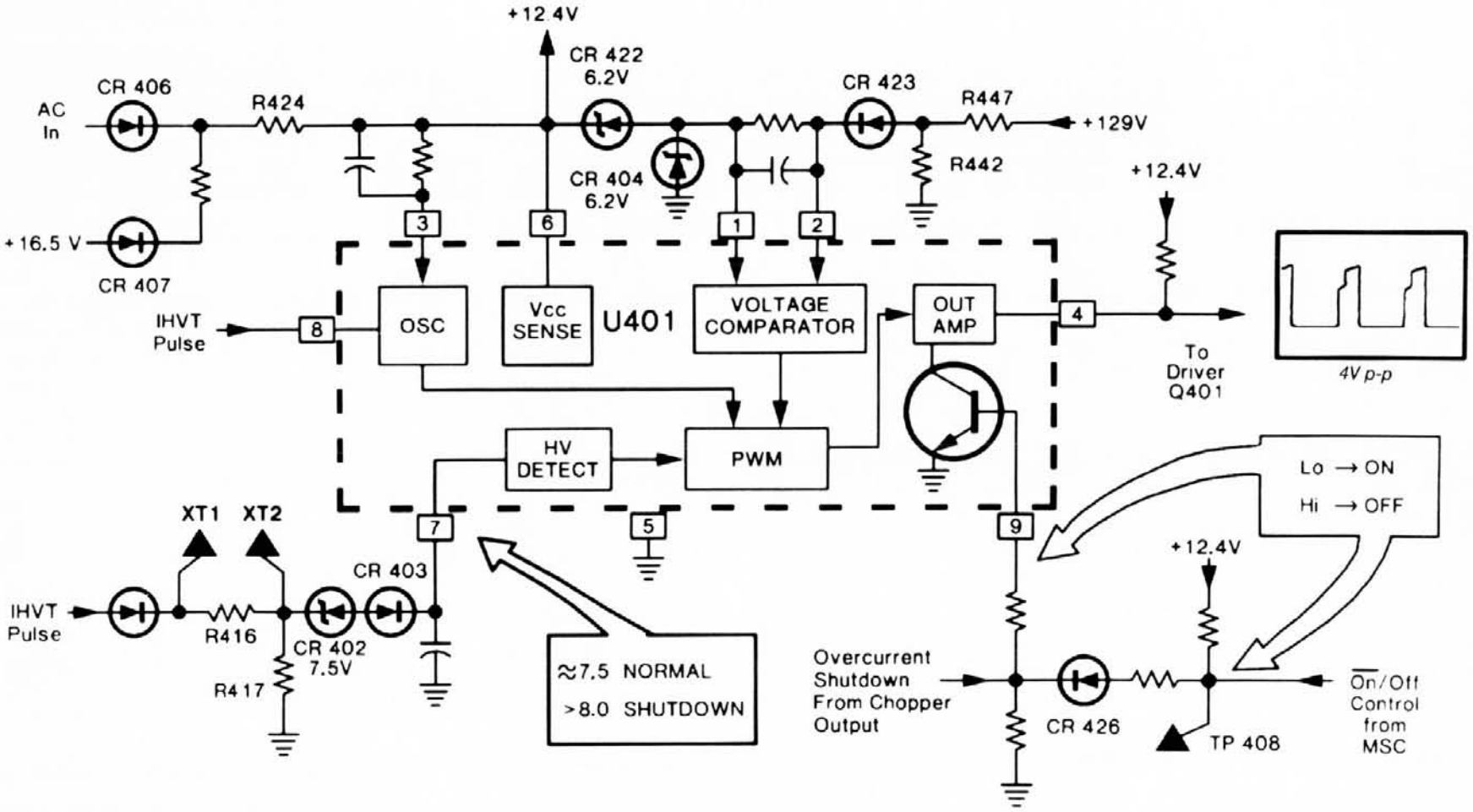
PWM/Chopper Regulator

The frequency of operation of the PWM (Pulse Width Modulated) chopper regulator is the same as the receiver's horizontal (15,734 Hz) circuitry. IC U401, the pulse width modulated regulator integrated circuit drives transistor Q401. Driver transistor Q401 is transformer coupled via T103 to the base of chopper output transistor Q101. The base circuit of Q101 contains a chopper turn-off transistor, Q100, to ensure that the chopper output transistor is in a turned "off" state when required. The chopper output transistor is then transformer coupled through T105 to a variety of rectifier diodes to generate **four B+ outputs** to power the television chassis. B+ power for the chopper output stage is supplied from a line rectified B+ source to the input or primary of transformer T105.

The 120-volts AC is also routed through step-down standby transformer T101, which halfwave rectifies the AC voltage. In addition, the ground return for the secondary of T101 is routed through the MSC control module. The rectified voltage (startup) is routed to a 12.4-volt regulator that maintains the proper B+ to the PWM regulator IC and driver transistor Q401. The output of Q401 is transformer coupled to the chopper output stage (Q100 and Q101). The emitter current of the chopper output transistor, Q101, is routed through the primary of transformer T104. The secondary of T104 is passed to an overcurrent protection circuit, which is coupled into the PWM integrated circuit On/Off control system. The sensing line protects the chopper circuit from damage by turning "off" the PWM IC in the event of excessive current demands by the chassis.

The chopper output circuit consisting of Q101 and turn-off transistor Q100 is contained in a circuit that is electrically interconnected to the remaining part of the chassis by transformers. As a result, the chopper output circuit is the only area of the television chassis that has a "HOT" ground system. During servicing the technician must utilize an isolation transformer at all times, even though 85% of the chassis is "COLD" grounded. The reason an isolation transformer must be used during servicing is that the technician could be monitoring circuitry in the "COLD" ground area of the chassis and then move to measure or check the circuitry in the chopper output stage, **which is a "HOT" ground area. Therefore, not using an isolation transformer could result in damage to the equipment, the receiver, or injury to the technician.**

To summarize, the chopper regulator integrated circuit, U401, is turned "on" or "off" by the control signal from the tuner control module. Again, it is also turned "off" by any indication of an overcurrent problem in the chopper output stage. Also, the IHVT sample pulse is monitored for excessive amplitudes by the X-ray protection circuit and in the event of excessive high voltage, the PWM system turns "off" its output signal.



Chopper Regulator PWM Operation

Chopper Regulator PWM Operation

B+ power is supplied to IC U401 as soon as the receiver is plugged into a 120-volt AC source. When the receiver is "off," B+ power is derived from the standby transformer through a halfwave rectifier, CR 406 and R424. The other end of the R424 is routed to pin 6 of IC U401 — the Vcc input and series zener diodes CR 422/CR 404 to ground. Internal to IC U401 is a Vcc sense circuit that senses the level of B+ to the input of the integrated circuit. If the B+ level exceeds 13.8 volts or falls below approximately 10 volts, IC U401 ceases operation.

The junction of the two zener diodes (CR 422/CR 404) is routed to pin 1 of IC U401 as a reference for the voltage comparator circuit. Connected to this 12.4-volt source, obtained at pin 6 of IC U401, is an R/C time constant connected to pin 3. The R/C time constant determines the internal oscillator freerunning frequency of approximately 15,000 Hz. When the television is turned "on," sample pulses from the IHVT appear at pin 8. The oscillator is triggered (minimum 1V peak) to run at the same horizontal frequency of the television chassis. This minimizes interference and beats that may occur from radiation from the chopper supply into the receiver circuitry.

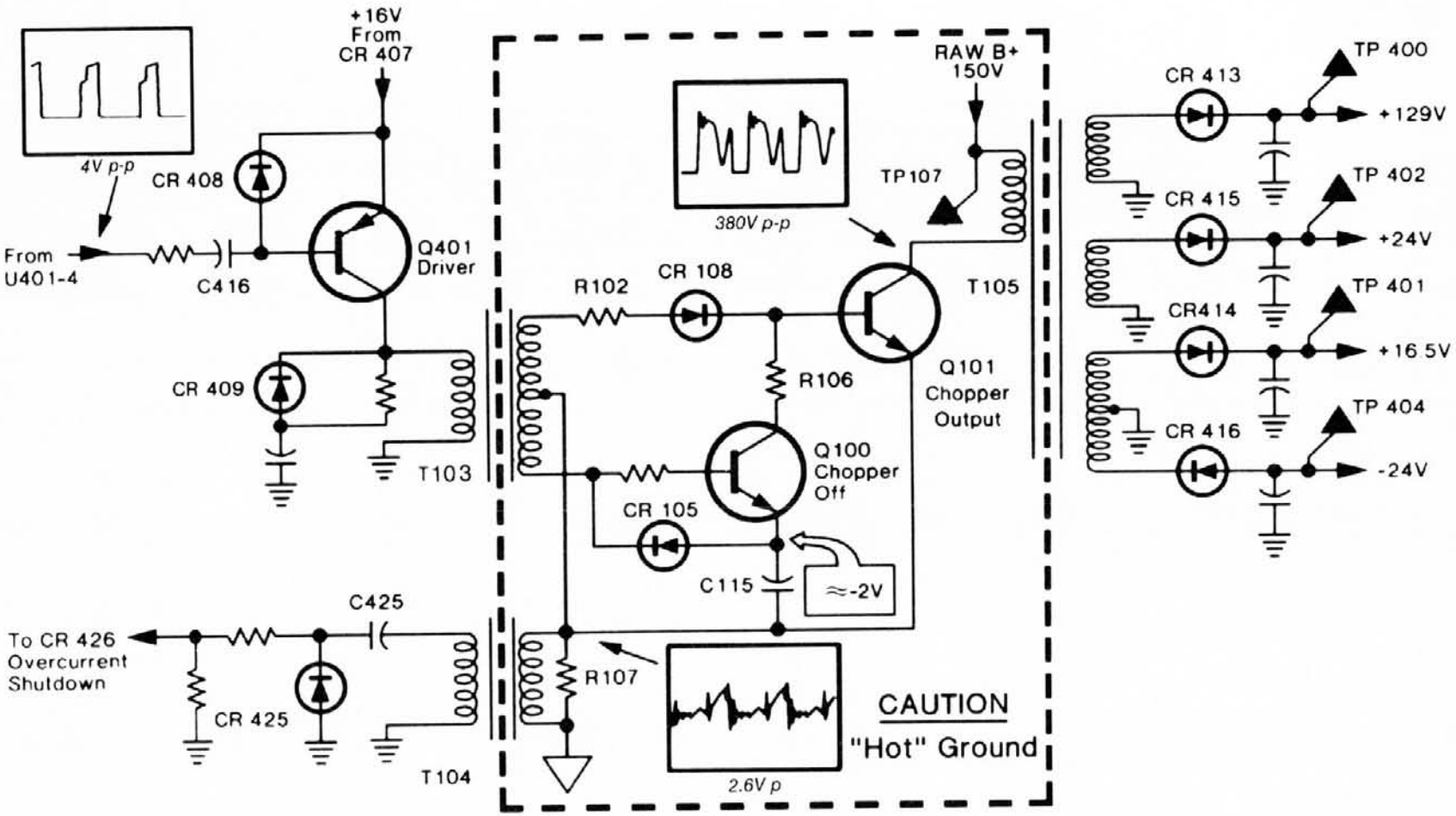
The output of the oscillator is then passed to the pulse width modulation circuitry within the IC along with a correction voltage from the voltage comparator circuit. The output of the pulse width modulator is applied to the output amplifier which is enabled by the logic signal at pin 9 of the integrated circuit. The output signal at pin 4 of IC U401 is present during the time pin 9 is pulled logic "Lo." When the receiver is turned "off," pin 9 is pulled logic "Hi." As a result, the drive waveform at pin 4 returns to zero, although the oscillator portion of the pulse width modulator is still functioning at approximately horizontal frequency. When the unit is turned "on," the output signal at pin 4 drives transistor Q401, which drives the output chopper transistor. With the presence of the output from the chopper supply, the +129-volt output source is sensed and passed through CR 423 to the input of the comparator at pin 2. The pulse width of the drive signal is varied to maintain the same DC voltage on pin 2 of U401 that is supplied by the reference voltage at pin 1 of IC U401.

The pulse width modulator (PWM) circuitry is also driven by the high voltage detector circuitry whose input is from pin 7 of IC U401. A sample of the IHVT pulse is rectified by CR 401 and passed through the X-ray shutdown voltage divider, through level sense zener diode CR 402 and diode CR 403. When the voltage appearing across R417 exceeds approximately 16 volts, the voltage at pin 7 increases above 7.5 volts. Therefore, when the input voltage at pin 7 reaches approximately 8 volts, the high voltage detect circuitry within the IC is activated, turning "off" the pulse width modulator circuitry within the integrated circuit. As a result, the chopper regulator output shuts down B+, stopping the output from the horizontal output stage.

When the IHVT pulse is reduced at the input of CR 402, the shutdown voltage is removed, resulting in the PWM system activating again to generate output. As a result, during an X-ray shutdown condition, a very noticeable visual "on/off" symptom appears. The "on/off" cycle occurs at approximately 0.5-Hz rate.

When the receiver is first attached to AC power, the on/off control input, pin 9 of IC U401, is pulled "Hi" via CR 426 and a resistor to the 12.4-volt source. Turning "on" the receiver requires removing the logic "Hi" on pin 9. This is accomplished via the control line from the MSC module to TP 408. The logic "Lo" turns "off the internal transistor, allowing the output amplifier to output the signal to driver Q401. To turn "off" the output amplifier, one of two methods must occur; either the logic signal from the MSC module returns to a logic "Hi" state or another input from the overcurrent shutdown circuit is applied to pin 9 at the anode of CR 426 forcing the chopper supply to turn "off."

When the chopper supply is fully operational, the +16.5-volt source output from the chopper regulator output stage is routed through CR 407, and a resistor supplying the remaining **run B+** to the PWM integrated circuit. The chopper regulator output circuit is discussed in the next section.



Chopper Regulator Output Circuit

Chopper Regulator Output Circuit

The pulse width modulated drive signal from IC U401, pin 4, is capacitively coupled to the base of driver transistor Q401. The charging action of capacitor C416, through the emitter base junction of Q401, turns the driver transistor "on." The discharge action of capacitor C416 is routed through the base bypass diode, CR 408. The collector of driver transistor Q401 is connected to the primary of transformer T103 and diode CR 409 through a capacitor to ground. The on/off period of driver transistor Q401 determines the amount of energy that is applied through transformer T103 to turn the base of driver transistor Q101 "on" and "off." The secondary center tap of driver transformer T103 is returned to the emitter of output chopper transistor Q101.

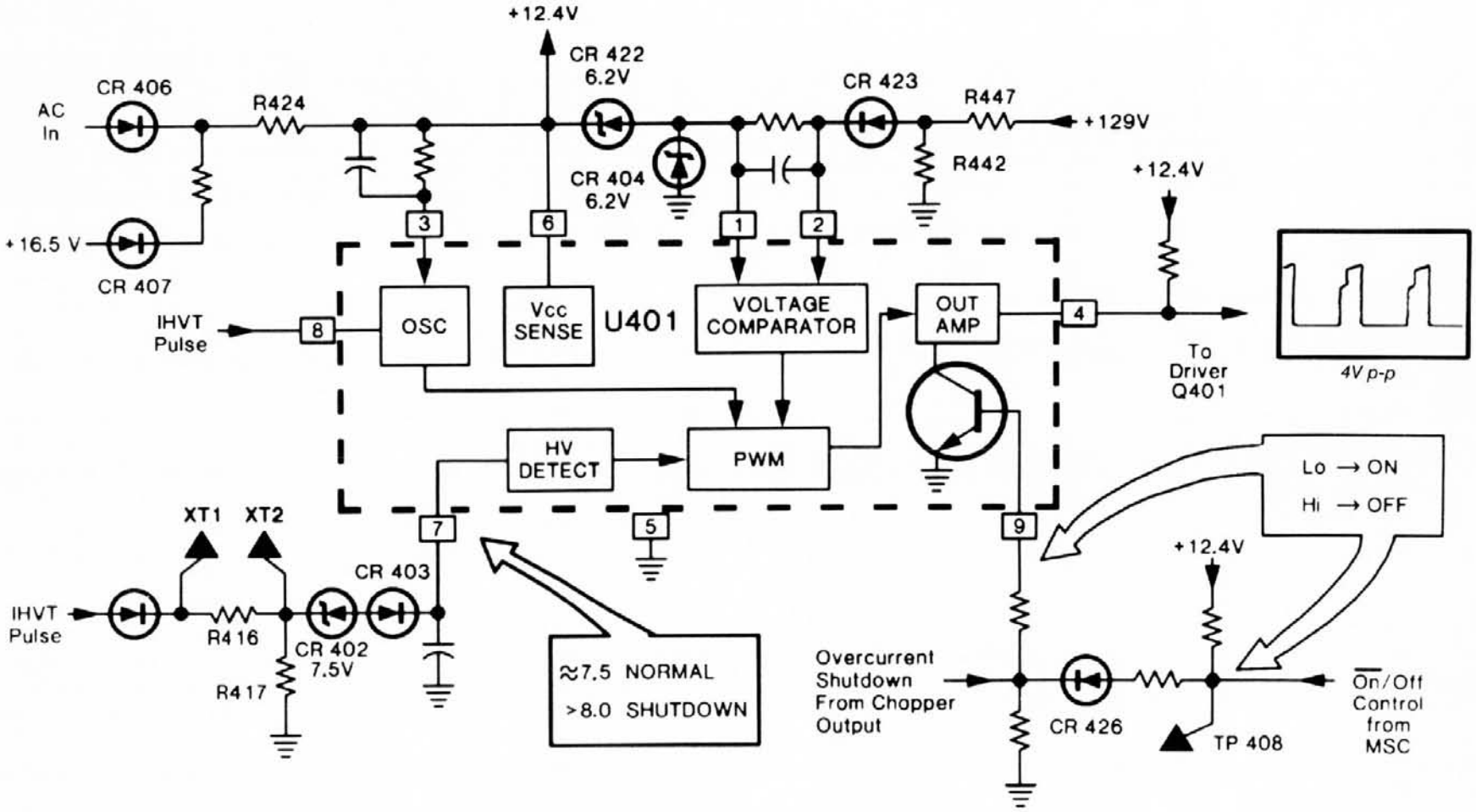
The top end of the secondary winding of T103 is connected through R102 and CR 108 to the base of the transistor Q101, providing the turn "on" current for the emitter base junction of Q101. At this same time, the voltage polarity across the lower half of the secondary winding causes CR 105 to conduct, charging capacitor C115 to a level of approximately −2 volts in reference to the emitter of chopper transistor Q101. When the polarity of the drive waveform changes, diode CR 108 turns "off" and the polarity of the bottom half winding of T103 causes the emitter base junction of transistor Q100 to be forward biased. As a result, Q100 saturates causing reverse current flow through R106 removing the stored charge in the emitter base junction of Q101 to ensure that the transistor **turns "off" very quickly.** It is very important in this operation that the turn "on" current and turn "off" current to the base of Q101 be maintained at the proper levels to ensure reliable operation of the chopper output transistor.

During servicing, the technician must measure the turn "on" and turn "off" currents to make certain they are at the proper levels before allowing the unit to be returned to the customer's home. Servicing of the chopper power supply is covered later in this manual.

The collector of the output transistor is coupled to the primary of the chopper output transformer, T105. The secondaries of T105 are rectified by CR 413 through CR 416 to develop four chopper output B+ sources (+129 volts, +24 volts, +16.5 volts, and −24 volts.) The +129 volts powers the horizontal and vertical deflection systems in the CTC 131/132 chassis. The +24-volt source powers the vertical and audio output circuitry. The +16.5-volt source supplies power to the run B+ input of the chopper oscillator, the audio circuitry, and the majority of the signal processing circuitry of the CTC 131/132 chassis. The −24-volt source is mainly used as a reference for the automatic kine bias (AKB) circuitry located on the rear of the picture tube.

The emitter of Q101 is routed through the primary of transformer T104 and resistor R107 to ground. Variations in emitter current of transistor Q101 are passed through transformer T104 through a peak-to-peak detector and on to the overcurrent shutdown input of the chopper regulator integrated circuit at the anode of diode CR 426. If an overload condition exists in the output circuitry of the chopper supply or in a load somewhere in the television chassis circuitry, an increase in the emitter current of Q101 occurs. As a result, peak current is sensed by the level detector system within the chopper supply and when the threshold level is detected, the chopper supply turns "off."

As mentioned previously, the circuitry surrounding the chopper turn-off transistor and chopper output, Q100 and Q101 respectively, are referenced to the "HOT" ground of the chassis. As a result, it is important that the technician utilize an isolation transformer when servicing this area and any other area of the chassis.



Chopper Regulator PWM Operation

Chopper Power Supply Troubleshooting

Note: Once the technician has determined a chopper power supply failure and confirmed proper horizontal deflection circuit operation (through the use of the In-Home, In-Shop, and Horizontal Deflection Troubleshooting Flowcharts), he then may proceed with the steps outlined below.

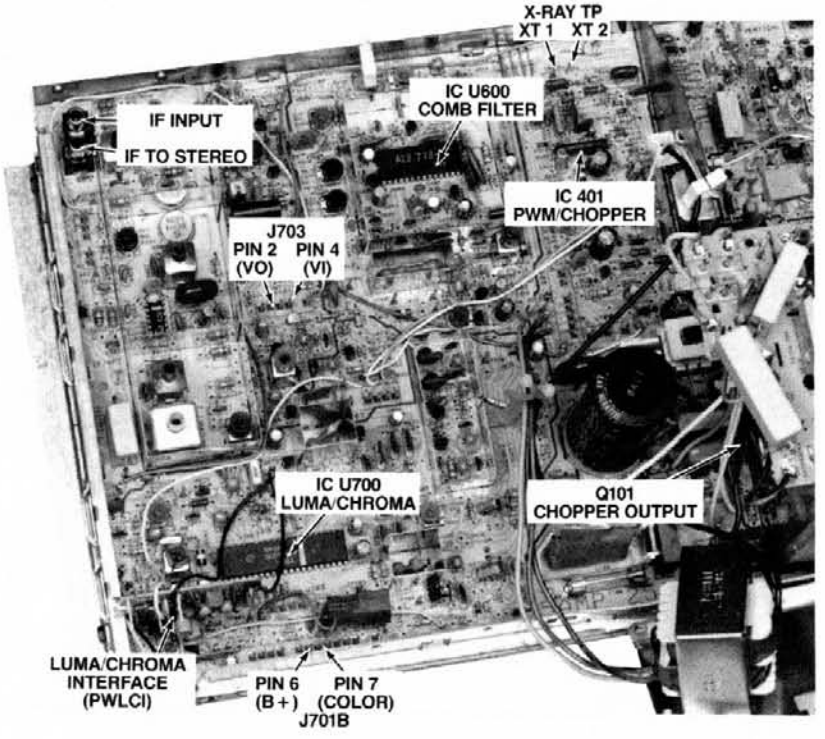
In order to assure reliability of the chopper power supply, a series of measurements consisting of **five steps are required to ensure proper performance and operation** of the chopper power supply system. During the isolation and measurement procedures, if a defect is found within the first or second step, **do not** assume that the repair is complete, allowing the unit to be returned to the customer's home. The technician must complete **all five steps** as required in this procedure to ensure the overall performance of the chopper supply is correct.

The operation of the PWM integrated circuit, Q401 driver stage, and base drive to the output chopper transistor **must be confirmed before full power is allowed to be supplied to the chassis circuitry.** As a result, step 1 requires removal of the mounting screws from the chopper and horizontal output transistors. Step 2 requires the technician to apply 120-volts AC to the power input cord of the receiver, confirm the proper B+ level at pin 6 of IC U401 and the reference voltage of 6.2 volts be present at pin 1 of IC U401. If these B+ sources are not present or correct, then service the appropriate regulator zener diode or standby power supply.

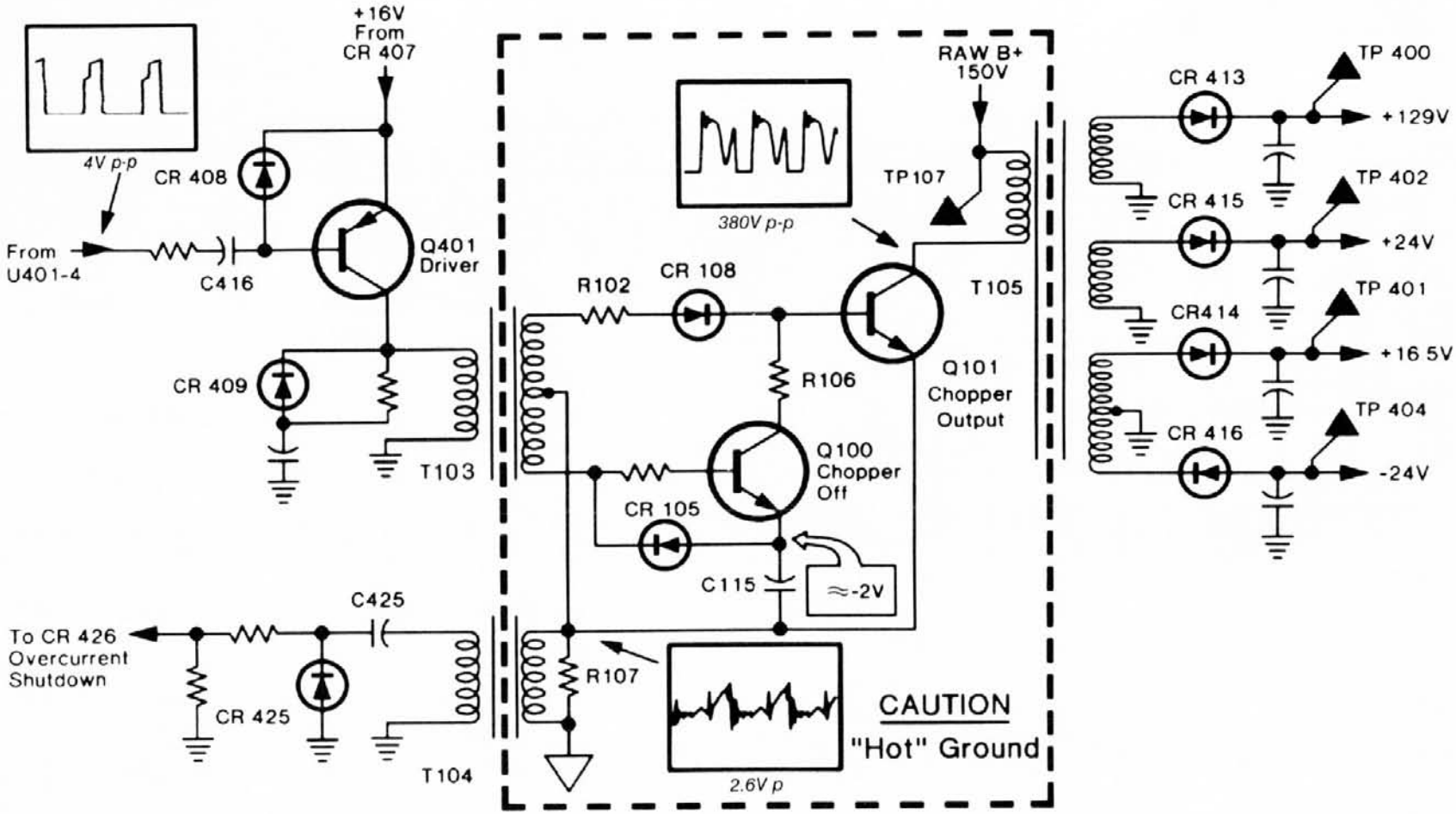
Chopper Power Supply Troubleshooting

Step 1 **Remove mounting screws from chopper output and horizontal output transistors.**

Step 2 **Apply 120V AC to TV and confirm proper +12.4 volts at U401-6 (cathode of CR 422) and +6.2 volts at U401-1 (cathode of CR 404). If these DC voltages are not present, turn set "off" before proceeding to next step.**

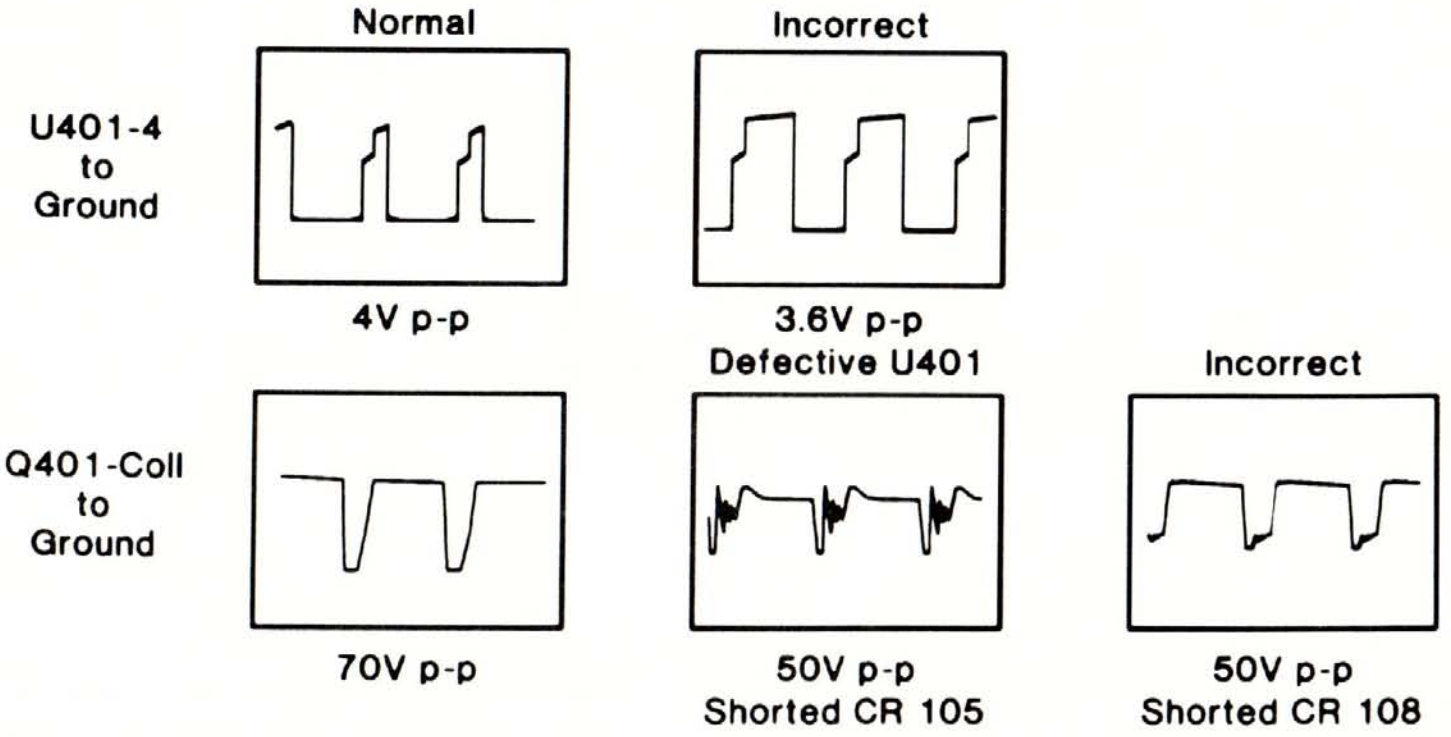


CTC 131 Television Chassis (Left Half)



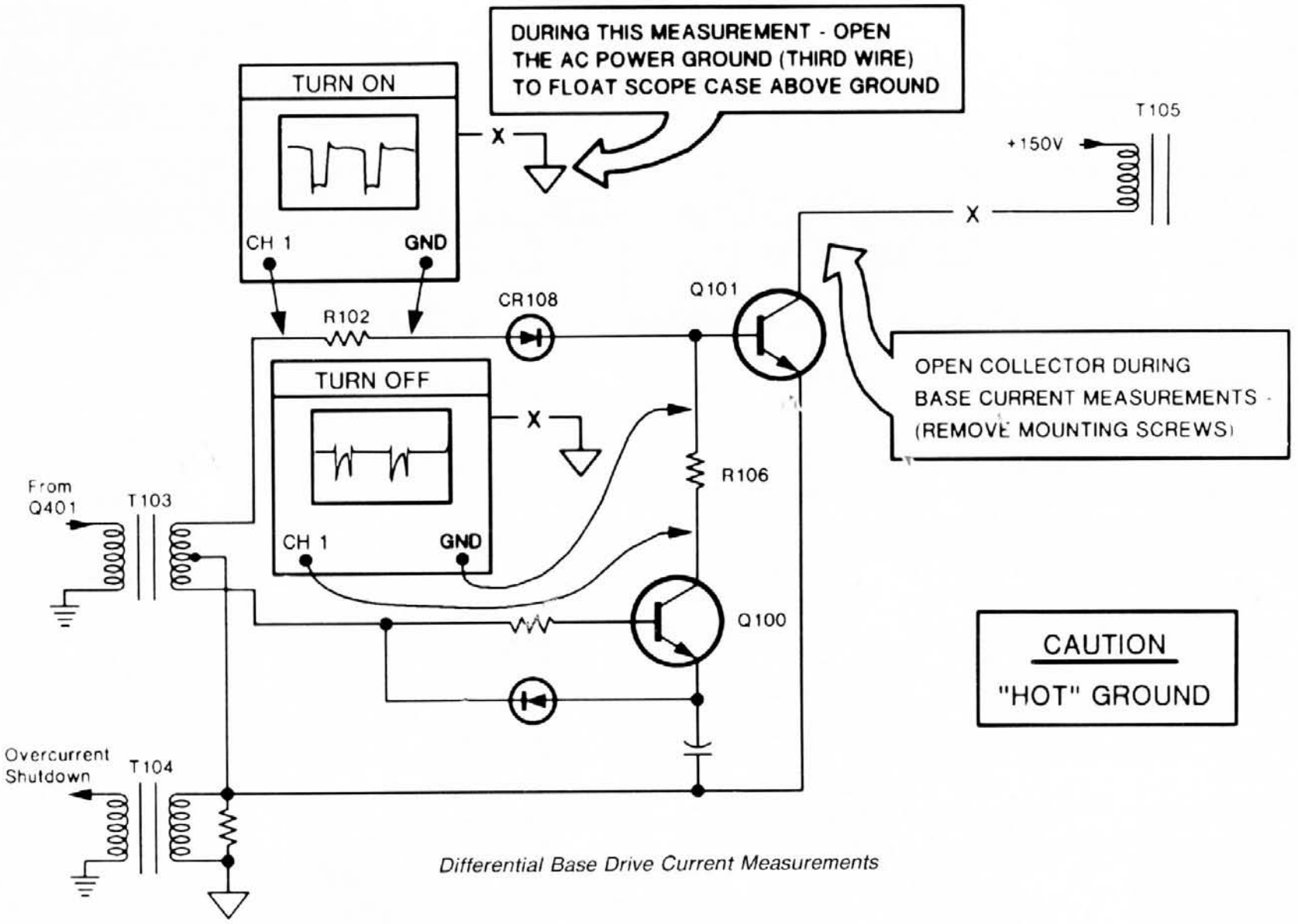
Chopper Regulator Output Circuit

Step 3
- Remove chopper output (Q101) mounting screws.
- Do not apply AC power to chassis.
- Ground TP 408.
- Apply external +16.5 volts at cathode of CR 414 (TP 401).



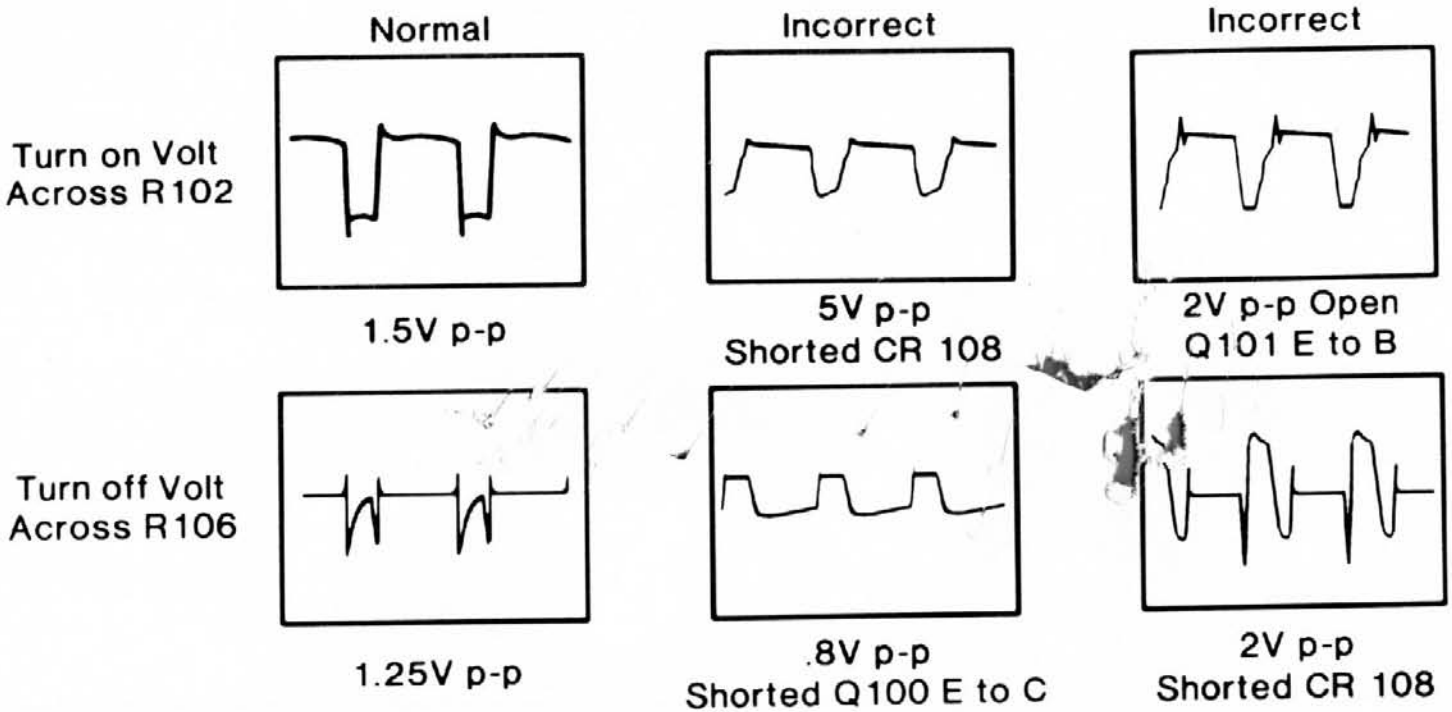
Step 3 requires the removal of the mounting screws (if not already done) from chopper output transistor Q101. **Do not** apply AC power to the chassis. Ground TP 408 and apply an **external +16.5 volts** at the cathode of diode CR 414 (TP 401). With an oscilloscope, monitor the waveform at the PWM output of IC U401, pin 4, for a normal 4-volt peak-to-peak waveform. In almost all instances, if the duty cycle or waveshape of this waveform is incorrect, it is most likely due to a defective IC U401.

Then monitor the output waveform at the collector of driver transistor Q401 for a normal waveshape and approximately 70-volts peak-to-peak amplitude. With the use of external B+ input, the technician can safely service this area without damaging costly components. If the waveform is found to be incorrect, suspect a possible defective component in the collector circuit of the driver transistor (Q401) or possibly in the secondary of the driver transformer (T103). Typical examples of resultant waveforms with inserted defects in the secondary circuit are shown. The technician should make every effort to ensure that the collector driver waveform is correct before proceeding on to the next measurement as an error in this waveform generates an error in the next measurement phase.



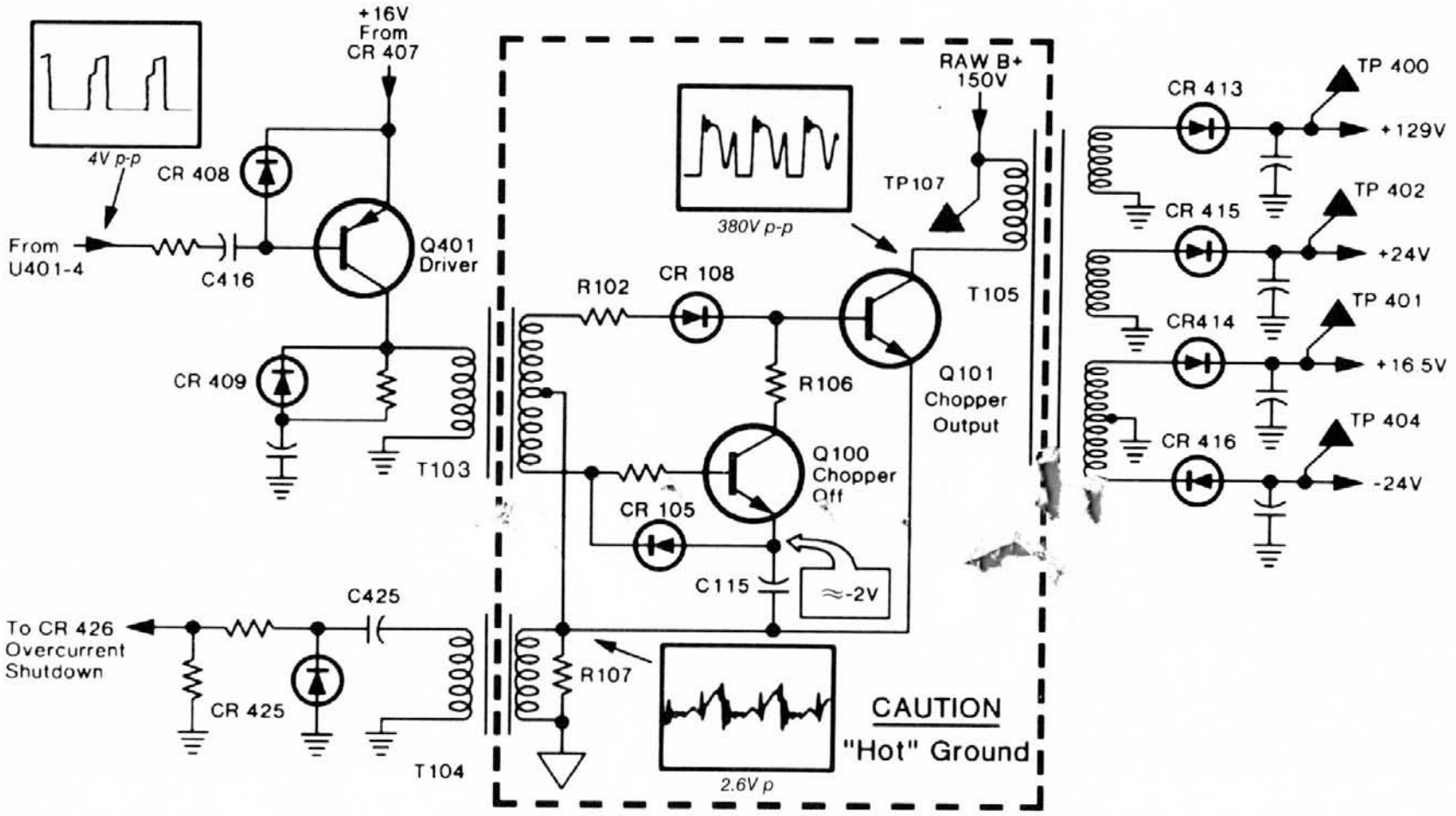
Differential Base Drive Current Measurements

Step 4
- Remove chopper output (Q101) mounting screws.
- Do not apply AC power to chassis.
- Ground TP 408.
- Apply external +16.5 volts at cathode of CR 414 (TP 401).



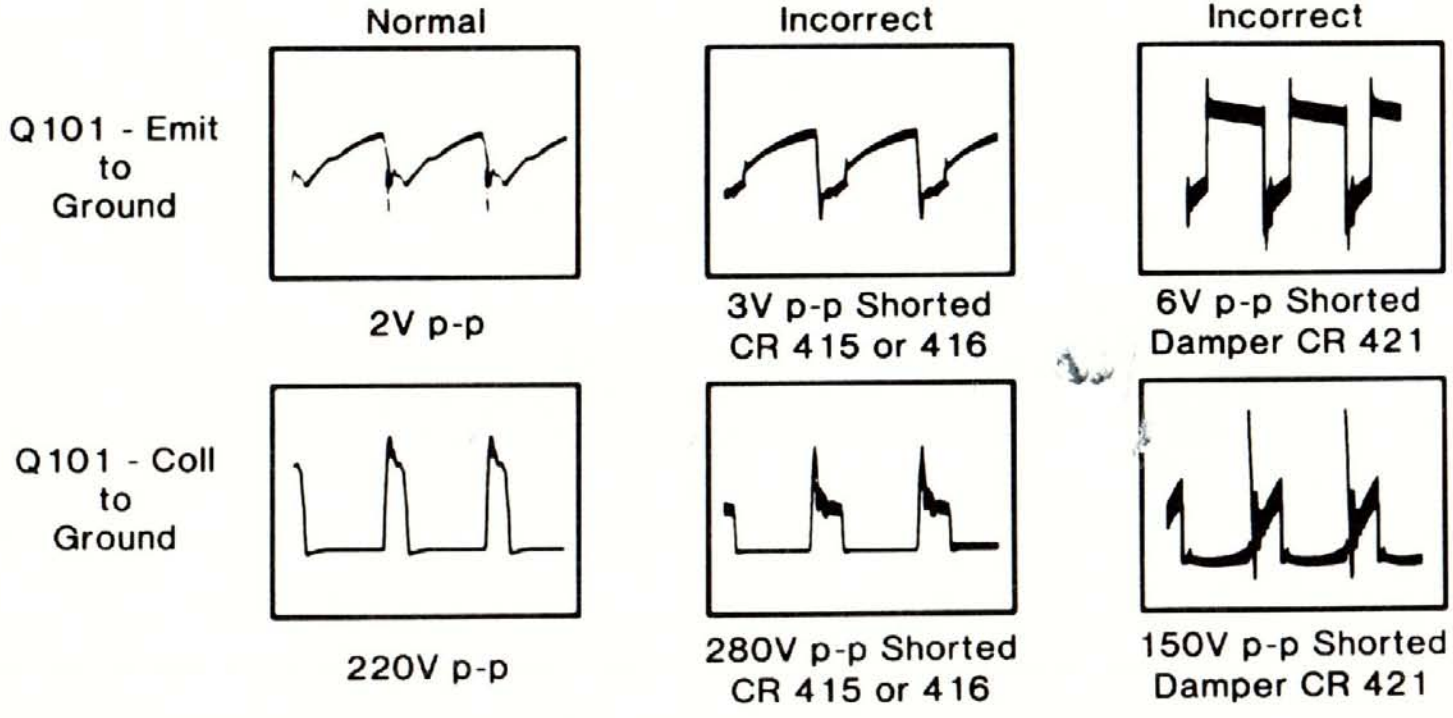
Step 4 requires the removal of the chopper output transistor (Q101) mounting screws. **Do not** apply AC power to the chassis. Ground TP 408 and apply an external +16.5 volts at the cathode of CR 414 (TP 401). Measure the differential voltage across R102, which indicates the **turn "on" current** supplied to the base of chopper output transistor Q101. Utilize the procedure as shown in the above drawing. If the resistive value of R102 is the proper value, the normal peak-to-peak waveform amplitude should be approximately 1.5-volts peak-to-peak. If this waveform is incorrect, possible problems could be because of a short in coupling diode CR 108 or a possible problem in the turn off circuit consisting of R106, Q100, or even a problem in the emitter base junction of Q101.

Measure the **turn "off" current** of the emitter base junction of Q101 by monitoring the differential voltage across resistor R106 using two channel inputs to the oscilloscope. With the proper resistance value of R106, the amplitude should be approximately 1.25-volts peak-to-peak. If abnormal, probable problems exist in diode CR 108, transistor Q100, or possibly output transistor Q101. Again, it is important that the technician achieve the proper waveforms at this point before proceeding, this ensures that damage does not occur to any other components in the chopper power supply/regulator system.

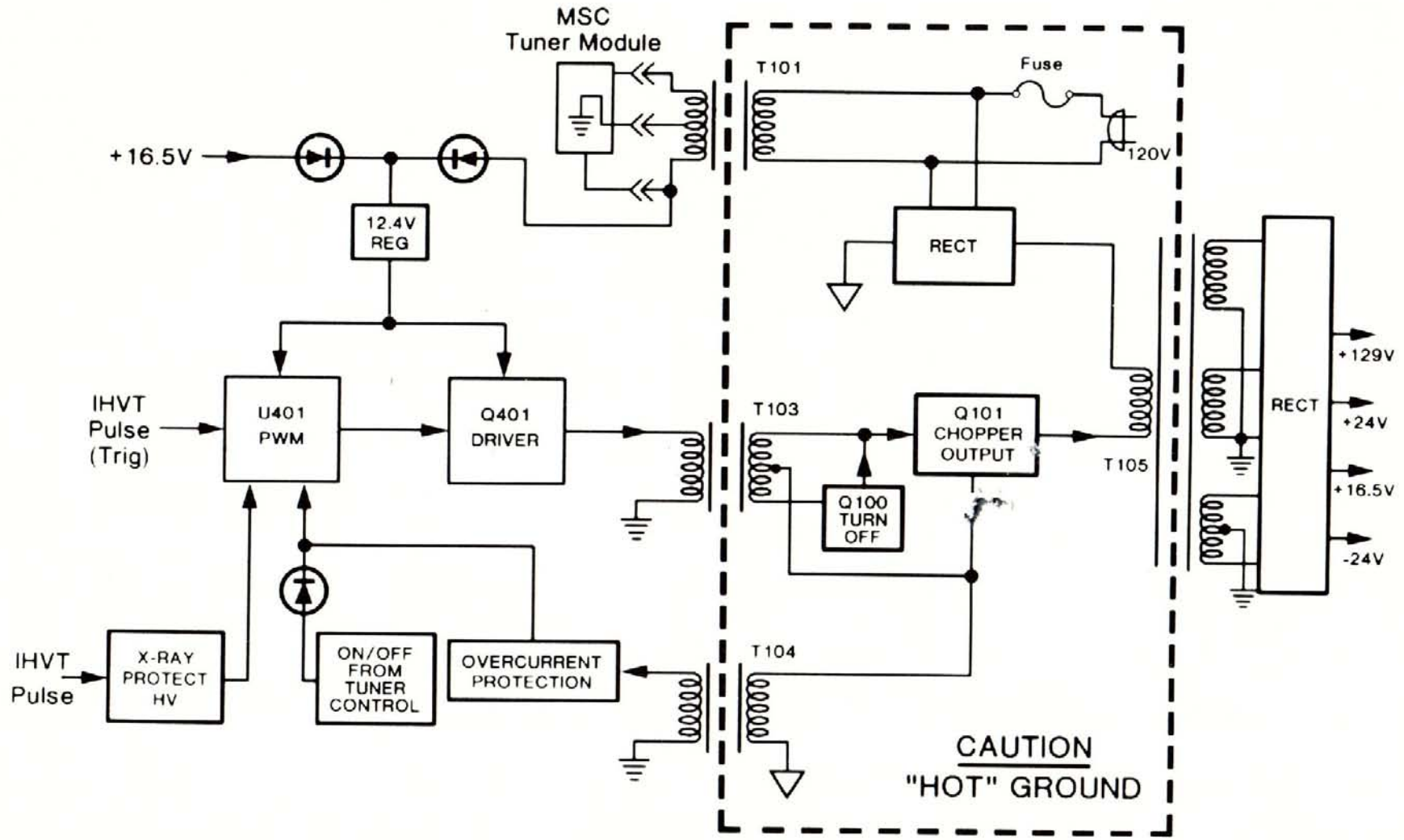


Chopper Regulator Output Circuit

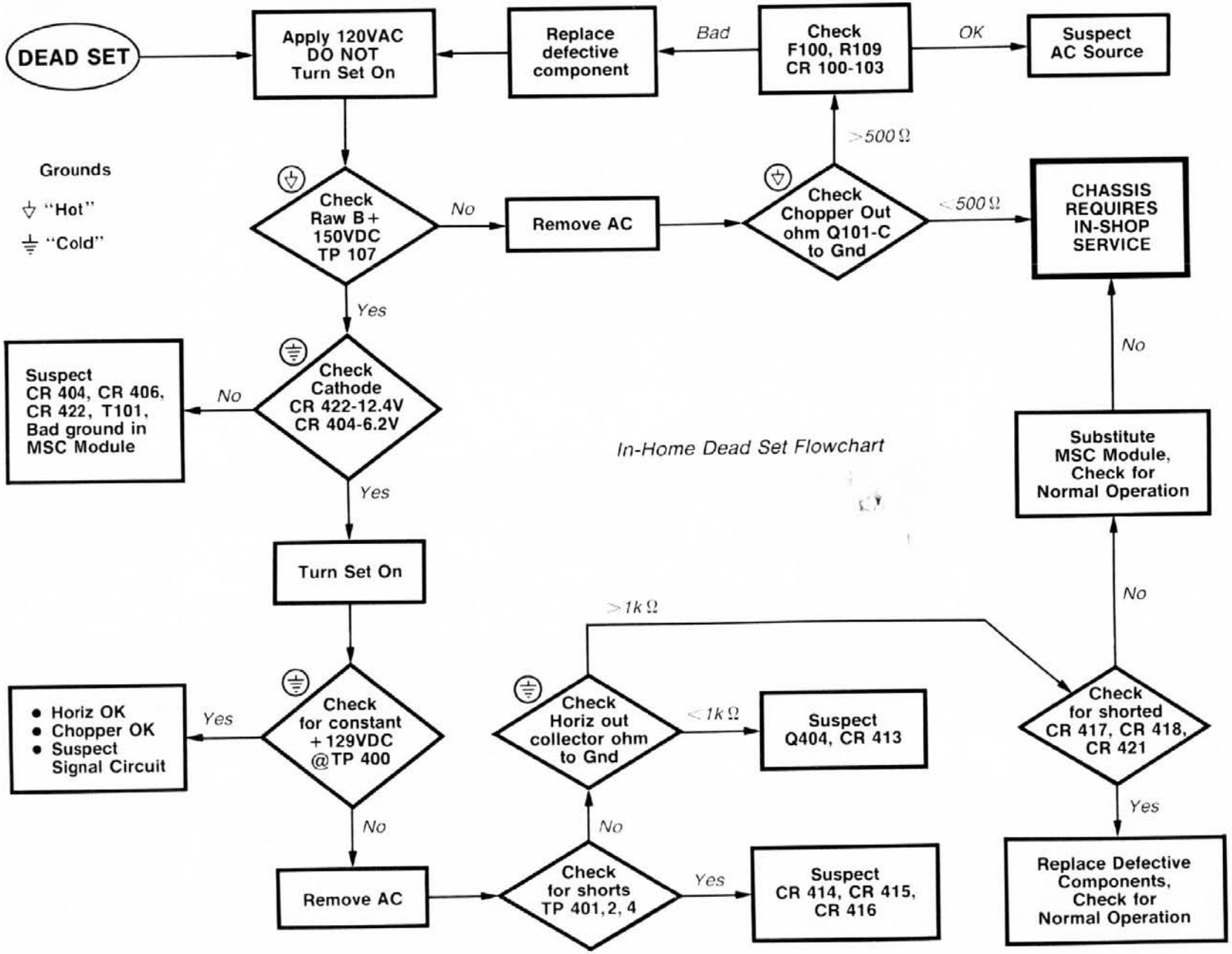
Step 5
- Replace chopper output (Q101) mounting screws.
- Remove horizontal output (Q404) mounting screws.
- Ground TP 408 - Apply external +16.5 volts at cathode of CR 414.
- Slowly raise AC line voltage (max of 25 volts) while monitoring emitter voltage (indicates cathode current) and collector voltage of Q101.

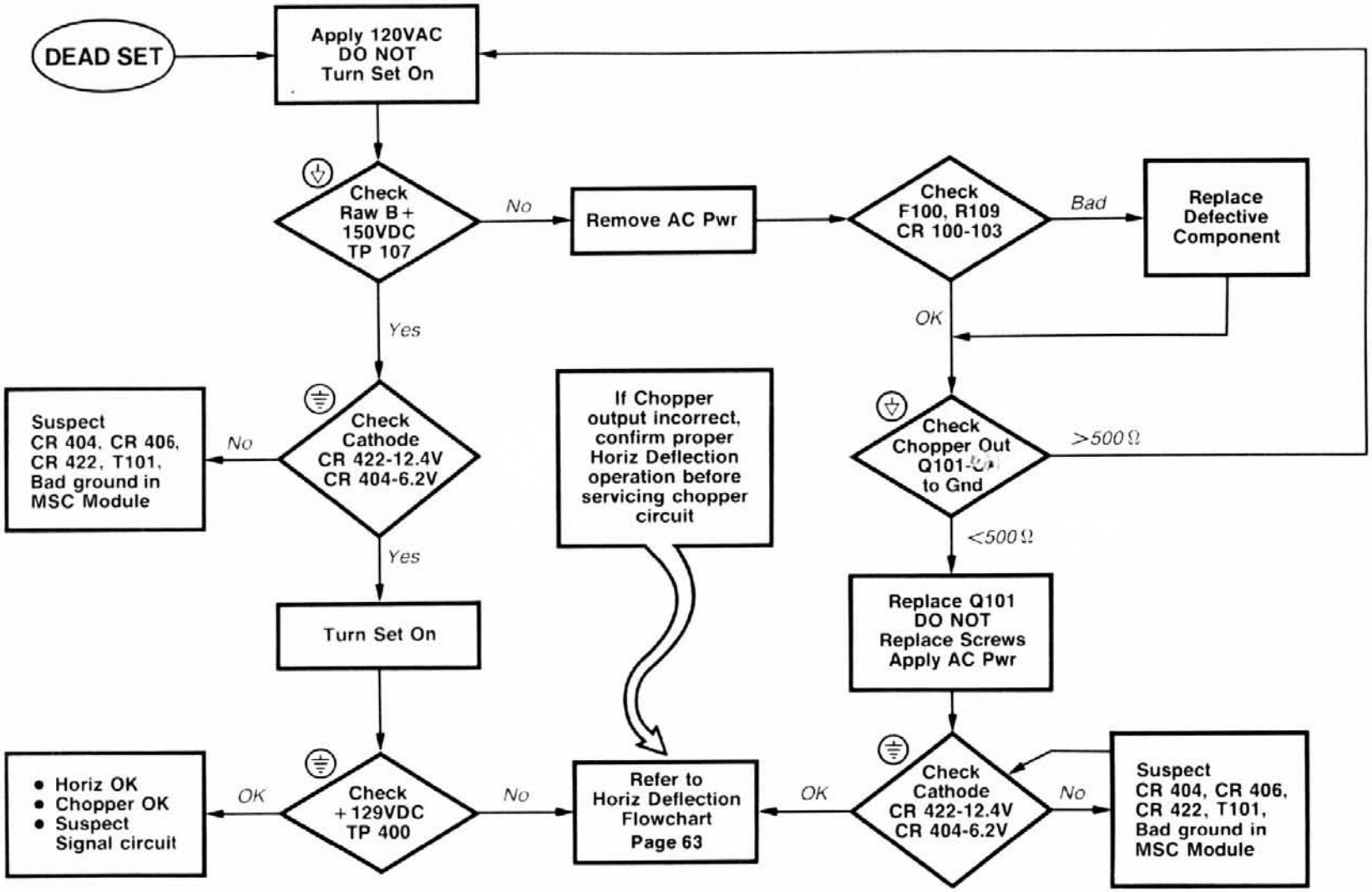


Step 5 requires re-installation of the chopper output mounting screws and removal of the horizontal output mounting screws. Ground TP 408 and apply an external +16.5 volts to the cathode of CR 414 (TP 401). While monitoring emitter voltage of Q101, which indicates the emitter current of the chopper output transistor and the collector voltage of the chopper output transistor, slowly raise the AC line voltage. **CAUTION:** Do not exceed an AC input voltage of 25-volts AC. Monitor the emitter voltage and collector voltage of Q101 for any indications of an excessive load of the chopper supply. If an excessive load exists on the chopper output circuitry, the emitter waveform is larger than 2-volts peak-to-peak and the waveshape distorted, as indicated by the examples. Also, the collector output signal also varies in both amplitude and waveshape with a defective or abnormal load condition on the output of the chopper supply. With the horizontal output stage disabled, confirm that the chopper supply is operating properly and normal loads exist. Then refer to the isolation troubleshooting techniques of the horizontal output stage, which are discussed later in this publication.

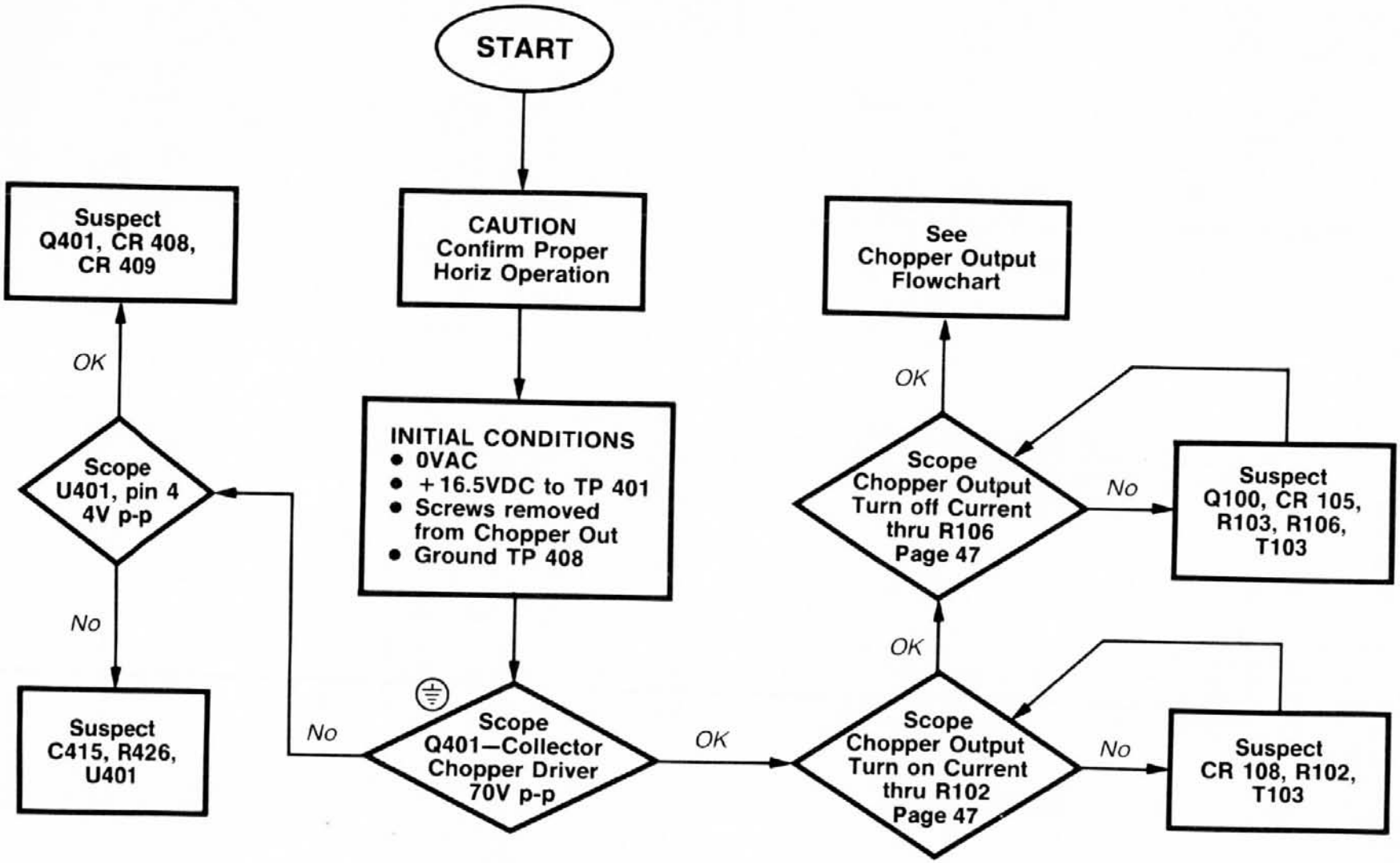


PWM/Chopper Regulator Block Diagram

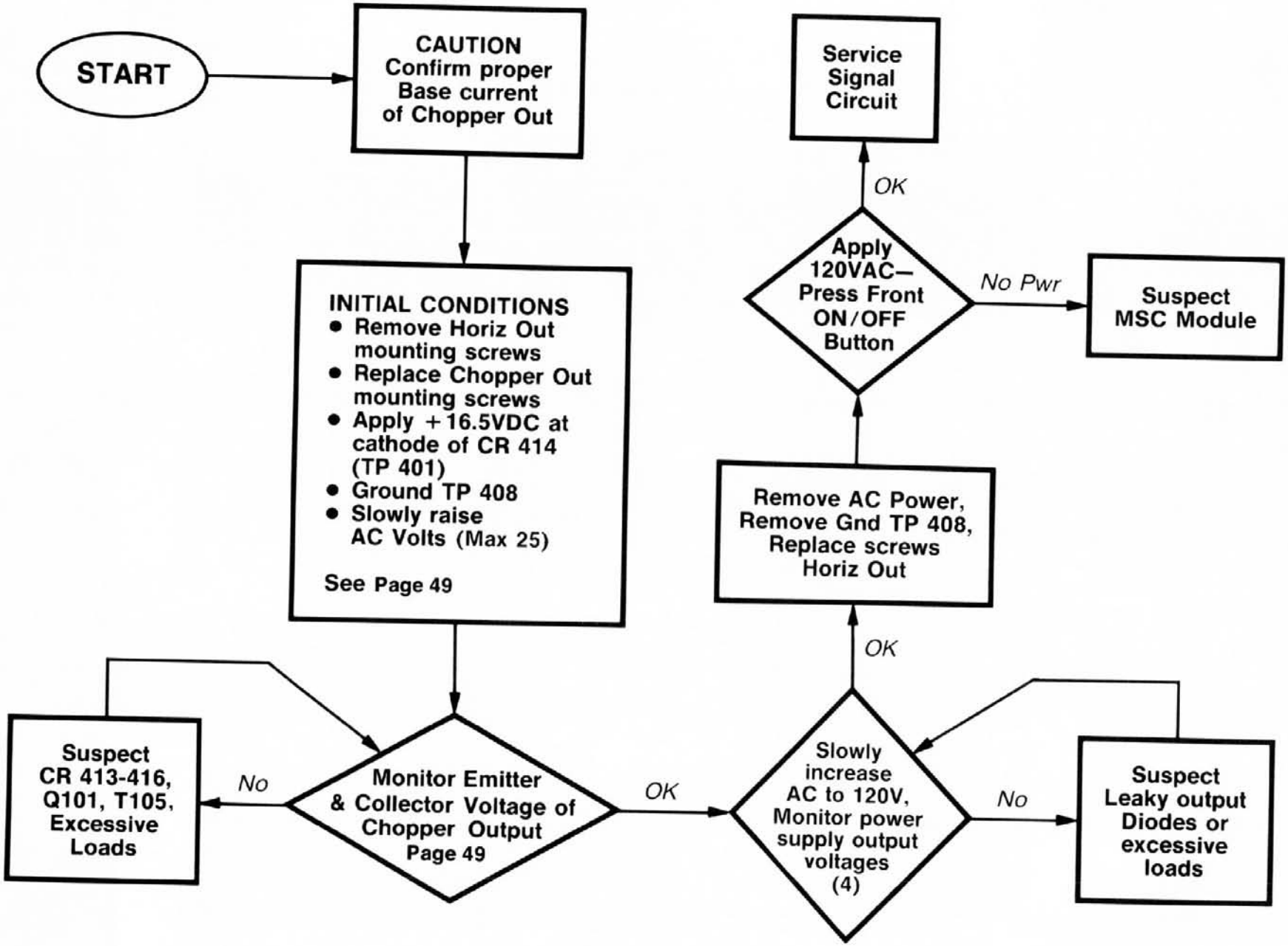

DEAD SET
Apply 120VAC DO NOT Turn Set On
Replace defective component
Bad
Check F100, R109 CR 100-103
OK
Suspect AC Source
Grounds
"Hot"
"Cold"
Check Raw B+ 150VDC TP 107
No
Remove AC
>500Ω
Check Chopper Out ohm Q101-C to Gnd
<500Ω
CHASSIS REQUIRES IN-SHOP SERVICE
Yes
Suspect CR 404, CR 406, CR 422, T101, Bad ground in MSC Module
No
Check Cathode CR 422-12.4V CR 404-6.2V
In-Home Dead Set Flowchart
No
Substitute MSC Module, Check for Normal Operation
Yes
Turn Set On
>1kΩ
No
Horiz OK
Chopper OK
Suspect Signal Circuit
Yes
Check for constant +129VDC @TP 400
Check Horiz out collector ohm to Gnd
<1kΩ
Suspect Q404, CR 413
Check for shorted CR 417, CR 418, CR 421
No
Yes
Remove AC
Check for shorts TP 401, 2, 4
Yes
Suspect CR 414, CR 415, CR 416
No
Replace Defective Components, Check for Normal Operation



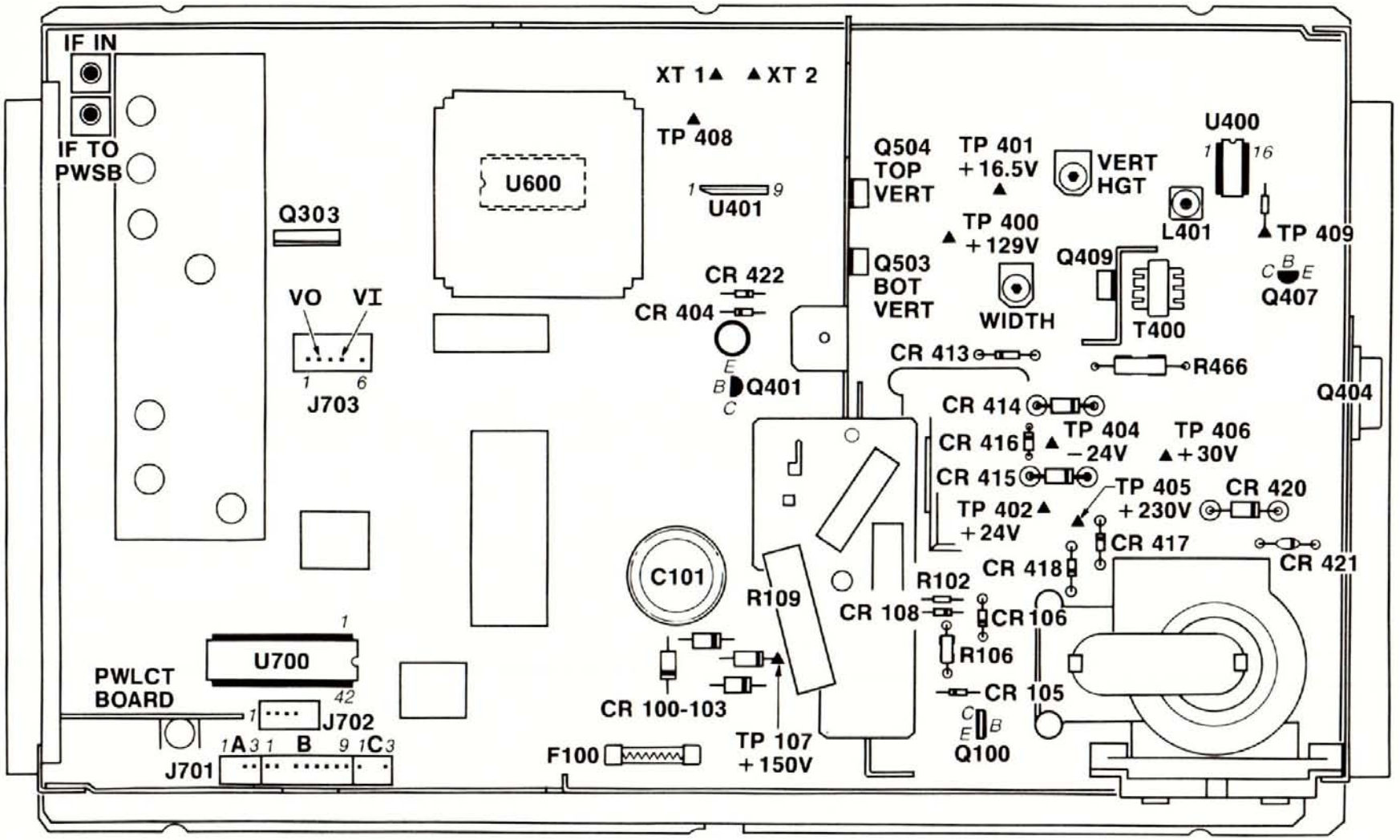
In-Shop
Dead Set Troubleshooting
Flowchart



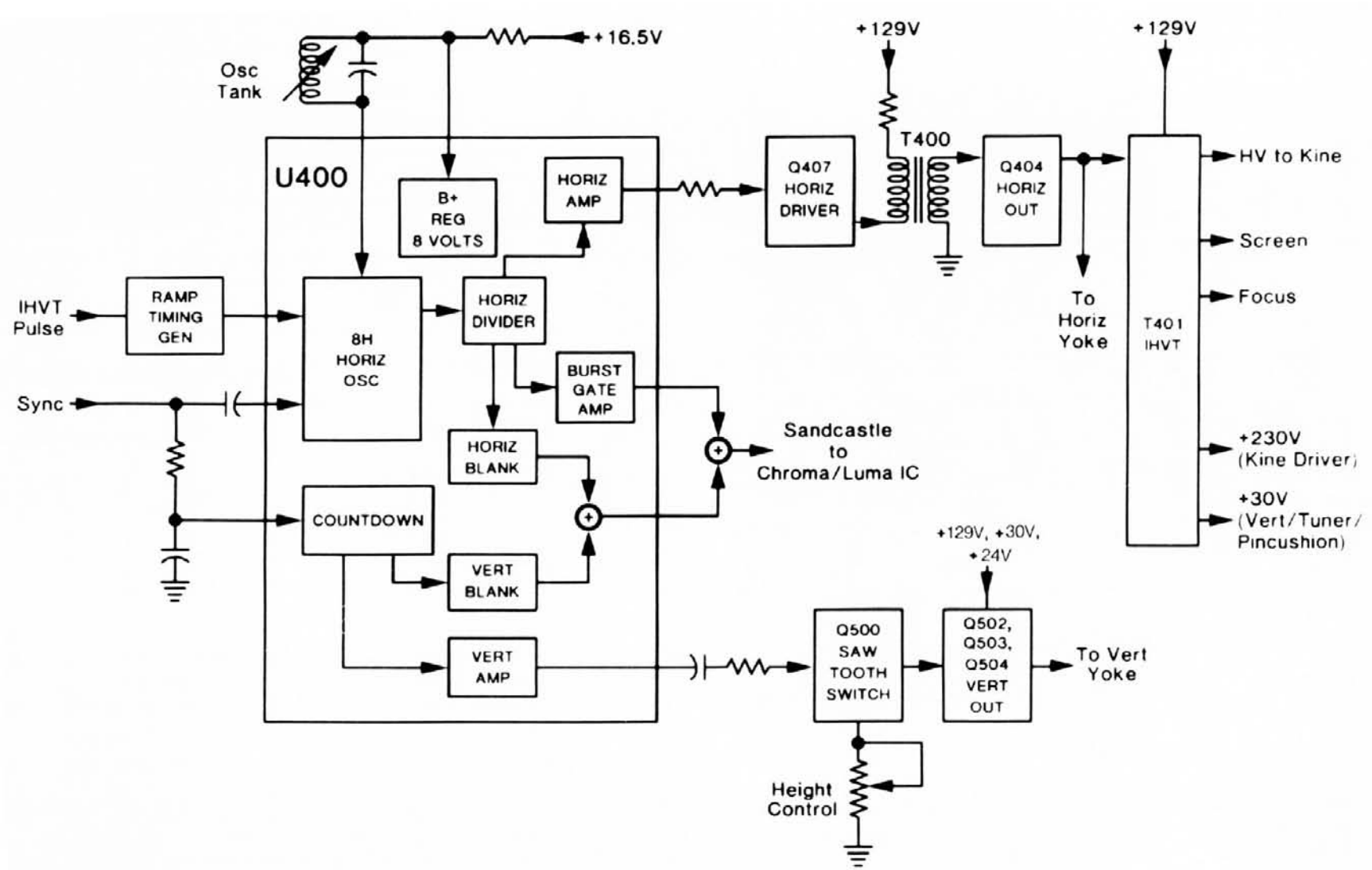
Power Supply PWM Drive Troubleshooting Flowchart



Chopper Output Troubleshooting Flowchart



CTC 131 TV Chassis Component Location
(Top View)



Deflection Block Diagram

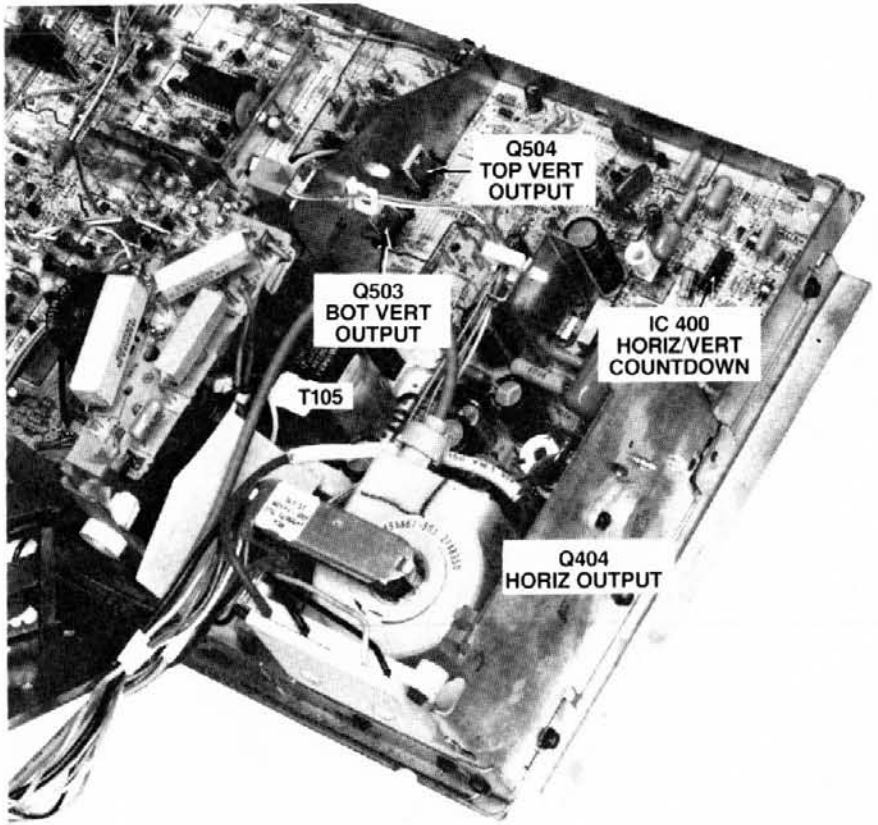
CTC 131/132 Deflection System Overview

The deflection system found in the CTC 131/132 television receiver is very similar to the systems used in previous RCA receivers. The deflection integrated circuit is identical to the type utilized in the CTC 126 13-inch portable color television receiver. The signals utilized for the horizontal and vertical scan systems are derived from a single oscillator found within integrated circuit, U400. The master oscillator within IC U400, operating at 8 times horizontal, is divided down by 8 and passed to the horizontal amplifier circuitry of the integrated circuit. Also, the oscillator signal is divided down by a variable countdown circuit and applied through a vertical amplifier to the vertical deflection system of the chassis.

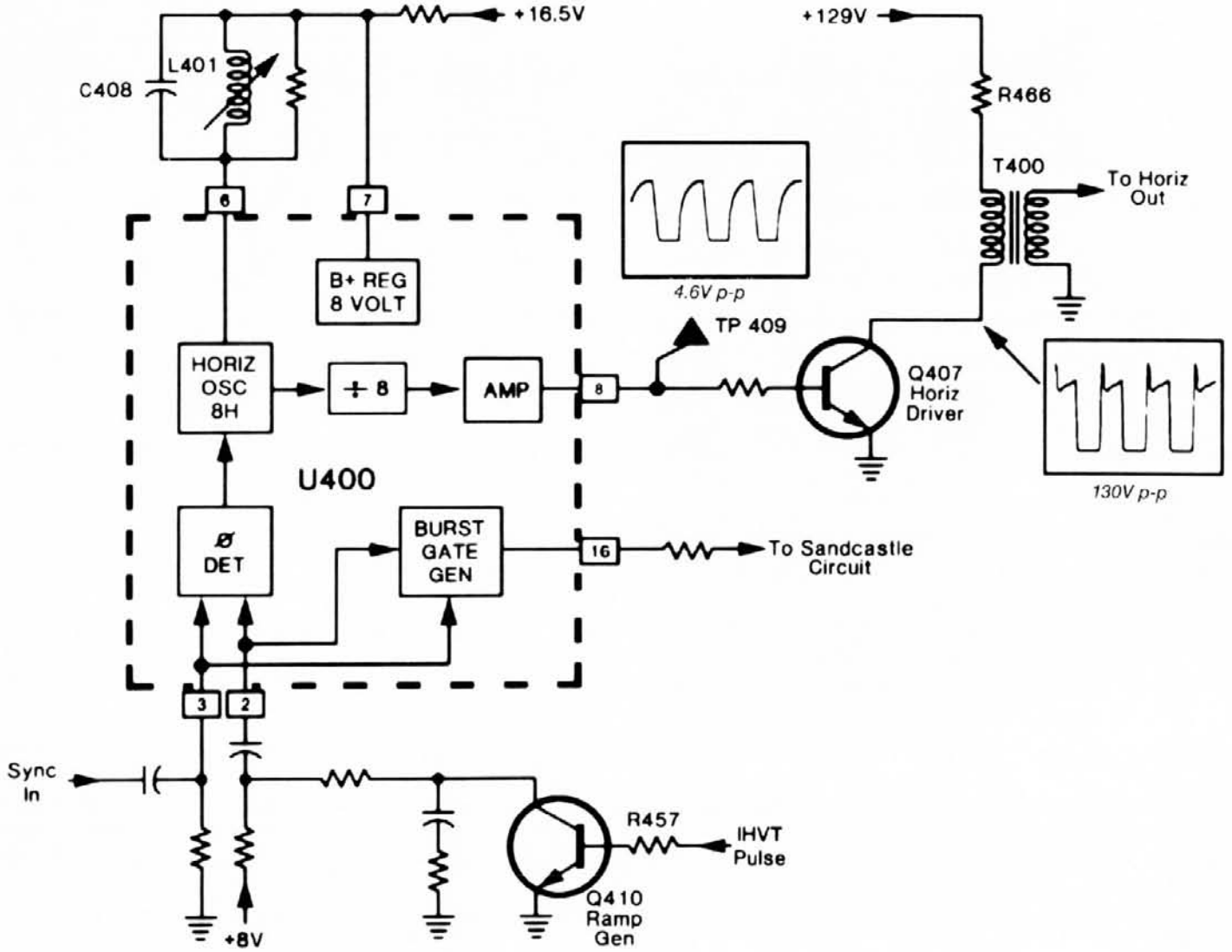
Since the frequency of the signal for the horizontal and vertical systems are derived from the same oscillator, one frequency adjustment control is required in the system for the 8 times horizontal oscillator. Horizontal AFC operation is performed within IC U400 by comparing the IHVT sample pulse to the externally supplied horizontal sync signal. The correction voltage is applied to the oscillator within the integrated circuit to maintain the frequency at exactly 8 times the horizontal. Also generated from within IC U400 are the composite horizontal and blanking signals required to develop the sandcastle waveform pulse which is utilized by the chroma/luma integrated circuit.

The horizontal output signal from the integrated circuit is amplified by horizontal driver transistor Q407 and transformer coupled to the horizontal output stage, Q404. The horizontal output stage then drives the horizontal yoke and IHVT, T401. Transformer T401 develops multiple output voltages to power circuitry on the chassis; high voltage, screen voltage, focus voltage for the picture tube guns, +230 volts for the kine driver stage and +30 volts for the vertical circuit, tuner and pincushion circuitry.

The vertical sawtooth switch utilized in the CTC 131/132 chassis develops a sawtooth signal from the pulse supplied by U400 and amplified by the vertical output stage to power the vertical yoke. The 16.5-volt B+ power for the deflection integrated circuit is derived from the chopper power supply. The +129 volts is required by the horizontal driver and IHVT system. As mentioned previously, B+ power for the vertical circuit is derived from the scan derived +30 volts and from the chopper output circuit +24-volt supply.



CTC 131 Television Chassis (Right Half)



Simplified Horizontal Oscillator and Driver Circuit

Horizontal Oscillator and Driver Circuit

B+ power for IC U400 is derived through a dropping resistor from the chopper power supply +16.5-volt source. This voltage is applied to pin 7 of the deflection integrated circuit regulated by an internal 8-volt regulator. The horizontal oscillator's frequency is determined by the LC resonant circuit connected from pin 6 to the 8-volt B+ source (pin 7). IC U400 internally divides the oscillator signal down to the proper frequency of 15,734 Hz for the horizontal deflection system. Horizontal AFC is achieved by comparing the horizontal sync signal applied at pin 3 to the sample ramp derived from the horizontal's IHVT sample pulse, generating a correction voltage to the oscillator within the integrated circuit.

The output from the horizontal divider circuitry is amplified by an internal amplifier and output at pin 8 to the base of driver transistor Q407. The drive waveform from the integrated circuit can be monitored at TP 409. Horizontal driver transistor Q407 amplifies the drive signal and transformer couples the signal to the horizontal output stage. B+ power for the horizontal driver transistor is derived through a dropping resistor from the +129-volt source of the chopper power supply. Also contained within IC U400 is a variety of gating circuits, developing the required horizontal blanking pulses and the vertical gate signal utilized in the formation of the sandcastle pulse required by the chroma/luma integrated circuit.

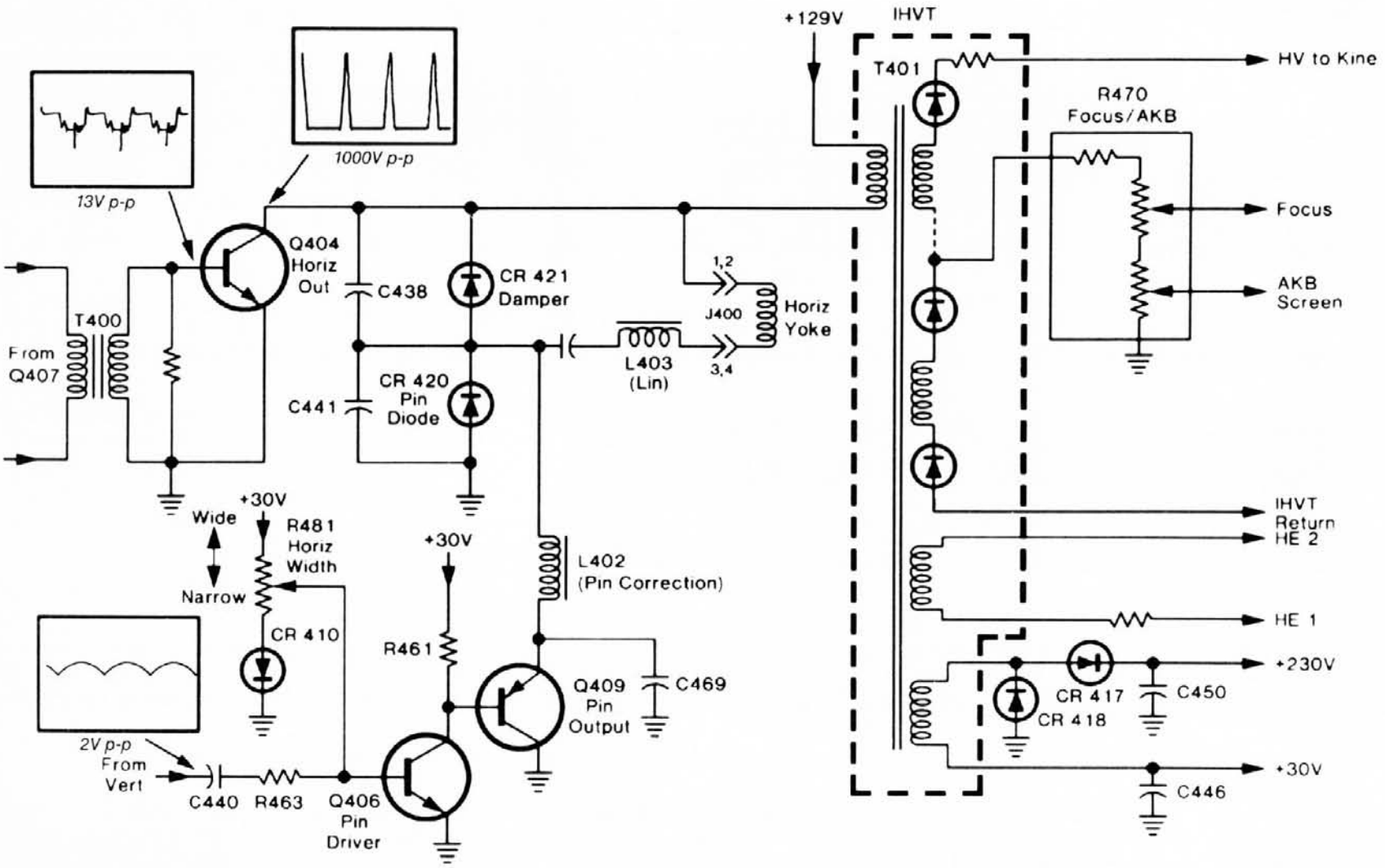
Symptom(s)

Dead Set

Service Procedure(s)

Servicing the horizontal oscillator/driver circuitry in the CTC 131/132 chassis requires applying an external 16.5-volt DC to the cathode of CR 414 (TP 401) during troubleshooting (see page 40 for location of CR 414 or TP 401). Confirm the presence of the proper drive waveform from pin 8 (TP 409) of IC U400. If missing, check the appropriate B+ sources and oscillator circuit of the integrated circuit. If this is found to be correct, suspect IC U400.

If output drive from IC U400 pin 8 is present, confirm the drive waveform on the collector of horizontal driver transistor Q407. If missing, suspect the driver transistor. If present, confirm proper operation of the horizontal output stage.



Simplified Horizontal Output Circuit

Horizontal Output Circuit

The signal from driver stage transistor Q407 is transformer coupled through transformer T400 to the base of horizontal output transistor Q404. The collector output of Q404 drives the primary of IHVT transformer T401 along with the horizontal yoke and retrace network. The horizontal yoke return line is coupled through a linearity network consisting of L403 and a series capacitor to the junction of diodes CR 420 and CR 421. Also connected to the junction of these diodes is the pincushion circuitry through inductor L402. The pincushion inductor is part of a tuning circuit on the return path of the horizontal yoke system. By varying the impedance of this network, the width of the horizontal scan is affected. Transistor Q409, the pincushion output transistor, is utilized to vary the impedance of the pincushion network.

Horizontal width control R481 determines the quiescent operating point of pin driver transistor Q406 and output transistor Q409. A sample vertical parabola signal is input to the base of transistor Q406 through capacitor C440 and R463 modulating the DC bias to the base of Q406. The purpose of this signal is to provide **dynamic** correction to the picture width at a vertical rate.

The secondaries of IHVT T401 develop a variety of outputs that are used to power circuitry within the CTC 131/132 chassis. Within the integral high voltage transformer is a network of six high voltage diodes utilized to develop the high voltage output which is applied to the anode of the picture tube. A reduced portion of the rectified signal is output to the focus/AKB (Automatic Kine Bias) assembly, R470. This control assembly contains a thick film network of dropping resistors and control elements. The control outputs develop the proper range for focus voltage adjustment and additionally the screen control (AKB) voltage. Additional isolated windings develop power for the heaters of the picture tube and to diodes CR 417 and CR 418 for generation of the +230-volt and +30-volt supplies. As mentioned previously, the two B+ sources are utilized to power the kine drivers and vertical output devices along with the tuner and pincushion circuitry. B+ power utilized by the horizontal output stage is derived directly from the +129-volt source of the chopper power supply while the pincushion circuitry requires power from the scan derived +30-volt source.

Symptom(s)

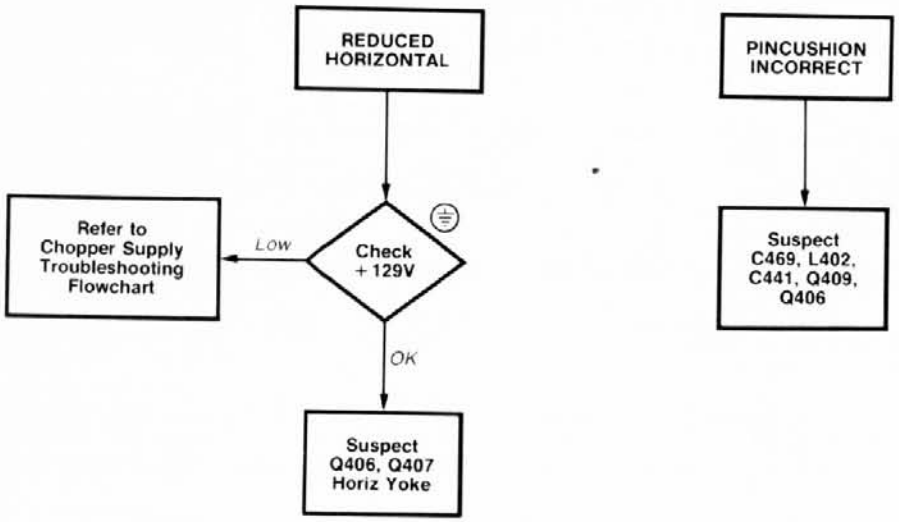
Dead Set

Service Procedure(s)

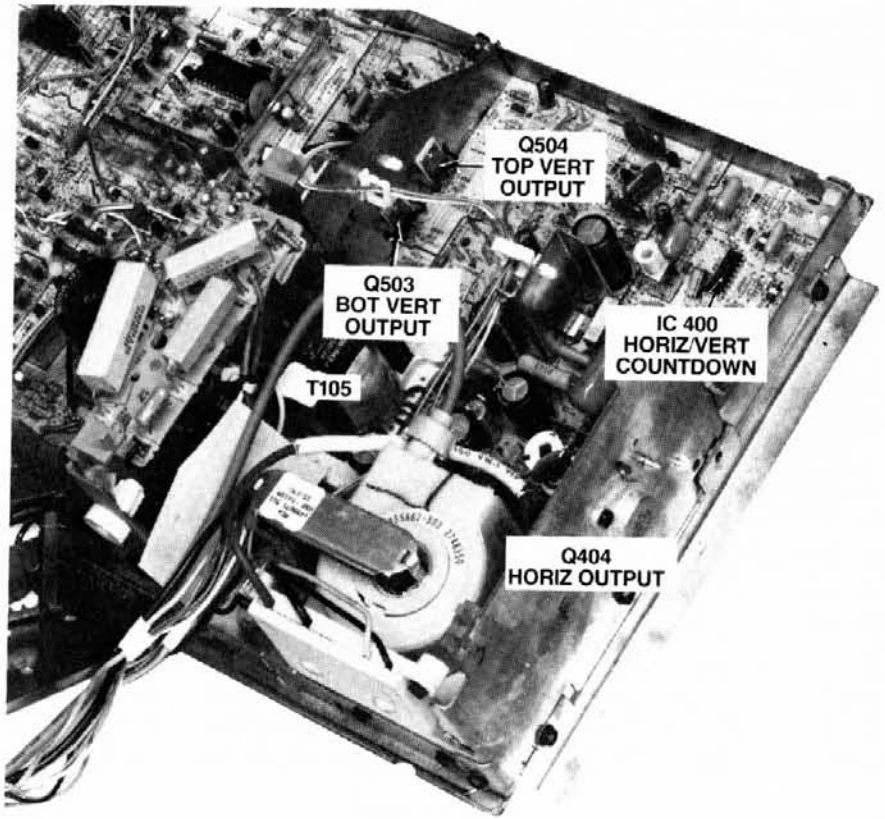
The servicing aspects of the horizontal output system of the CTC 131/132 chassis are very similar to procedures utilized in previous receivers. Unfortunately, as in most cases, any problem associated with the IHVT area generally results in excessive load to the horizontal output stage, which then results in the destruction of the output transistor. Because the horizontal output transistor receives power directly from the chopper power supply, damage to the power supply can also develop compounding the problem of servicing the horizontal output system.

The procedures in this publication dictate that the technician should **confirm proper operation of the horizontal output system** before concerning himself with troubleshooting problems within the chopper power supply. In the event that the horizontal system is malfunctioning, but the overcurrent shutdown of the chopper supply has protected the power supply from damage, it is recommended that during servicing, B+ power for the horizontal output stage be derived from the raw B+ source. Using clipleads, the technician should jumper the raw B+ from the output of the bridge rectifier to the 129-volt output of the chopper supply and also apply an **external 16.5 volts** to power the horizontal oscillator.

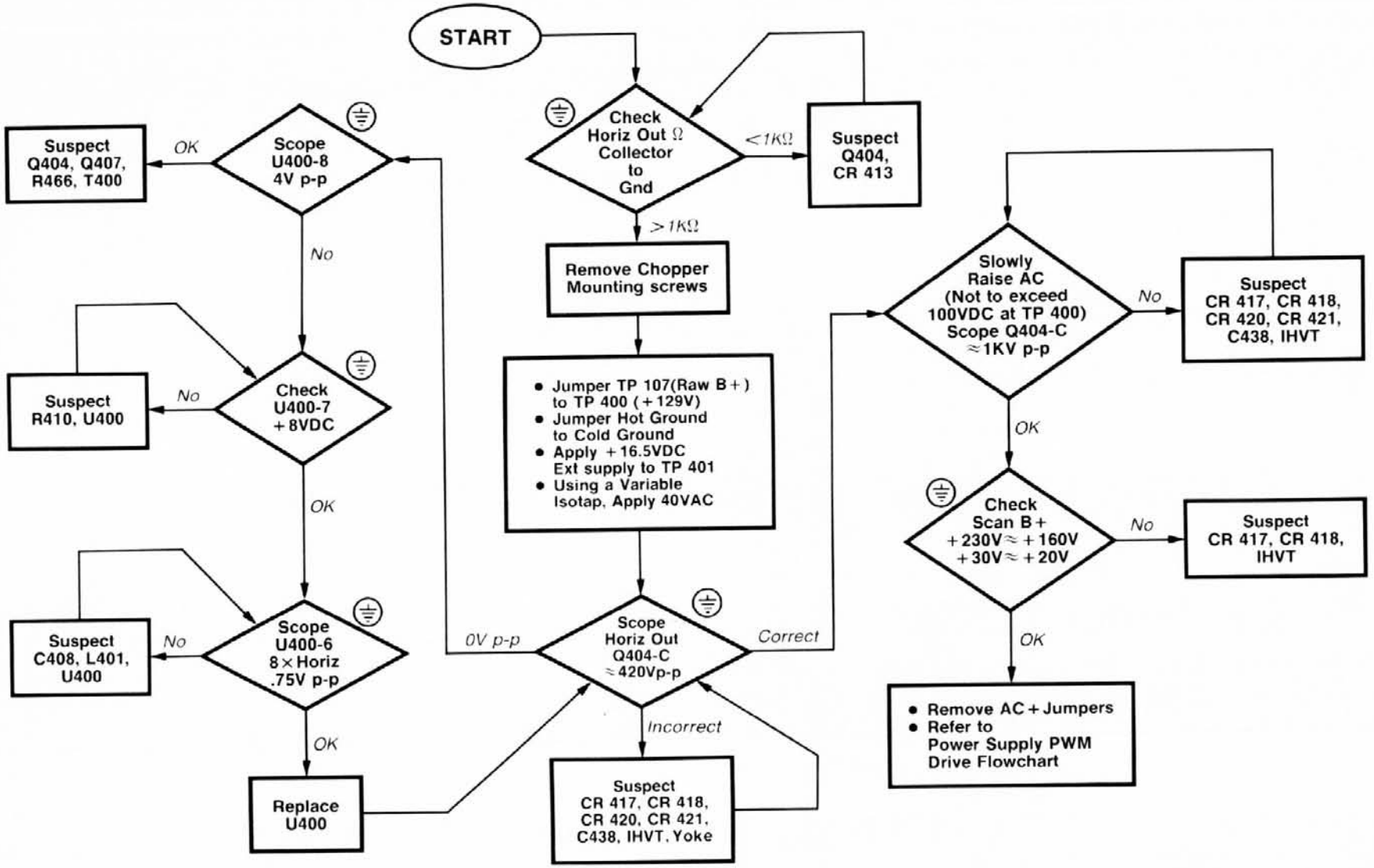
By using the above procedure, troubleshooting the horizontal system can be performed without damaging the chopper power supply. Detailed flowcharts are included at the end of this section concerning these and other procedures in isolating problems within the horizontal output and pincushion areas.



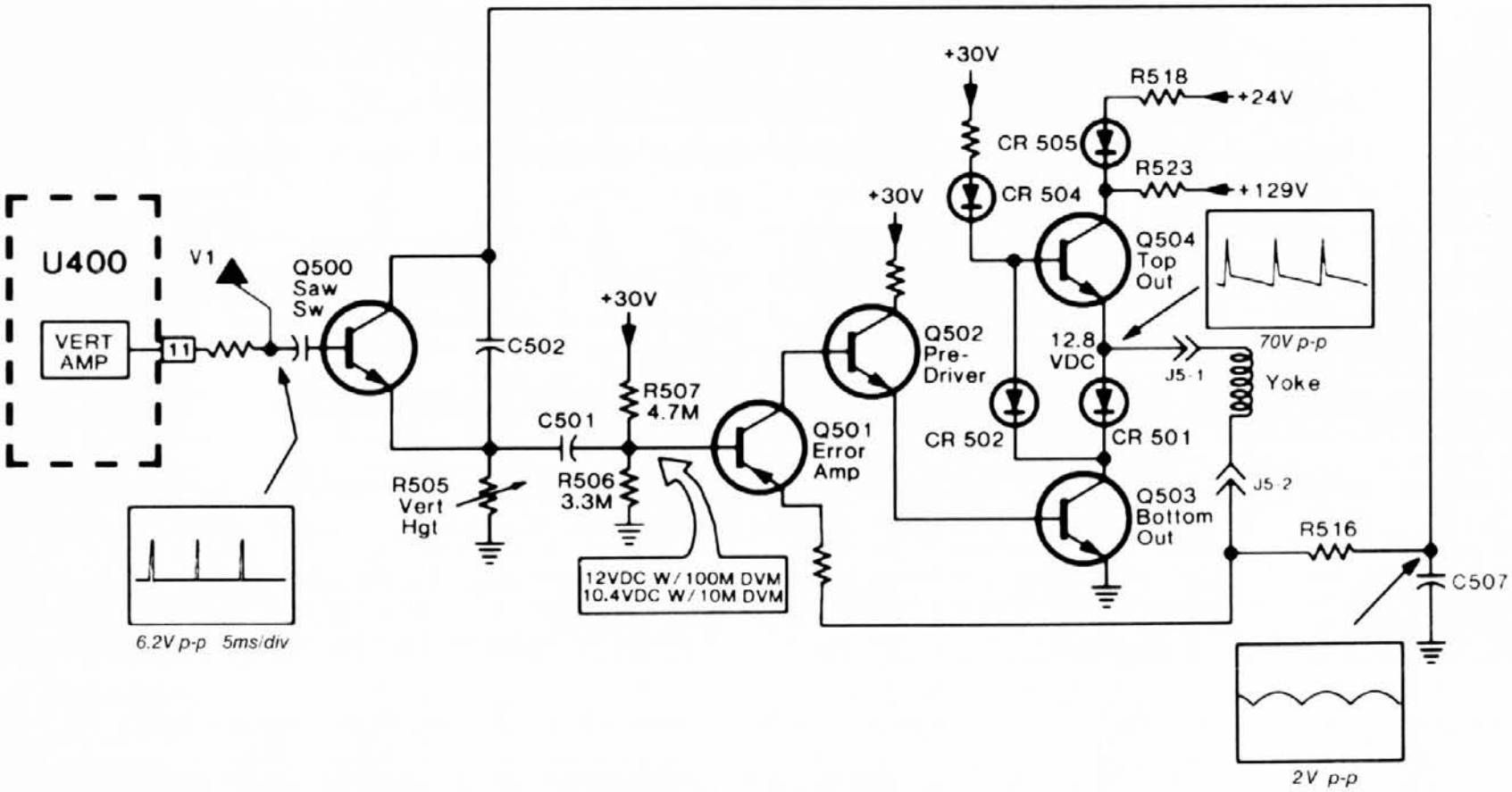
Horizontal Reduced Scan and Incorrect Pincushion Troubleshooting Flowchart



CTC 131 Television Chassis (Right Half)



Horizontal Deflection Troubleshooting Flowchart

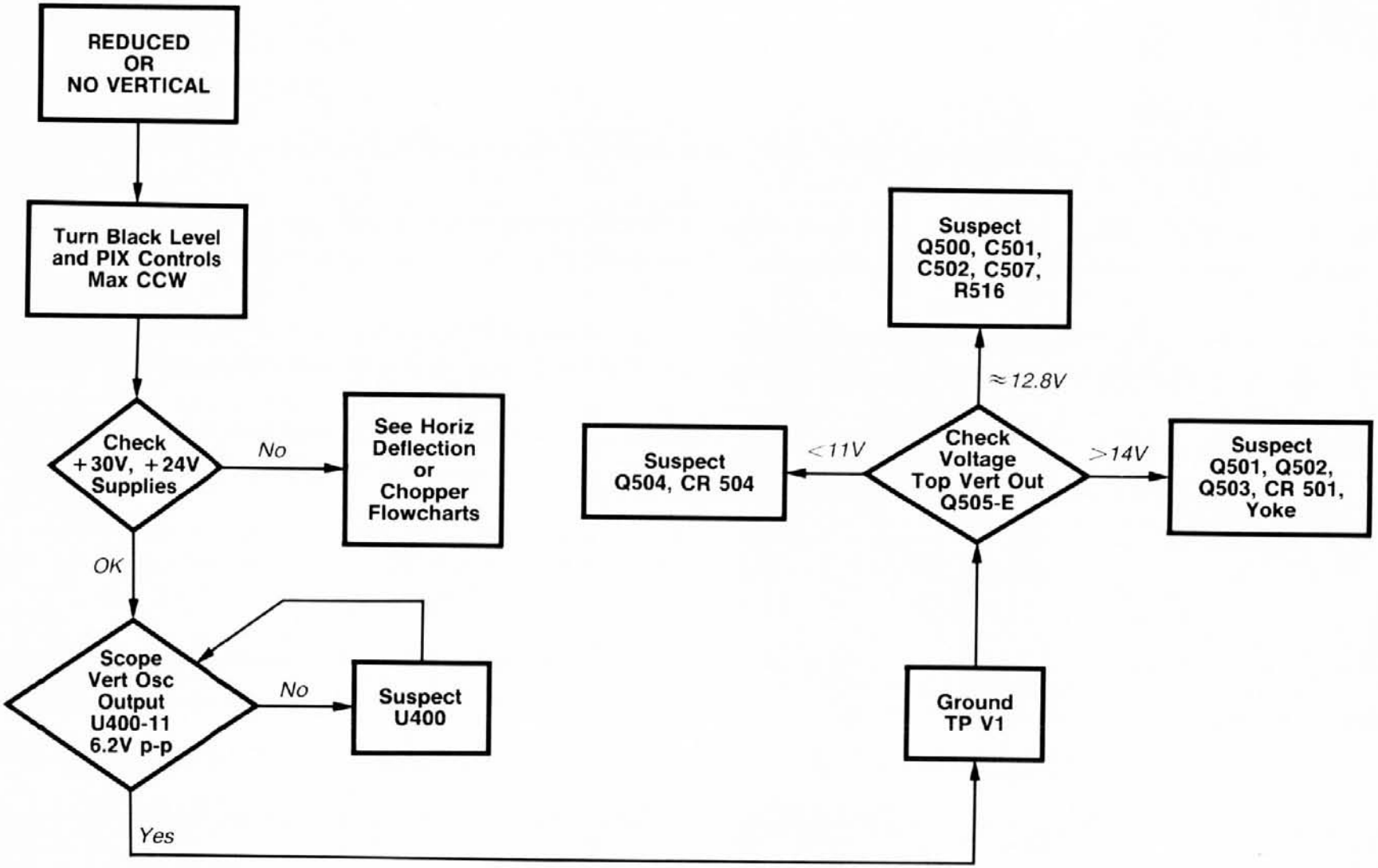


Simplified Vertical Deflection Circuit

Vertical Deflection Circuit

As mentioned previously, the trigger pulse for the vertical output stage is derived from integrated circuit U400, pin 11. When the trigger pulse is applied (through an R/C network) to the base of sawtooth switch Q500, it is in a logic "Lo" state turning "off" Q500. With transistor Q500 turned "off," capacitor C502 is charged through vertical height control R505. The amount of charge is dictated by the B+ present at the junction of the emitter and collector of the vertical output transistors. The current through capacitor C502 develops a sawtooth voltage appearing across R505. This sawtooth signal is capacitively coupled to the base of error amplifier transistor Q501. The base bias for Q501 is derived through two large value resistors, R506 and R507 from the +30-volt source. The divided down bias voltage is theoretically 12.4 volts, but measuring the voltage with a 100-megohm measurement device results in a measurement of approximately 12 volts. If the measurement is performed with a 10-megohm device, the voltage will be approximately 10.4 volts.

Capacitor C502 charges during the period the output at pin 11 of IC U400 is logic "Lo." When the output of the integrated circuit goes logic "Hi," transistor Q500 turns "on" discharging C502 through R516 preparing the capacitor for another charging cycle at the end of the logic "Hi" period. The sawtooth drive signal applied to the base of Q501 is amplified and passed to the base of vertical predriver transistor Q502. Transistor Q502 outputs the drive sawtooth to the base of bottom output transistor Q503. The vertical output stage consisting of transistors Q503 and Q504 along with a grouping of diodes and bias resistors is a circuit very similar to that used in previous chassis. The conduction state of Q503 determines the conduction state at Q504. When the sawtooth varies the conduction state of Q503, the collector current of the transistor also varies the base current to top output transistor Q504. As a result, yoke current is developed through the two output transistors equally. The yoke current is passed to ground through capacitor C507. The vertical parabola appearing across capacitor C507 is the signal that is utilized for pincushion correction by the pincushion circuitry discussed previously.



Reduced or No Vertical Troubleshooting Flowchart

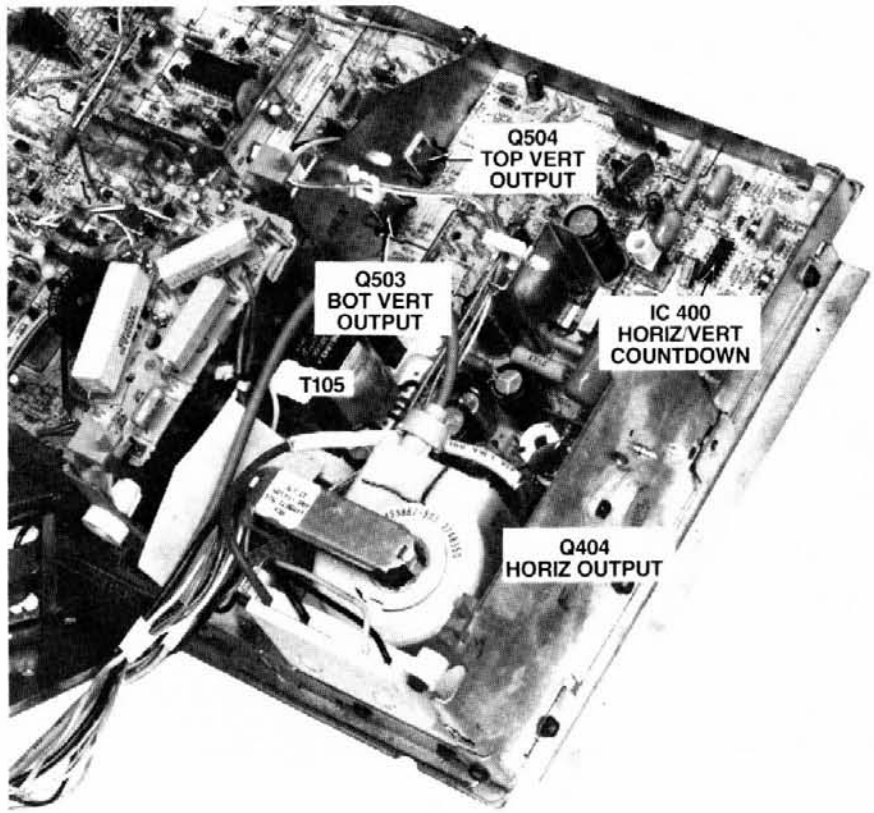
Symptom(s)

Reduced or No Vertical Scan

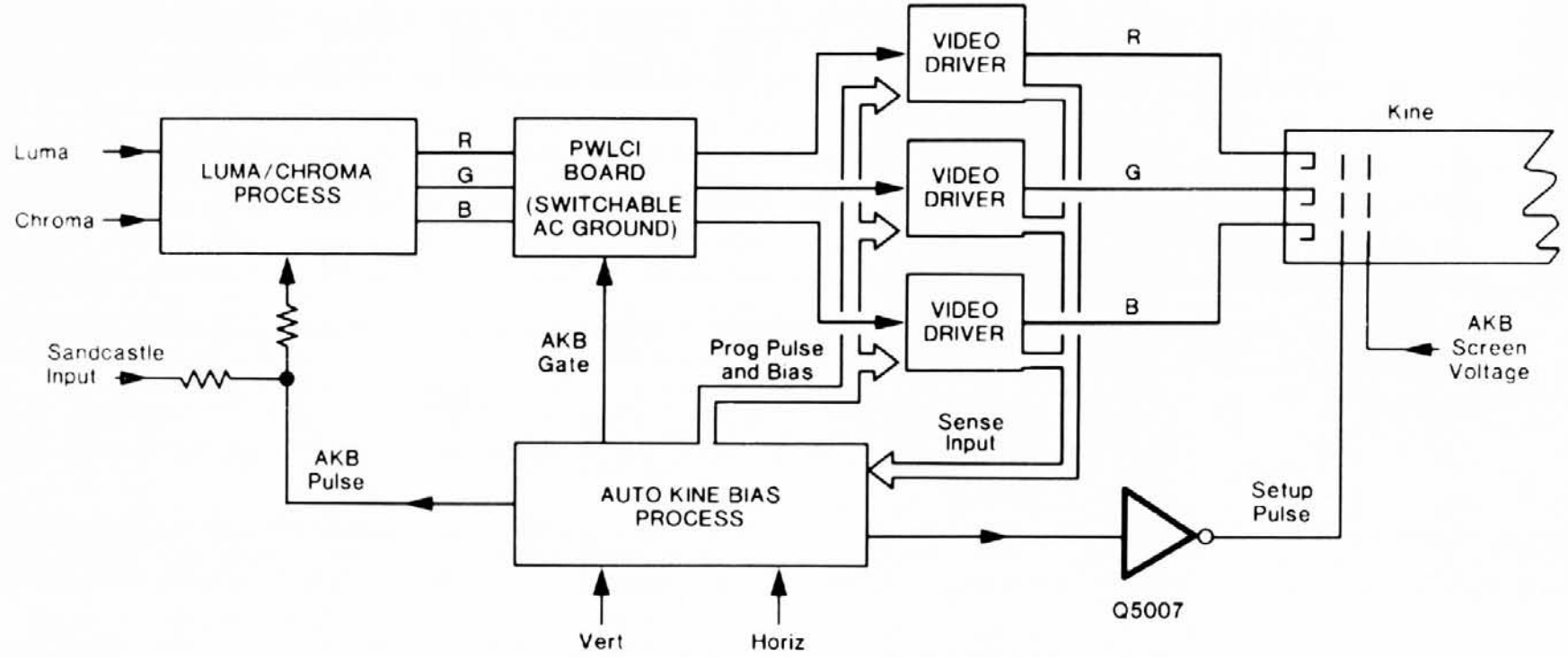
Service Procedure

Servicing the vertical output system in the CTC 131/132 chassis can be accomplished by first confirming for the presence of the vertical pulse at pin 11 of IC U400 or test stake V1. If the vertical pulse is present, DC voltage measurements can then be made to confirm operation of the vertical predriver and output stages. To ensure that the AC portion of the vertical signal does not generate errors in the measurements, test stake V1 should be grounded with a cliplead. A DC voltage measurement should be made in the output stage at the junction of the anode of CR 501 and the emitter of Q504 (connector J5 pin 1). The voltage at J5, pin 1 is approximately 1/2 of the +24-volt source. If this voltage is correct, then suspect a possible defective R516 or C507.

In the instance of insufficient vertical or vertical foldover, the problem is most likely contained within the vertical output or predriver stage. It is a simple matter of checking the vertical output transistors, predriver transistor, or the associated diodes in the vertical output stage. As stated previously, the base of error amplifier transistor Q501 is biased from a very high impedance voltage divider from a +30-volt source. When making the measurement, be aware of the impedance of your meter as it can effect the voltage reading.



CTC 131 Television Chassis (Right Half)



Automatic Kine Bias (AKB) Simplified Block Diagram

Automatic Kine Bias (AKB)

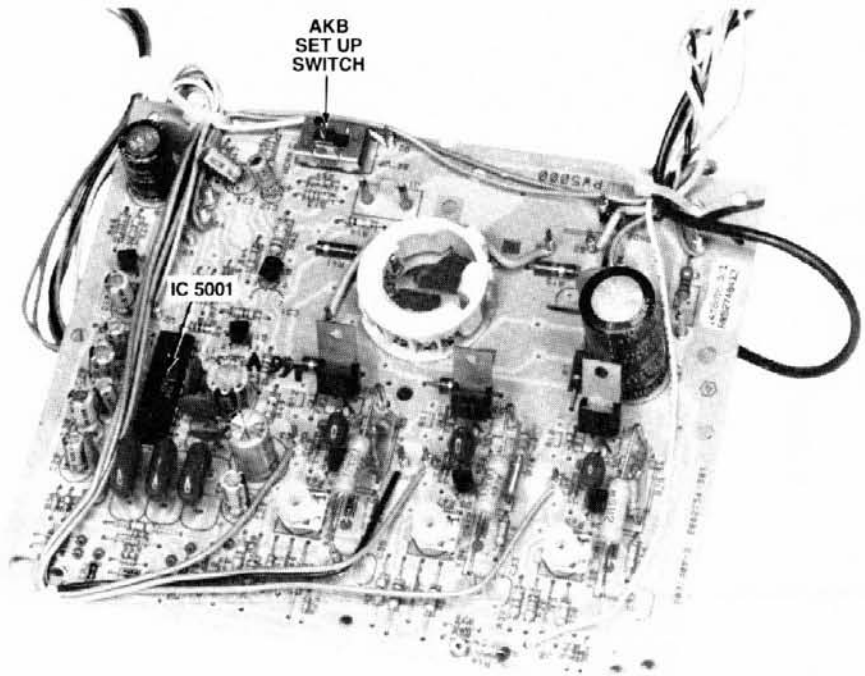
A new circuit found in the CTC 131/132 chassis is the **automatic kine bias** system. This circuit alleviates color temperature drift problems encountered in previous receivers which normally occur during the life of the picture tube. A dynamic circuit is utilized to monitor the cathode current of the three guns in the picture tube, correcting the DC bias of the video driver stage to maintain the proper gray scale (color balance) of the picture. The automatic kine bias circuitry monitors various gating signals within the video driver circuitry during a test period called the **AKB process period.** The AKB process period occurs during 7 horizontal scan lines just **after vertical blanking.** By reducing the vertical height of the receiver, the AKB period can easily be seen at the top of the screen. The AKB process circuitry requires vertical and horizontal pulses from the countdown integrated circuit to properly time its operation.

During the AKB period, the automatic kine bias circuitry generates a variety of control pulses to set up the video output stage to a known state. A grid pulse, referred to as a setup pulse, is applied to the picture tube grid from transistor Q7. At the same time, the AKB pulse and AKB gate are applied to the luminance/chrominance process circuitry and the luminance/chrominance interface board (PWLCI) respectively. These pulses, output from the AKB process circuitry, are utilized to set up the inputs of the video driver stage during the measurement period, which determines the cathode current emission of the picture tube guns. Again, this AKB period occurs only **during 7 horizontal lines at the beginning of vertical scan.** Otherwise, the luma/chroma process, luma/chroma interface (PWLCI circuit board), and video drivers operate normally.

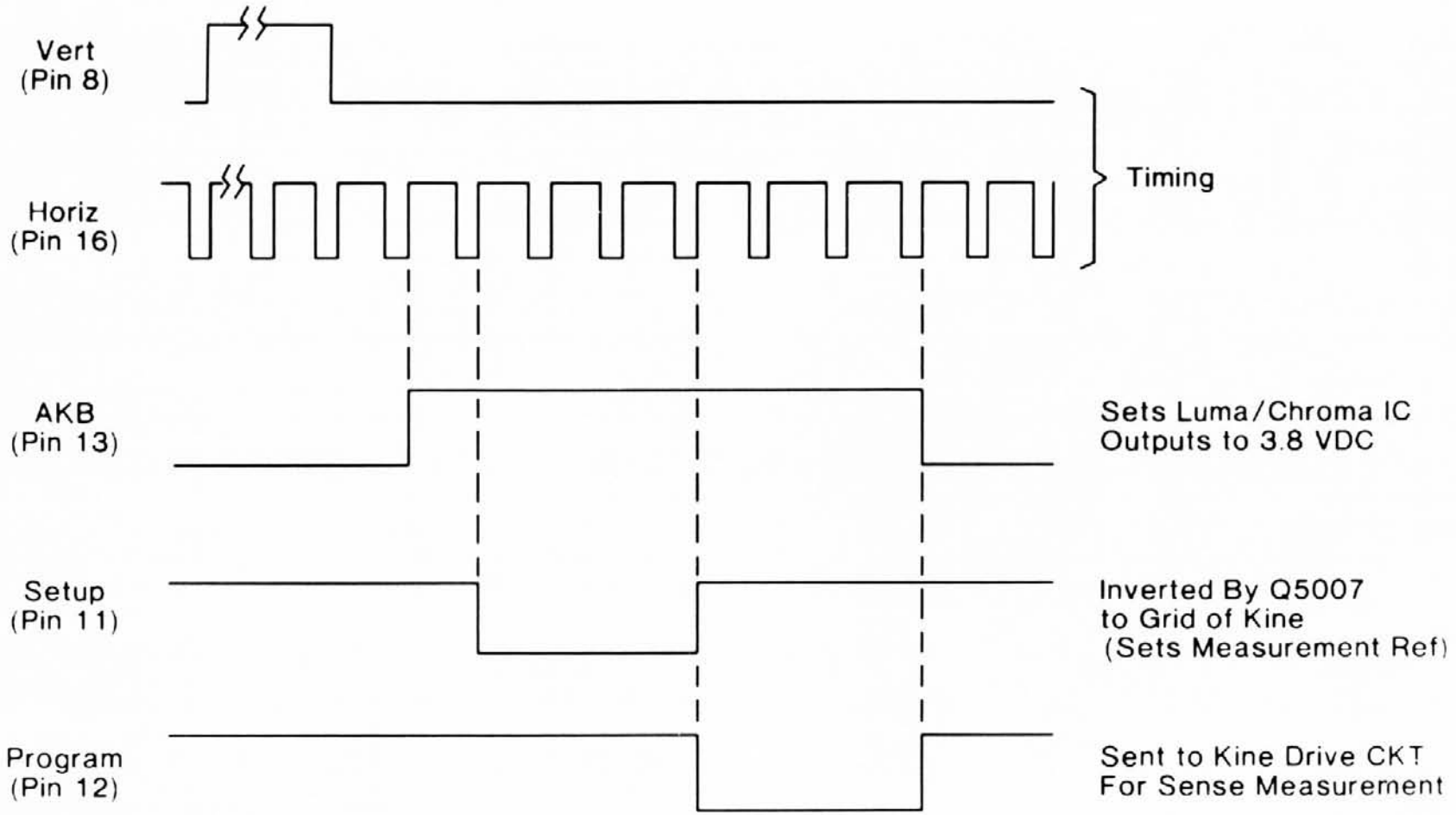
Unique for this type of circuit is the elimination of three separate screen controls. Only one screen control (AKB) is utilized to adjust the screen potential to all three guns simultaneously.

AKB Setup

The procedure to properly set up the gray scale or the receiver is to place the setup switch (on the kine drive board) into the setup position and adjust the AKB control (found on the rear of the IHVT transformer) until one color just barely becomes visible on the screen. Then place the setup switch to the normal position and the automatic kine bias circuitry dynamically corrects the drive bias to the video driver stages adjusting the conduction currents of the picture tube guns maintaining the proper gray scale. This correction system is updated 60 times a second (or every vertical field). The result of this system is the user now has optimum gray scale of the picture information over the normal life of the picture tube without being concerned with variations in the emission of the guns.



Auto Kine Bias/Video Driver Board (PW 5000)

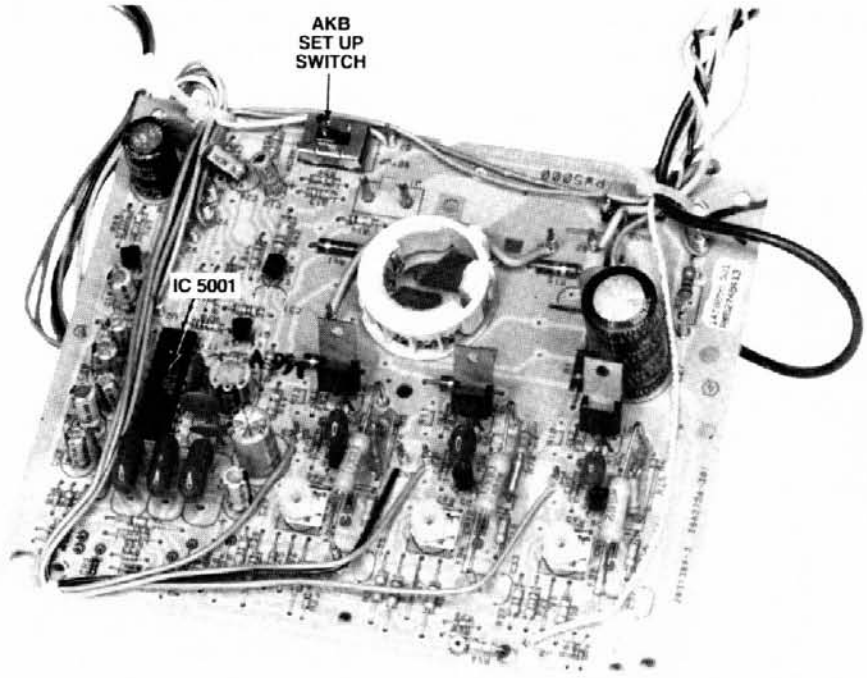

Vert
(Pin 8)
Horiz
(Pin 16)
Timing
AKB
(Pin 13)
Sets Luma/Chroma IC
Outputs to 3.8 VDC
Setup
(Pin 11)
Inverted By Q5007
to Grid of Kine
(Sets Measurement Ref)
Program
(Pin 12)
Sent to Kine Drive CKT
For Sense Measurement

AKB Timing

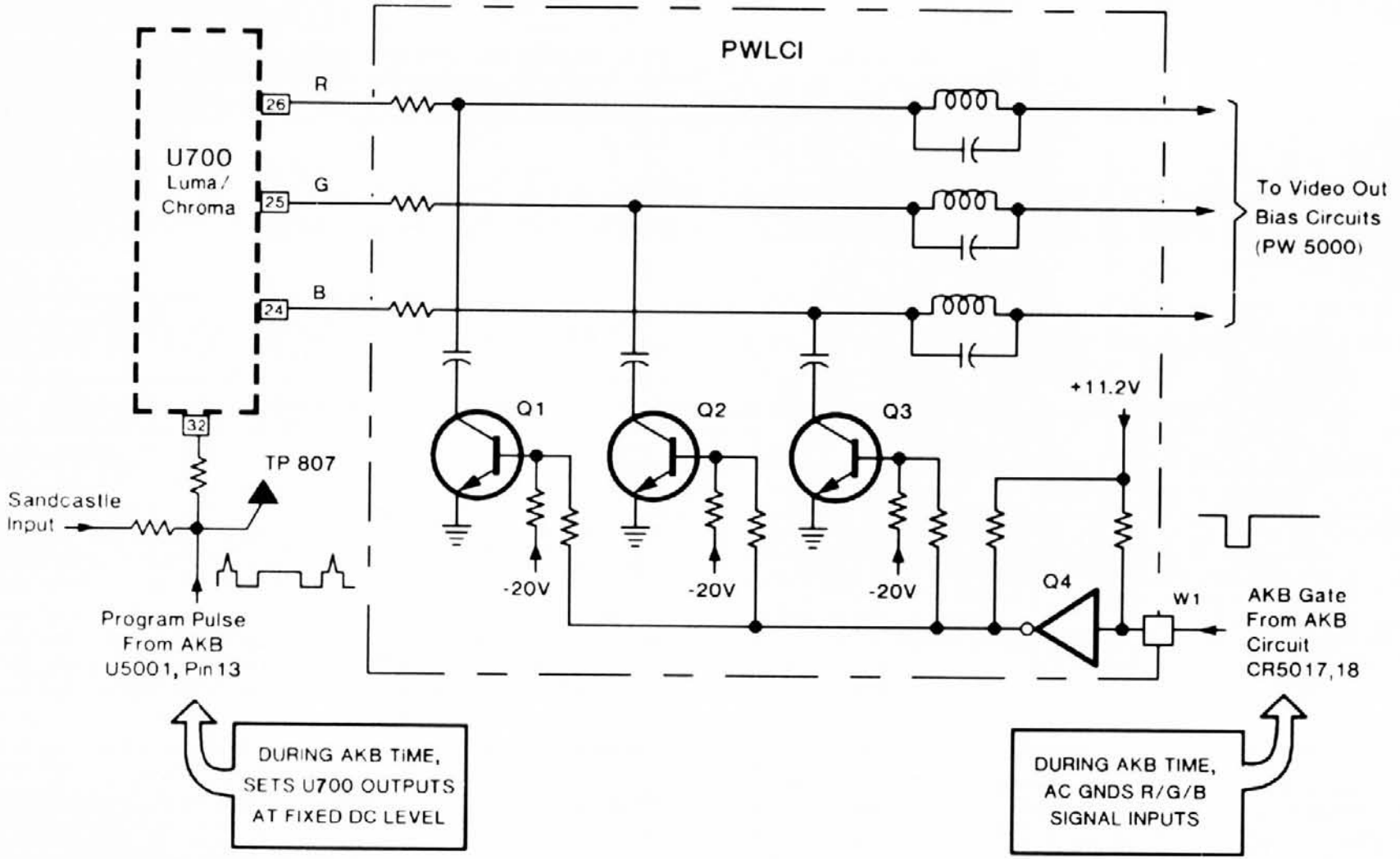
AKB Timing

As mentioned previously, the AKB period utilized for the automatic kine bias processing is accomplished **within 7 horizontal lines** at the **beginning** of vertical scan. The vertical and horizontal pulses from the deflection countdown integrated circuit are utilized by the AKB process system to time its operation. Referring to the timing chart, at the end of vertical blanking, pin 13 of the AKB IC develops a positive pulse lasting the complete AKB period. This output pulse is passed to the chroma/luma integrated circuit instructing the IC to **fix the R/G/B outputs** at a **3.8-volt DC level** during the AKB period. Utilizing an oscilloscope **synchronized** at the **vertical rate** the technician can observe this AKB pulse and its effect on the output of the chroma/luma IC's R/G/B outputs.

The setup pulse from pin 11 of the automatic kine bias integrated circuit occurs one horizontal line after the start of the AKB period. The setup pulse is passed to transistor Q5007, inverted and applied to the grid of the kine gun. This pulse sets the **reference point** utilized for the AKB period to make the proper measurement. The program pulse from pin 12 of the automatic kine bias circuit is developed approximately **4 horizontal lines** after the start of the AKB period or the end of the setup period. The program pulse, referred to as the sense period, has a duration of 3 horizontal lines. During this period of time, the pulse is sent to the kine drive circuitry and a measurement is taken to determine the conduction state of the three guns.



Auto Kine Bias/Video Driver Board (PW 5000)



AKB Period Input Reference

AKB Period-Input Reference

In order for the AKB processing system to properly adjust the video driver bias, the input signal from the chassis to the kine drive circuitry must be fixed at a predetermined DC value and have complete removal of any AC component. As a result, **two control pulses** are derived from the AKB process circuitry to generate this condition.

The output from pin 13 of the AKB IC U5001 is applied to the sandcastle network input, pin 32 of luma/chroma IC U700. During normal operation of the receiver, sandcastle waveforms are present at the input pin 32 of the chroma/luma IC. During the 7 horizontal lines of the AKB process period, just after vertical sync, the signal from the AKB integrated circuit, pin 13, is applied through the sandcastle network to the input at pin 32. This input **overrides the sandcastle** pulses and fixes the input voltage at pin 32 to a predetermined DC state. This input DC condition forces the chroma/luma integrated circuit to remove AC signals and fix the output voltage of the R/G/B outputs at pins 24, 25, and 26 to a fixed DC level of 3.8-volts DC. The R/G/B outputs of the luma/chroma IC are routed through an interface circuit board assembly (PWLCI), which is then passed to the bias circuits of the video outputs on the PW 5000 board.

Since it is imperative that this signal from the chroma/luma integrated circuit be pure DC with no AC component, transistors Q1, Q2, Q3 and Q4 on the PWLCI board are utilized to AC ground these three R/G/B lines from the luma/chroma system during the AKB period. After the AKB period, these devices are turned "off" allowing proper passage of the R/G/B signals to the kine circuitry.

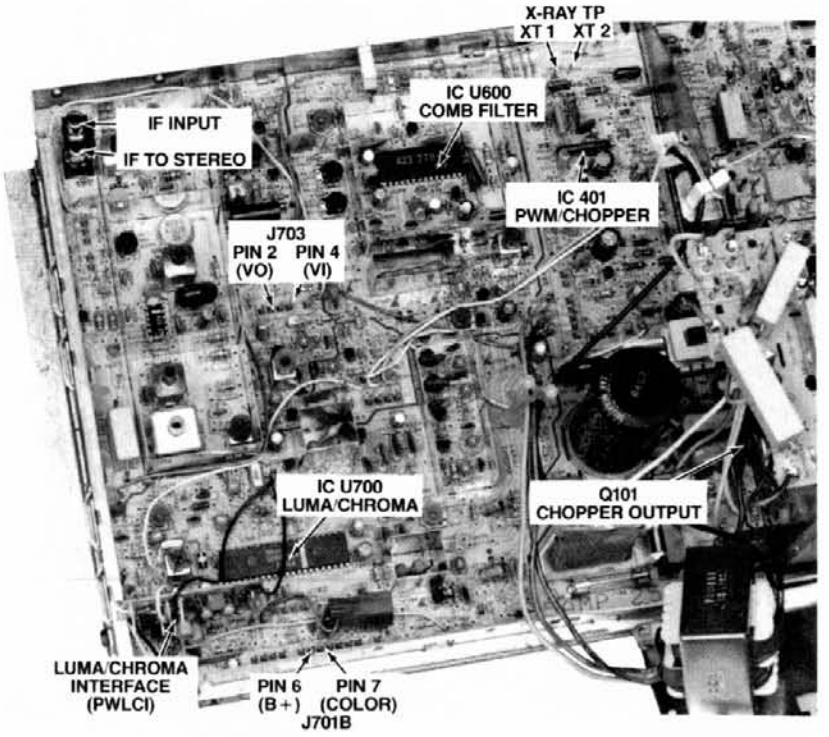
Symptom(s)

Dark Picture

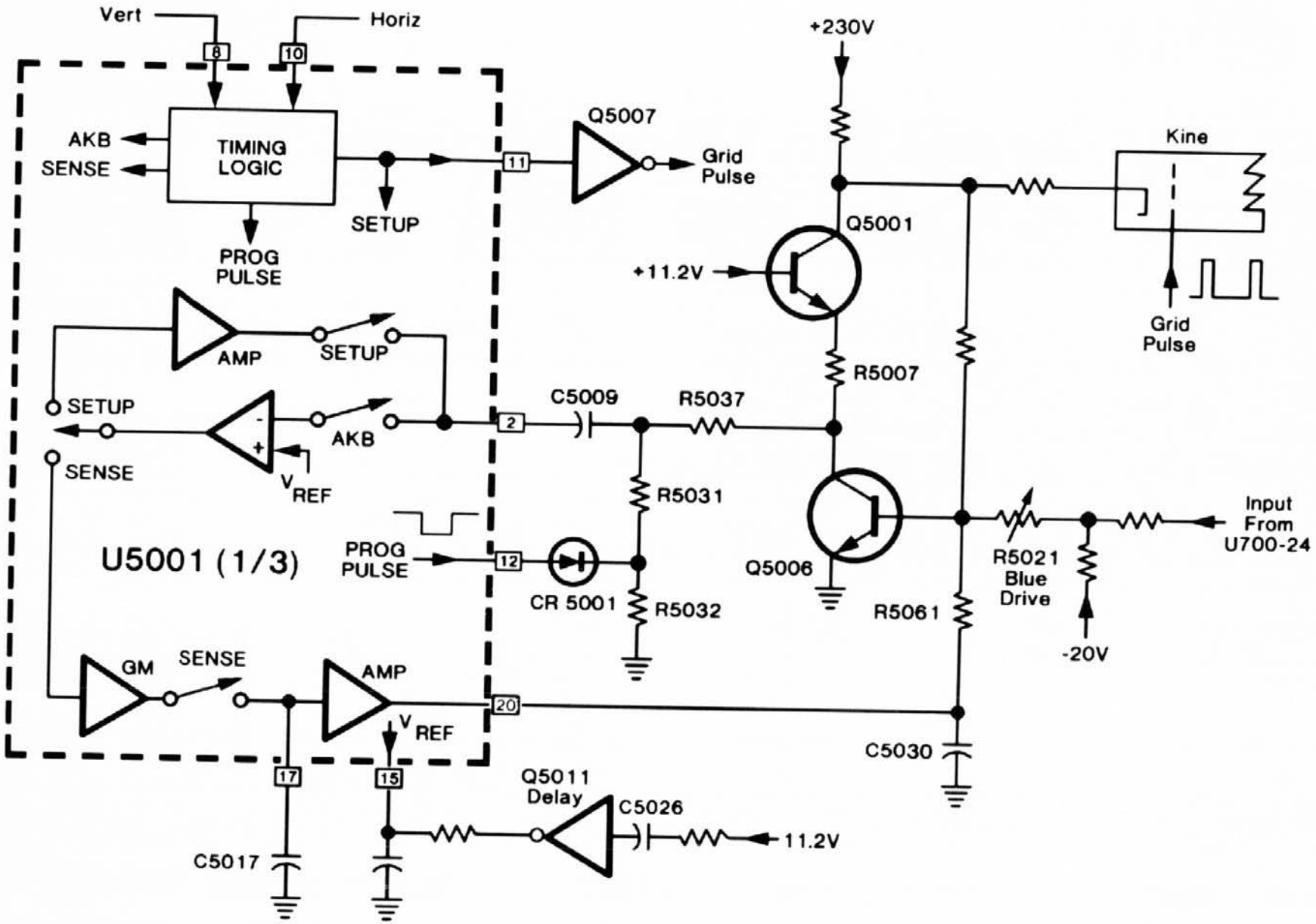
Loss of One Color

Service Procedure(s)

During servicing of problems concerning luminance information, the technician should always confirm proper operation of the AKB circuitry. Monitoring TP 807 for the proper sandcastle waveform is required, but also synchronizing the oscilloscope at a vertical rate to look at the AKB pulse during the 7 horizontal lines following vertical blanking. Also, the output of the luma/chroma integrated circuit develops a DC output level of 3.8 volts during this AKB period at the three R/G/B outputs. Problems can exist with the AC grounding transistors on the PWLCI board if they do not turn "off" when required. As a result, symptoms such as insufficient luminance, no chroma information, and loss of one or two colors can be caused by a defect within the PWLCI circuit board. Servicing flowcharts are included at the end of this section for servicing problems in the AKB/kine driver area.



CTC 131 Television Chassis (Left Half)



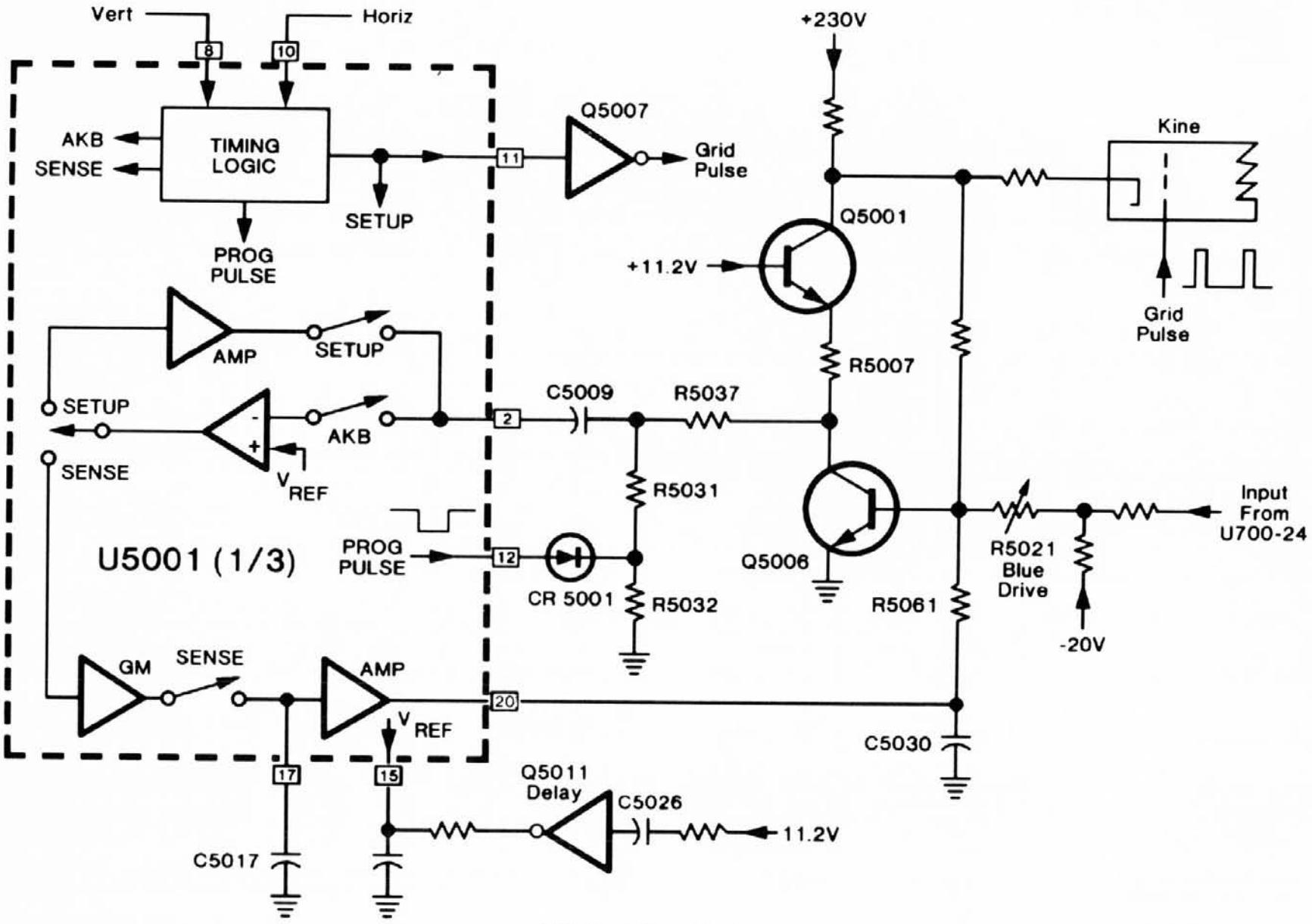
AKB Operation (Blue)

AKB Operation (Blue)

The AKB processing is synchronized by the vertical and horizontal pulses from the countdown integrated circuit, applied to pins 8 and 10 of IC U5001. The timing logic within the AKB integrated circuit develops a variety of pulses to control AKB operation. The setup pulse is output through pin 11 to transistor Q5007, amplified, and applied to the grids of the kine. Within IC U5001, a variety of pulses are generated to control solid-state switches within the IC. These switches control the operation of various amplifier stages. Integrated circuit U5001 contains three identical sample circuits that perform the measurement of the cathode current on each gun. Since each area is identical, only the blue channel is discussed. Internally IC U5001 develops a reference voltage. The reference voltage is filtered by the capacitor present at pin 15 to ground. Attached to this filter is a delay transistor network utilizing transistor Q11. The input of Q11 is coupled through an R/C time constant to the 11.2-volt source. This delay network eliminates rapid start up of the AKB processing during picture tube warm up. This is evident by the characteristic of the receiver at turn "on" coming up with luminance and video at a slow rate.

If this circuit is defective, the picture comes on very bright and then reduces to a nominal brightness level. This symptom occurs because the AKB processing circuitry immediately senses low cathode current setting the bias on the guns to minimum. As a result, when the cathode current becomes activated the bias to those guns is so small that the guns conduct heavily until the AKB process system has the time reduce the cathode current or the bias to the output circuitry. If C26 is leaky, the instrument delays too long before coming up. If C26 or Q11 is shorted, then the instrument will not come up. C26 being leaky is the most common mode of failure.

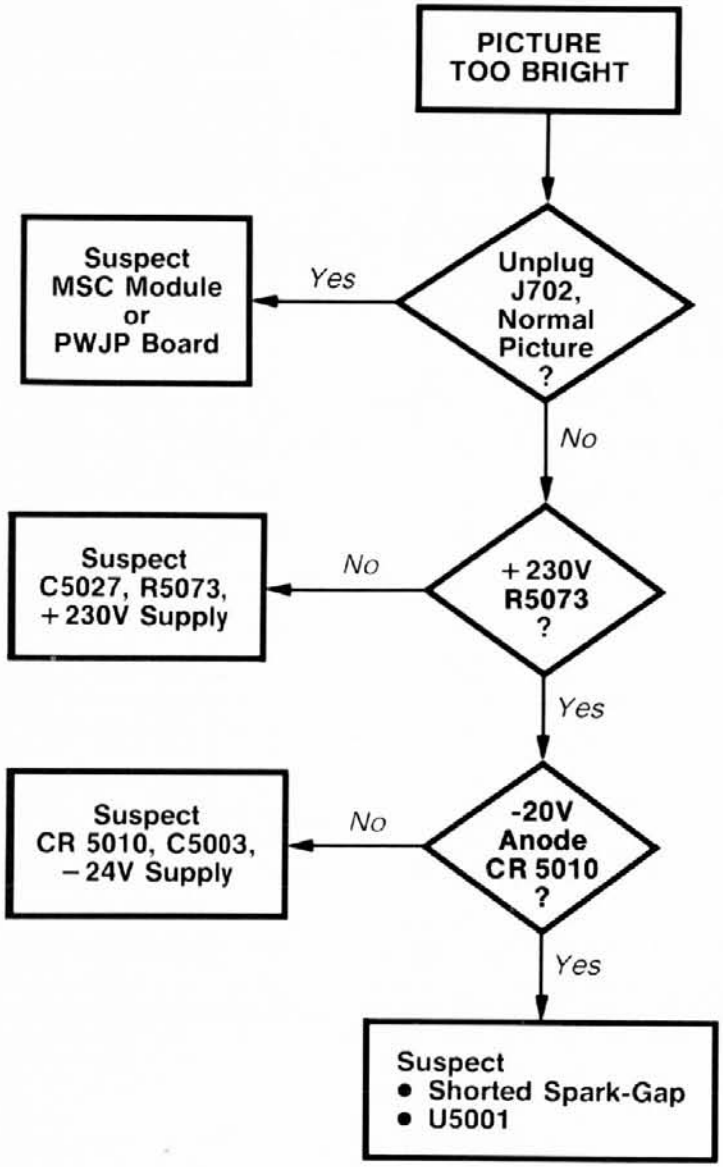
The internal reference voltage is utilized by an internal comparator inside IC U5001 for the measurement of the sense signals from the driver circuitry. During the initial start of the AKB period, a setup pulse is generated closing a variety of switches within the IC U5001 circuitry. This setup period also develops the grid pulse to cause the guns of the picture tube to conduct. The cathode current of the picture tube develops cathode current which is passed through driver transistors Q5001, Q5006, and resistor R5007. With an increase in cathode current, as a result of the grid pulse, the voltage at the collector of Q5006 goes "Lo." At the same time, internal to IC U5001, a variety of switches close causing the internal comparator to route its output through an amplifier back to its inverting input. In this mode of operation, the voltage at pin 2 of IC U5001 reverts to the same voltage as the internal reference voltage. During this period, a charge develops across capacitor C5009 in preparation for the sense period. At the end of the setup period, the sense period occurs. The internal logic timing generates a sense pulse which switches the output of the comparator to a transconductance amplifier within the integrated circuit. Also during the sense period, the program pulse is output at pin 12 through diode CR 5001. The output of pin 12 is normally "Hi" and goes logic "Lo" during the sense period causing diode CR 5001 to turn "off." The output of the transconductance amplifier is routed through a sense mode switch, charging capacitor C5017 at pin 17. The voltage across C5017 is internally amplified and output at pin 20.



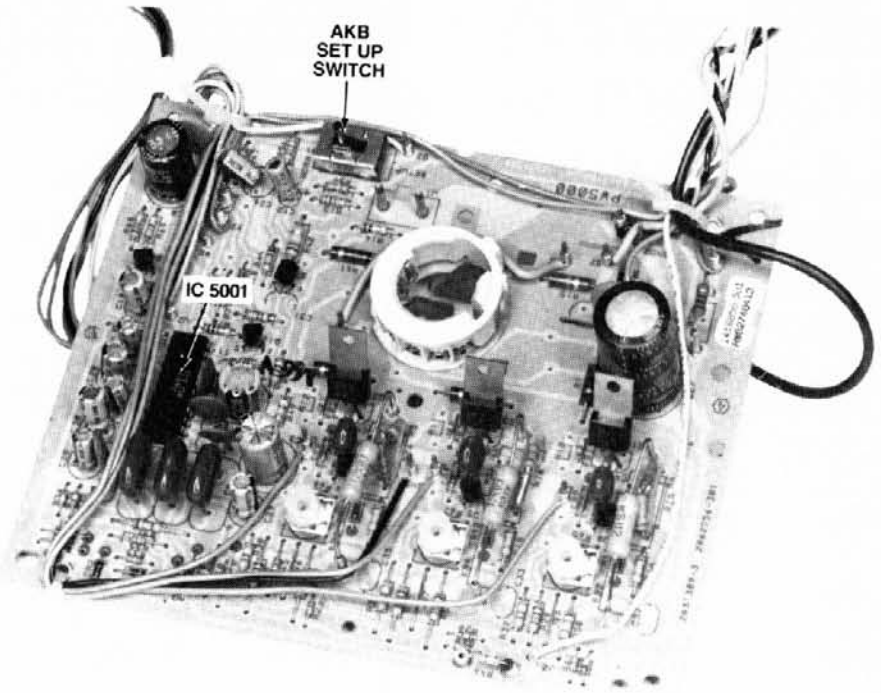
AKB Operation (Blue)

The correction for proper bias is determined by the charging or discharging action of capacitor C5009 during the period the setup pulse terminates and the sense period starts. At this time, the collector of Q5006, which is held at a "Lo" state during the setup period, is now reverted back to it nominal level during the sense period. The change in voltage develops a current through resistor R5037 applied to the end of capacitor C5009. At the same time, the generation of the sense pulse at the output pin 12 of IC U5001 reverts to logic "Lo," turning "off" diode CR 5001. The resultant current generated by the voltage divider of R5031 and R5037 develops a charging or discharging current to capacitor C5009. During the sense period, if there is **no change** in the charge in capacitor C5009, then **no correction** is generated at the output, pin 20 of the IC U5001. If the cathode current of the gun is too high, the voltage change at the collector of Q5006 is larger than normal. As a result, a charging current is applied to capacitor C5009, increasing the voltage at the inverting input of the comparator. Then the output of the comparator goes "Lo" causing the transconductance amplifier (GM) reducing the charge on capacitor C5017 and the output voltage at pin 20. The corrective action of the output voltage changes the bias on the base of Q5006, reducing the bias to the picture tube, maintaining the correct cathode current current. Conversely, if the cathode current of the gun is lower than normal, the change in voltage at the collector of Q5006 develops a discharging current in capacitor C5009 resulting in the voltage at pin 2 of IC U5001 becoming less positive. The output of the comparator then increases causing the transconductance amplifier to increase the charge to capacitor C5017. The higher voltage across C5017 is amplified within IC U5001 and output at pin 20. This increases the bias voltage to Q5006, developing more collector current, reducing the picture tube cathode voltage. The sequence of events just discussed is accomplished at a 60-Hz rate.

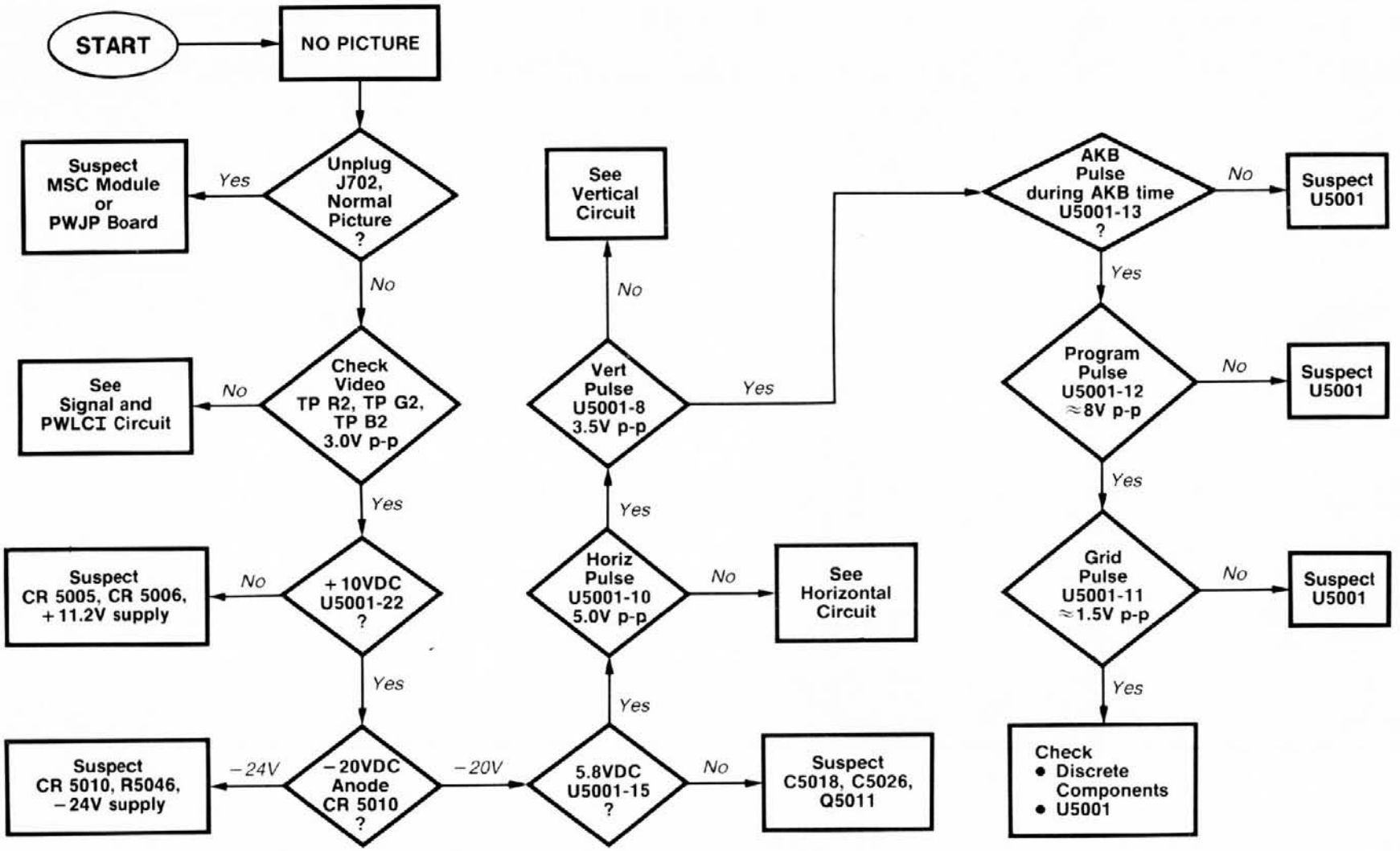
The chroma/luma information is applied through a resistor bias network from IC U700, pin 24, through blue drive control R5021 to the base of Q5006. The input signal and correction voltage from the AKB circuitry is applied to the base of Q5006 along with a −20-volt bias current. The DC bias voltage of the picture tube cathodes is adjusted during every vertical field to maintain proper color temperature. In the event a loss of one of the signals occurs, the automatic kine bias circuitry tries to compensate for this by changing the bias voltage to maintain the same cathode current in the picture tube guns. Flowcharts are contained in this publication to isolate problems in the kine bias/AKB circuitry found in the CTC 131/132 receiver.



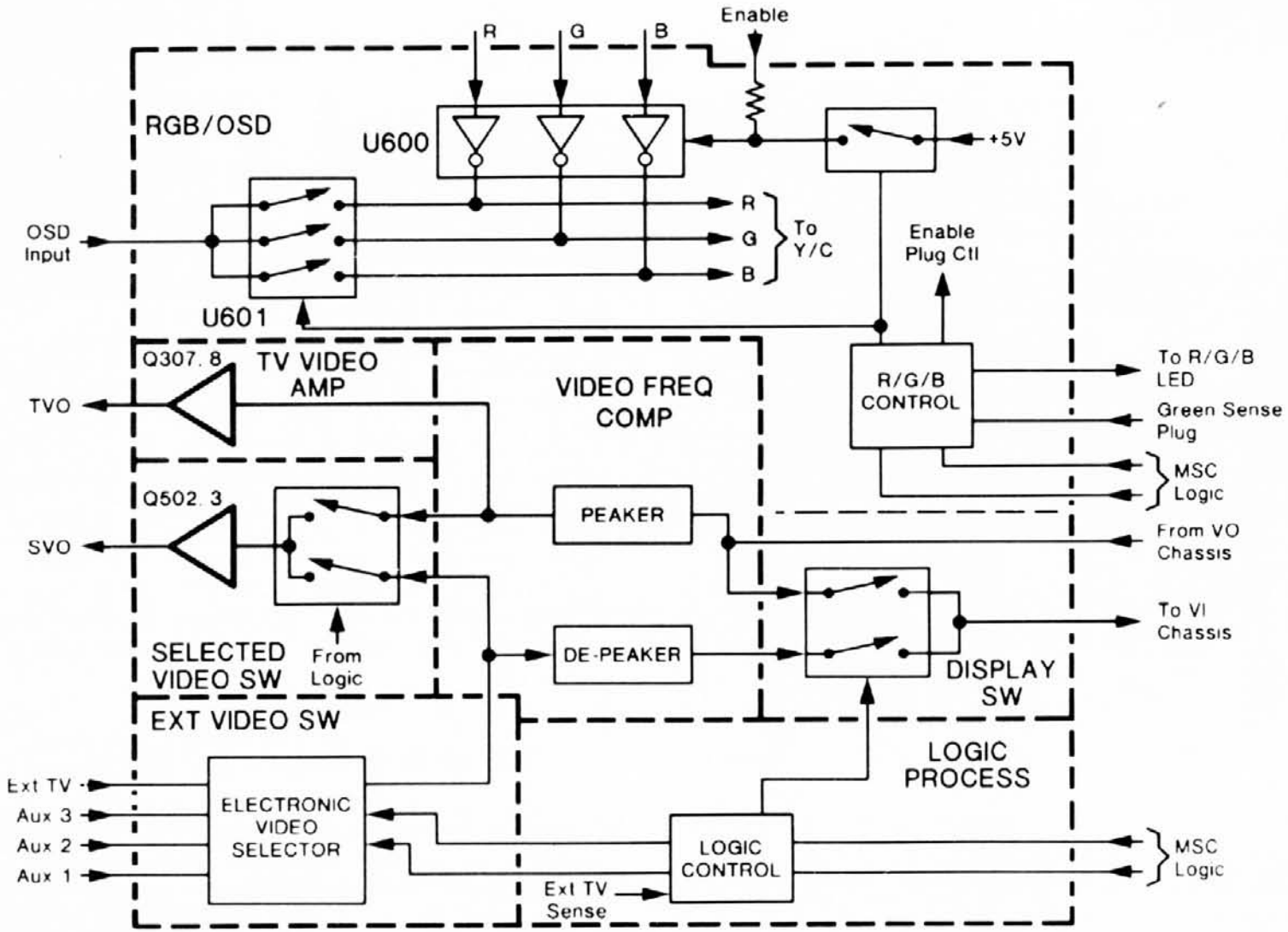
AKB Flowchart—Bright Picture



Auto Kine Bias/Video Driver Board (PW 5000)



AKB Flowchart—Dark Picture



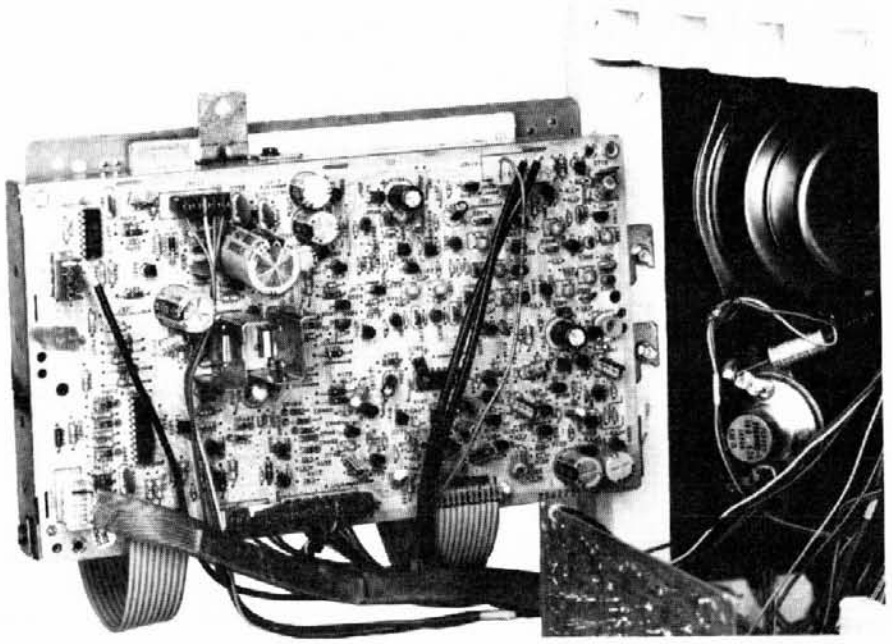
Video I/O (PWVIO) Board Block Diagram

Video I/O (PWVIO) Board

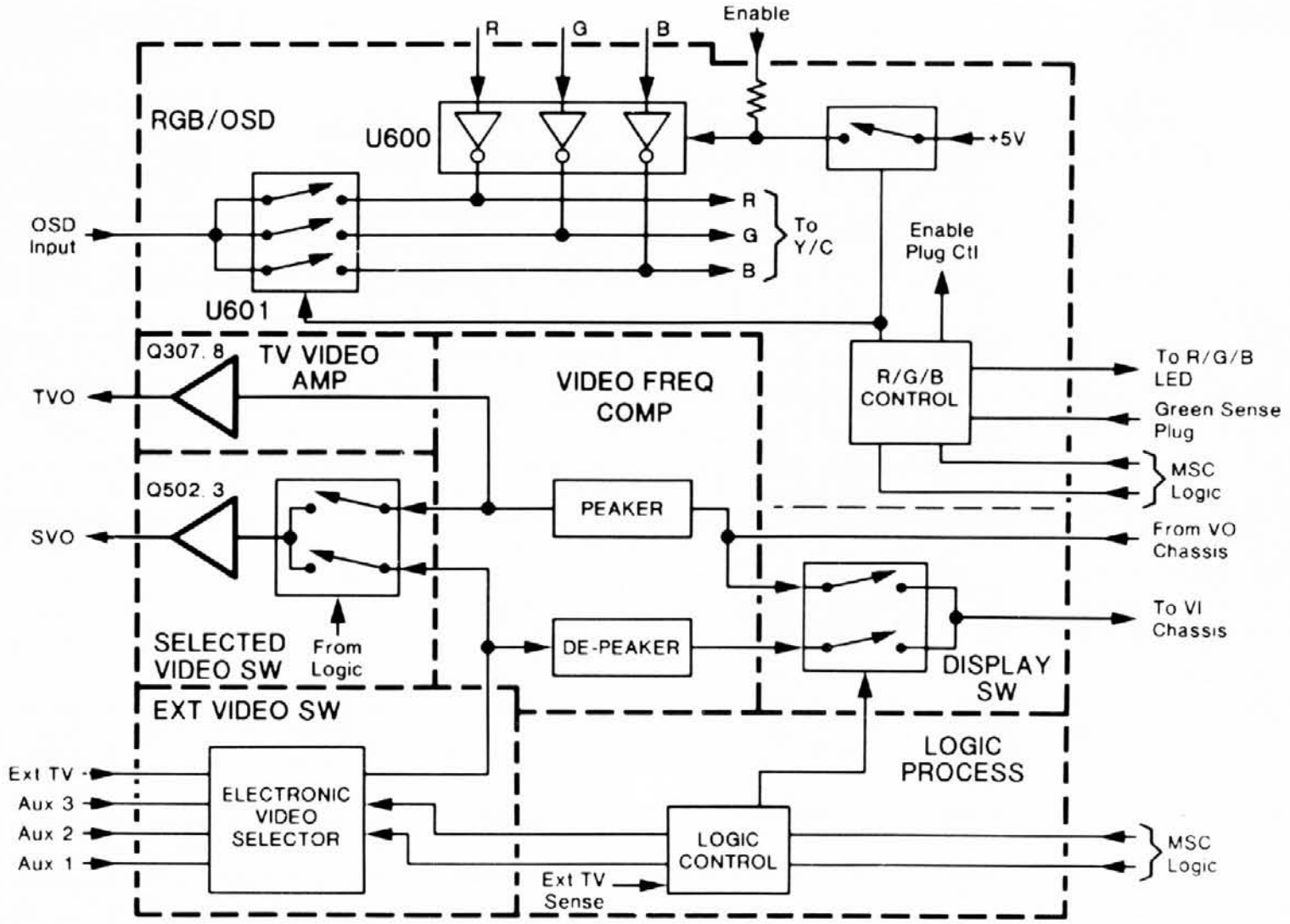
The RCA ColorTrak 2000 "Maxi" Video Monitor series utilizes a 29-connector patch panel at the rear of the receiver, allowing for a substantial amount of versatility in connecting various peripheral devices. With the variety of connections, many applications can be achieved to connect various input/output signals and some accessories to the rear of the receiver. The 29-connectors are mounted on a circuit assembly called the PWJP (jacks panel) assembly. This assembly contains the input/output connectors and a small amount of circuitry that switches the audio sources to the input of the audio processing system.

The video I/O (PWVIO) circuit assembly is mounted on the rear of the jacks panel board. Contained on this assembly is a variety of circuits allowing the electronic selection of external video input signals, output of the **selected video** signal, and output of the television tuner/IF video signal. The video input path contains a depeaker circuit to characterize the frequency response of the incoming video signal, optimizing the overall video system performance. Also, for the television video output path, the chassis video is routed through a peaking/equalizer system to characterize the television tuner/IF video for the same frequency response as wide baseband video.

New for the RCA ColorTrak 2000 Video Monitor series is the ability to input digital R/G/B signals directly into the video driver system of the receiver bypassing the luminance and chrominance processing systems. The advantage of using direct digital R/G/B inputs to the video driver circuitry of the television chassis allows for a much higher resolution picture for use with some home computers and video games. Also, the on-screen display information generated within the tuner control module (MSC) is applied through a solid state switch onto the R/G/B bus, which is then passed to the luma/chroma integrated circuit. As in previous ColorTrak 2000 Monitors, the selection of external video sources are achieved by selecting Channel 91, 92 or 93.



PWVIO Board Service Position



Video I/O (PWVIO) Board Block Diagram

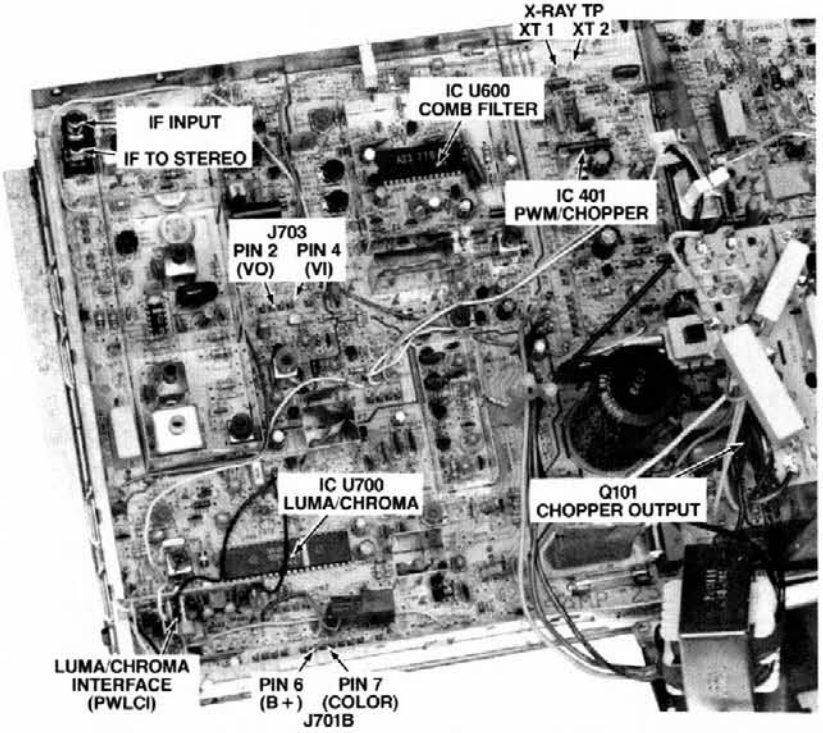
Symptom(s)

No Video

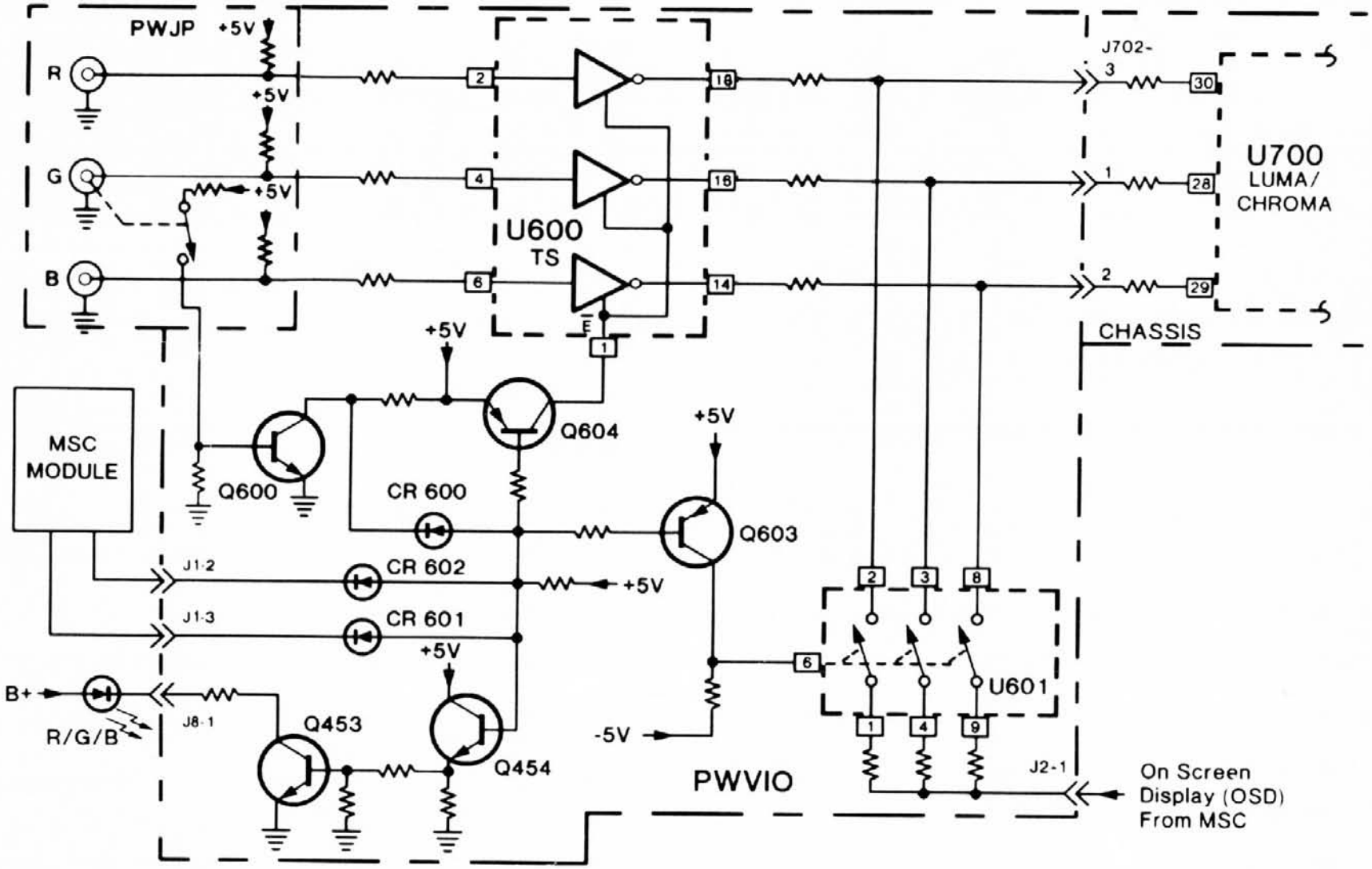
Service Procedure(s)

The detected video signal from the IF circuitry is routed from the CTC 131/132 chassis, stake VO, to the PWVIO circuit board assembly. The video select circuitry on the PWVIO board then utilizes solid state switches to select the proper video source of either the television video or one of the auxiliary inputs — Aux 1, 2 or 3. The selected video is then routed back to the video input point of the television chassis at stake VI.

During servicing of the Monitor/Receiver for a symptom of No Video, it is necessary to isolate the problem to the video selection circuitry of the video IO board or the video circuitry of the TV chassis. In order to easily achieve this, remove the cable assembly that interconnects the video I/O panel and the television chassis. This cable is connected to the CTC 131/132 chassis at connector location J703. Then connect a cliplead jumper between pins 2 and 4 of J703, routing the output video from the chassis back to the video input of the chassis. This bypasses the external video processing of the VIO circuit board assembly. If normal video appears on the receiver screen, assume the problem is contained somewhere on the video I/O board (PWVIO). If the video information still does not appear on the screen, assume that a problem exists somewhere in the signal processing area of the chassis.



CTC 131 Television Chassis (Left Half)



R/G/B On-Screen Display Input Operation

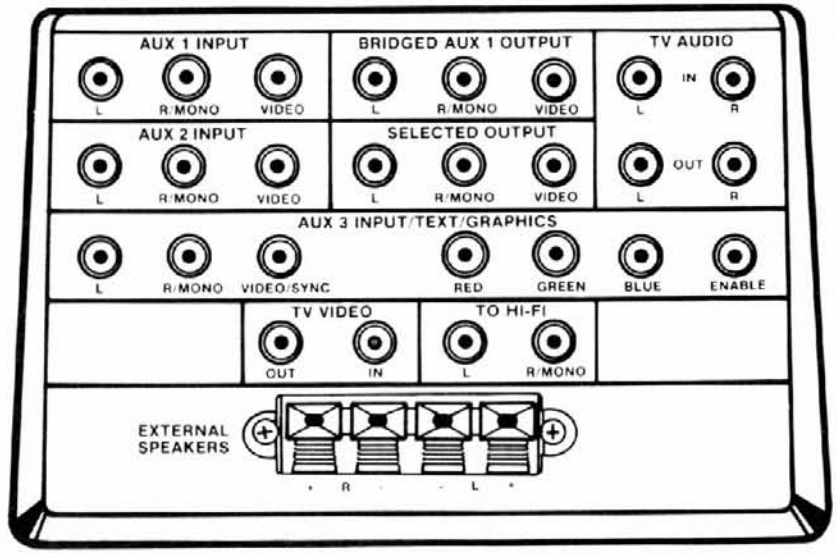
R/G/B On-Screen Display Input Operation

A new type of input system utilized in RCA ColorTrak 2000 "Maxi" Video Monitors allows for direct input of **digital R/G/B** input signals. Applying digital R/G/B signals to the video driver circuitry, via the jack panel, eliminates all of the luminance and chrominance processing areas. This allows for much higher resolution picture when compared to conventional video input methods.

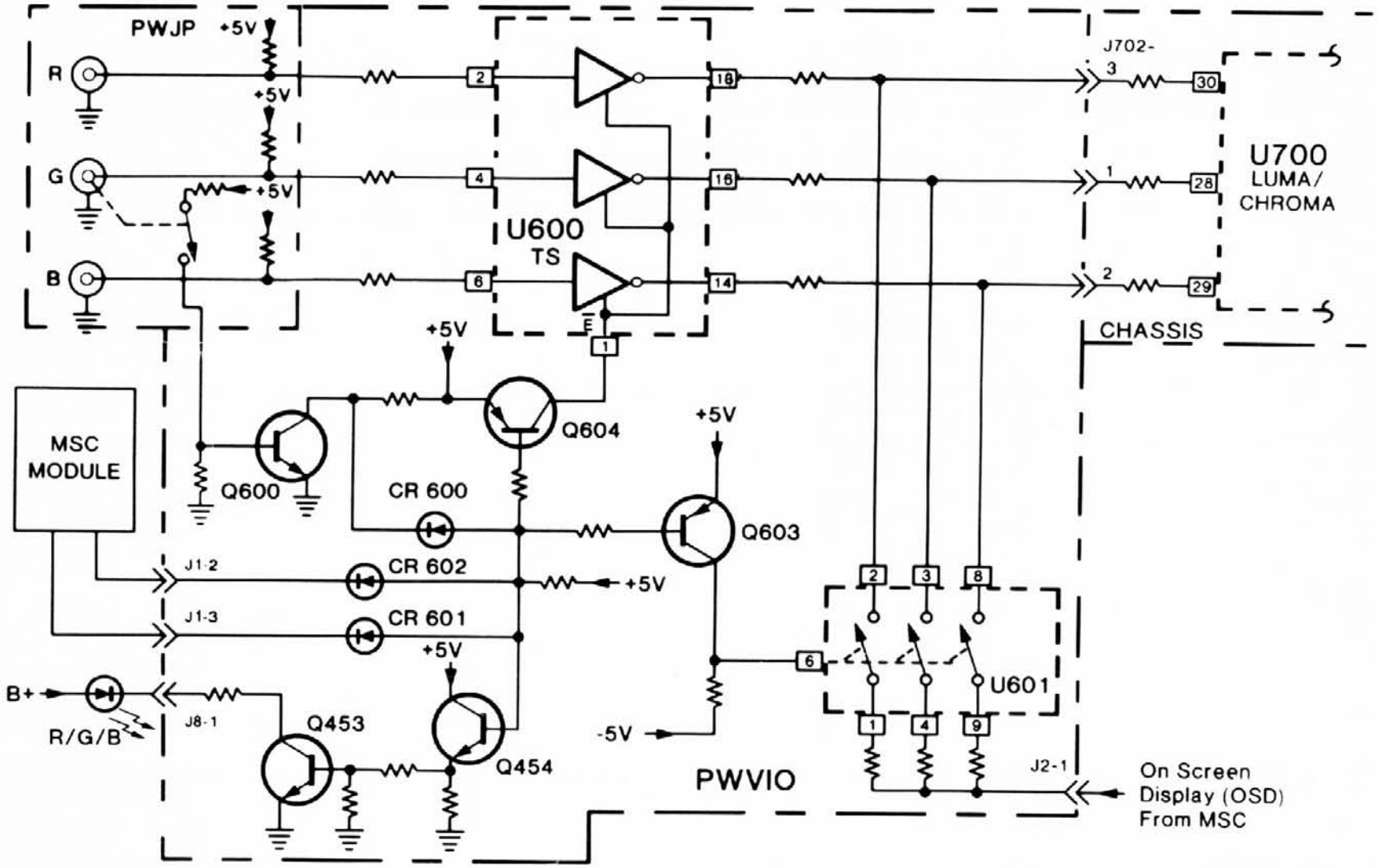
Luma/chroma IC U700 allows for the direct input of three digital signals at pins 28, 29 and 30. The luma/chroma IC input pins are **TTL (Transistor-Transistor-Logic) sensing** ports, and internal to the luma/chroma IC is circuitry that detects if a TTL source has been applied to any of the three inputs. If the IC detects a TTL source at one of the signal input pins, U700 then utilizes that particular input signal and directly applies it to the kine drive circuitry. The signal is routed through the PWLCI board directly to the Automatic Kine Bias/Driver board. If **no connection** is made to any of these three input pins, the luma/chroma IC utilizes the internally processed luminance and chrominance information that is derived from the NTSC video input at stake VI of the television chassis. The luma/chroma IC's R/G/B inputs also include signals from the on-screen display (OSD), generated within the tuner control module (MSC).

The on-screen display information occurs when the IR hand unit signal is received, requiring a display be brought up on the screen to indicate the status of the channel and the time information. During this period of time, the on-screen display signal from the MSC control module is applied through connector J2, pin 1, to IC U601, pins 1, 4 and 9. For example, assume that the television receiver is set for a normal off-the-air channel. The logic input at pin 6 of IC U601 is logic "Hi" closing all three switches, passing the on-screen display signal to output pins 2, 3, and 8 and then to the R/G/B bus. This output signal is routed to IC U700 the luma/chroma IC, pins 28, 29, and 30. During the time the on-screen display is activated, the TTL signal source within the MSC module is sensed by the luma/chroma IC and the on-screen display information directly to the screen of the receiver. At the end of the on-screen display period, the MSC module circuitry tri-states the output port of the on-screen display output. In this application, the tri-state mode simply means that the output device of the circuit is in a mode of operation where it is open circuited and supplies no signal. To summarize, at the end of the on-screen display period with the output of the MSC module going to a tri-state condition, the luminance/chrominance IC R/G/B input ports sense the loss of the TTL source and reverts back to utilizing the internally processed luminance/chrominance information from the NTSC video signal

During R/G/B input operation (Aux 3 or 93 selected and plug in green jack), the digital signals are applied to RCA phono jacks at the rear of the receiver on the PWJP circuit assembly. These three signals are routed to the input of buffer IC U600, pins 2, 4 and 6. The output of the inverting buffer stage for each R/G/B signal are pins 14, 16 and 18. Integrated circuit U600 is also a tri-state integrated circuit, where the enable input, pin 1, determines if the output ports of the integrated circuit are in a **TTL source** state or an **open circuit** state. A logic "Lo" at pin 1 places the output ports in a TTL active state. A "Hi' at pin 1 places the IC in the tri-state (floating) mode of operation. During actual R/G/B operation (Aux 3 or 93 is selected and phono plug inserted into green jack), pin 1 is logic "Lo." This logic "Lo" enables the buffer stages to invert the incoming R/G/B signal and apply them to the bus. The luma/chroma IC uses the R/G/B signal for a signal source instead of the internally demodulated NTSC signal.



29–Connection ColorTrak 2000 Maxi Monitor Rear Patch Panel



R/G/B On-Screen Display Input Operation

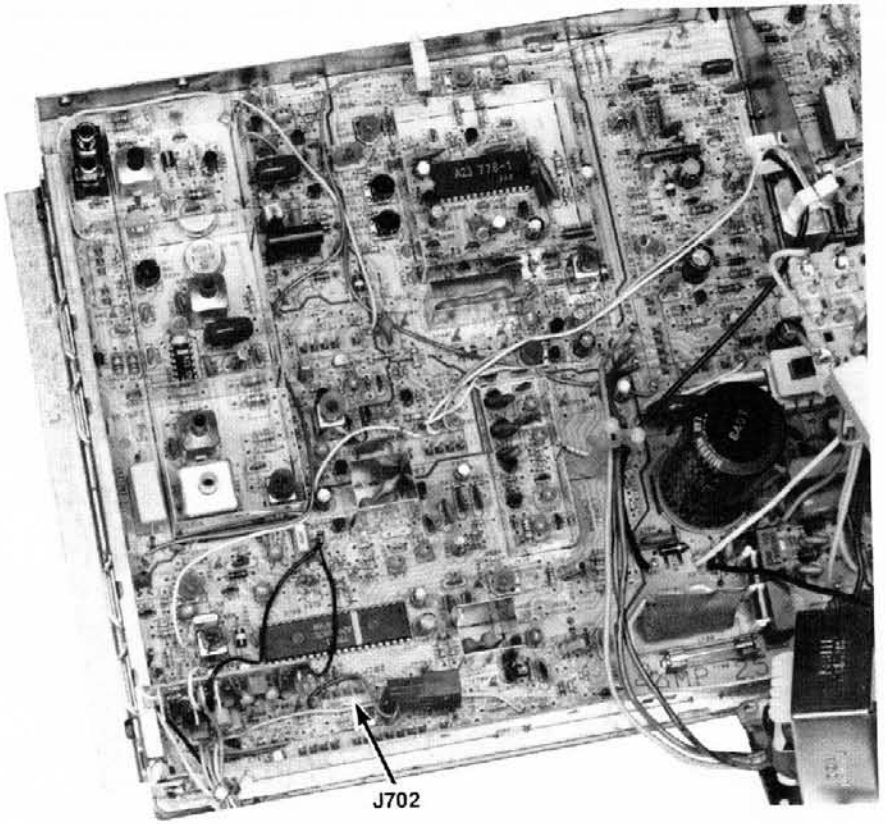
The logic condition of transistors Q603 and Q604 determines when the R/G/B or OSD inputs are used. When the user selects Channel 93, the MSC module generates a logic "Hi" output at connector J2, pins 2 and 3. A logic "Hi" at these two connectors, reverse bias diodes CR 601 and CR 602. If R/G/B cables are **not** plugged into the rear of the jack panel, the video select system automatically switches to the Auxiliary 3 (Channel 93) inputs, utilizing the Auxiliary 3 video input jack as a standard NTSC Video-In port. When an RCA phono jack is plugged into the **green input phono socket** on the rear of the receiver, an internal switch to the socket senses the plug. This opens the connection between the base of transistor Q600 and the pull-up resistor at the green input socket. When this occurs, transistor Q600 turns **"off"** applying a logic "Hi" to the cathode of diode CR 600, reverse biasing the diode. With diodes CR 600, 601, 602 reverse biased, the anodes are pulled "Hi," placing the bases of transistors Q454, Q603 and Q604 logic "Hi." The logic "Hi" at transistor Q454 is passed to the base of Q453, turning "on" the transistor, which illuminates the front panel R/G/B indicator. The logic "Hi" applied to the base of transistor Q603 turns **"off"** the emitter base junction, allowing the collector to be pulled to the −5-volt level or logic "Lo." This action opens the on-screen display switches within IC U601. Lastly, the logic "Hi" applied to the base of Q604 turns "off" transistor Q604 removing the logic "Hi" at pin 1 of IC U600. This allows the internal impedance of the integrated circuit to assume a "Lo" state enabling the output ports of the integrated circuit into a TTL mode of operation. The various digital inputs at the R/G/B input connectors are then inverted and passed into the input of the luma/chroma IC during this mode of operation. The digital information appearing at the R/G/B inputs on the PWJP circuit board assembly, develop character displays on the screen of the receiver through the luma/chroma integrated circuit. Plugging the phono jack into the green input socket switches the Auxiliary 3 input into the R/G/B mode of operation. The **Aux 3 video input** system is then utilized as a sync signal input from the R/G/B signal source, allowing the receiver's oscillators to synchronize to the incoming R/G/B signals.

Symptom(s)

Loss of One Color, Dark Screen, White Screen

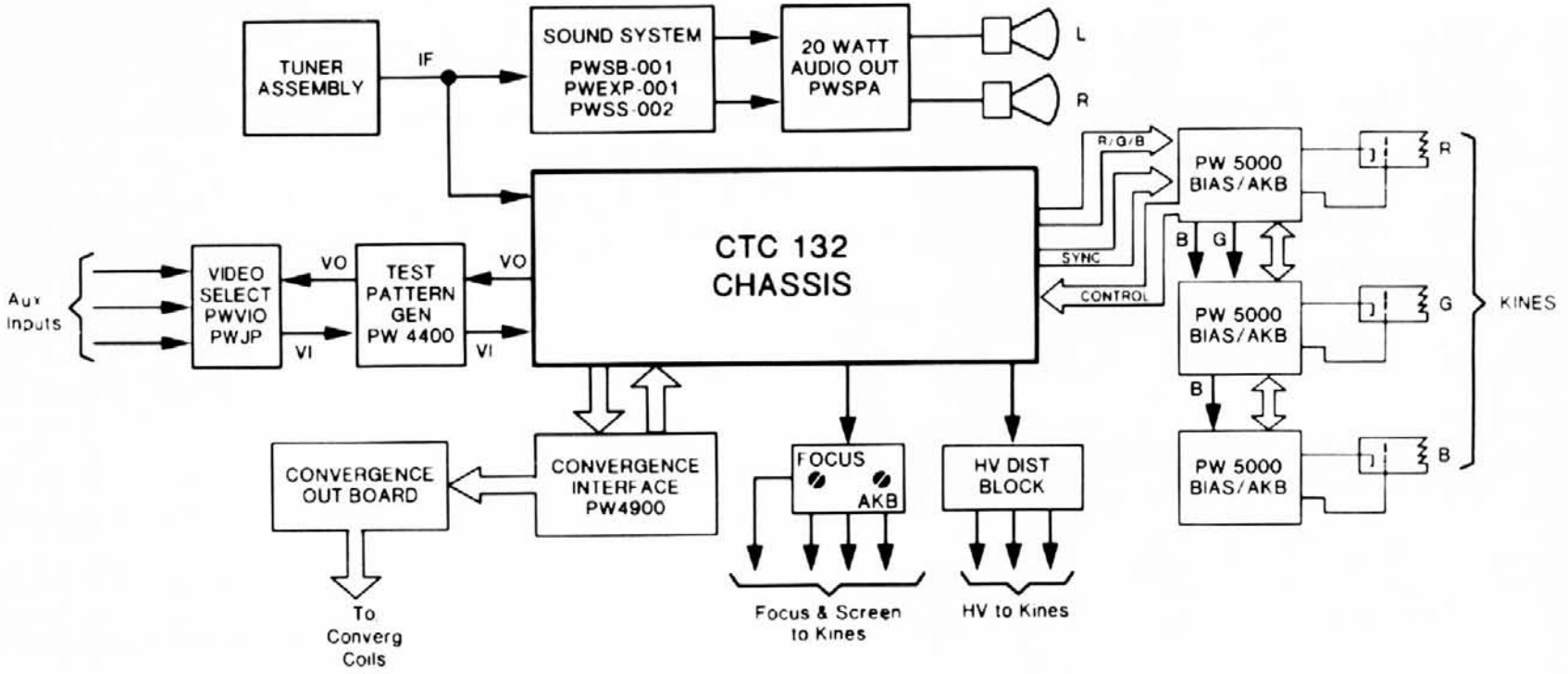
Service Procedure(s)

A defect in the on-screen display buffer within the MSC module or a problem in tri-state buffer IC U600 of the PWVIO circuit board can cause symptoms similar to chassis video processing problems. As a result, the technician should make an attempt to isolate the problem to either the external on-screen display (on the PWVIO assembly) or the CTC 131 chassis.



CTC 131 Television Chassis (Left Half)

Isolation can easily be accomplished by removing plug P702 from connector J702 on the CTC 131/132 chassis. If the symptom disappears after removing P702, then assume the problem falls either in the on-screen display buffer (within the MSC module) or tri-state buffer, IC U600. If the video problem stills exists, the problem is most likely on the television chassis.



K-Line Projection Television Block Diagram

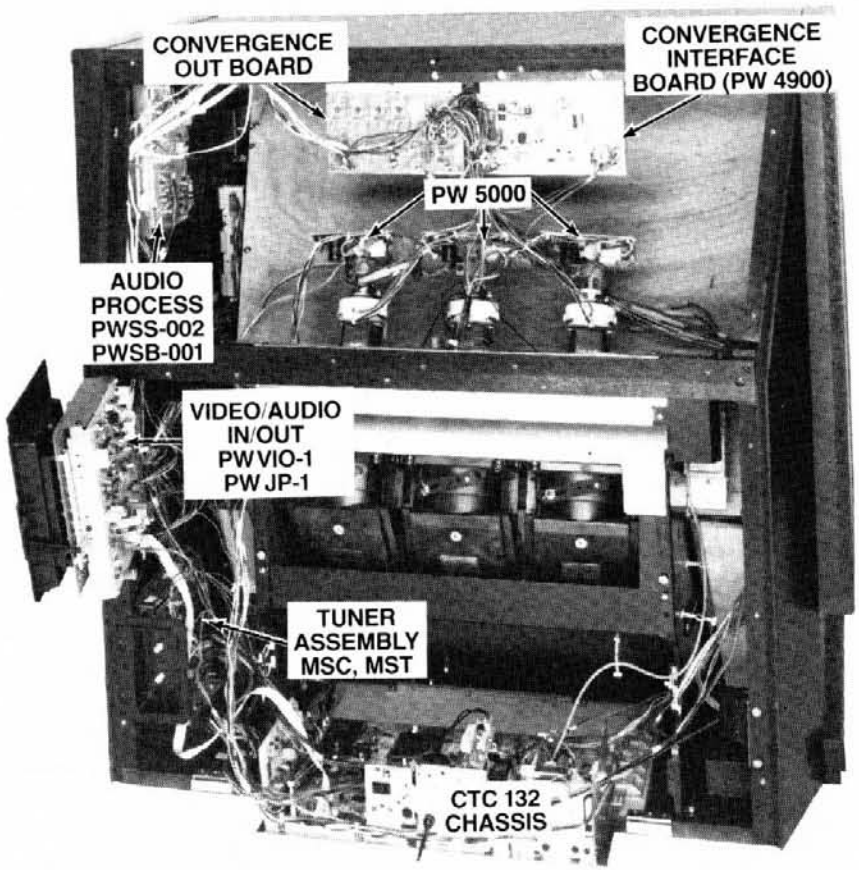
K-Line Projection Television

As stated earlier in this publication, the RCA K-line Projection TV series utilizes a CTC 132 chassis, which is a modified CTC 131 chassis. Circuit descriptions of areas within the CTC 131 also pertain to the concepts utilized in the CTC 132 chassis. Satellite assemblies, such as the audio sound system, PWSB, PWEXP and PWSS assemblies are identical to the ones utilized in the RCA ColorTrak 2000 Monitors. Additional assemblies utilized to adapt the RCA television chassis to the Projection Television System include: the high voltage distributor block, convergence interface (PW 4900) assembly, convergence output board assembly, test pattern generator (PW 4400), 20-watt audio output subassembly (PWSPA), and three kine bias/AKB circuit assemblies.

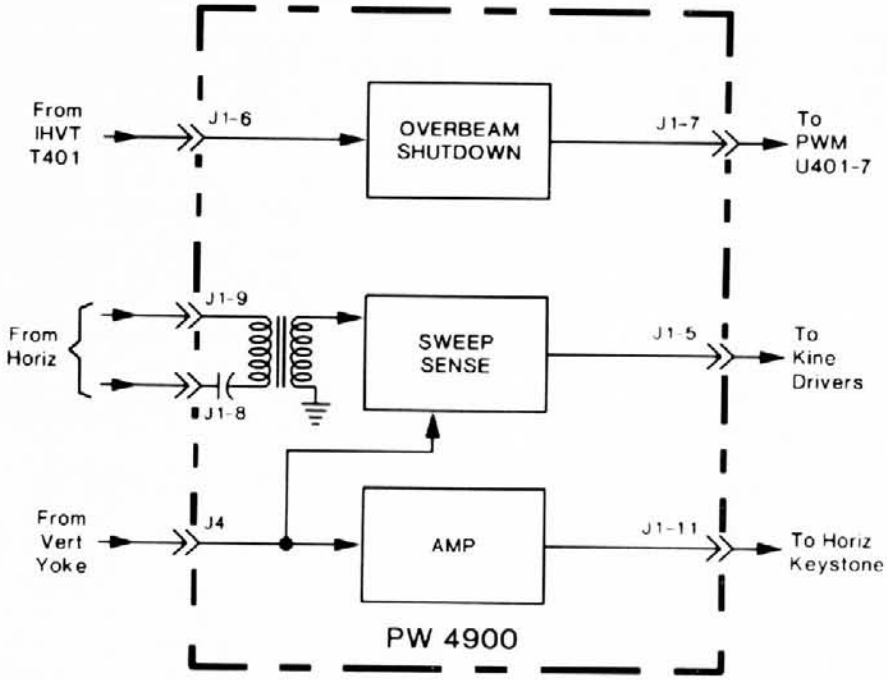
The video bias/AKB circuit assemblies utilize this same AKB integrated circuit as the previously discussed CTC 131 chassis. Because the projection television utilizes three separate CRT's, an AKB integrated circuit is utilized at the kine drive board at the rear of each picture tube. In the CTC 131 chassis, each gun of the picture tube is processed by one of three independent channels **within** the AKB integrated circuit. However, in the projection television where there are three separate picture tubes and three separate AKB integrated circuits, only **one-third** of the analog processing system of each AKB chip is utilized.

The added test pattern generator circuit board assembly (PW 4400), connected between the external video select assembly and television chassis, is included with the projection television series allowing generation of a test pattern for convergence adjustments on the screen. If a problem exists, where the technician feels the problem may possibly be on the test pattern generator circuit board assembly, merely unplug the cable from the external video select assembly (PWVIO) and exchange it with the cable on the CTC 132 (chassis cable that goes to the test pattern board). If the video problem disappears, the defect is on the test pattern generator circuit board assembly.

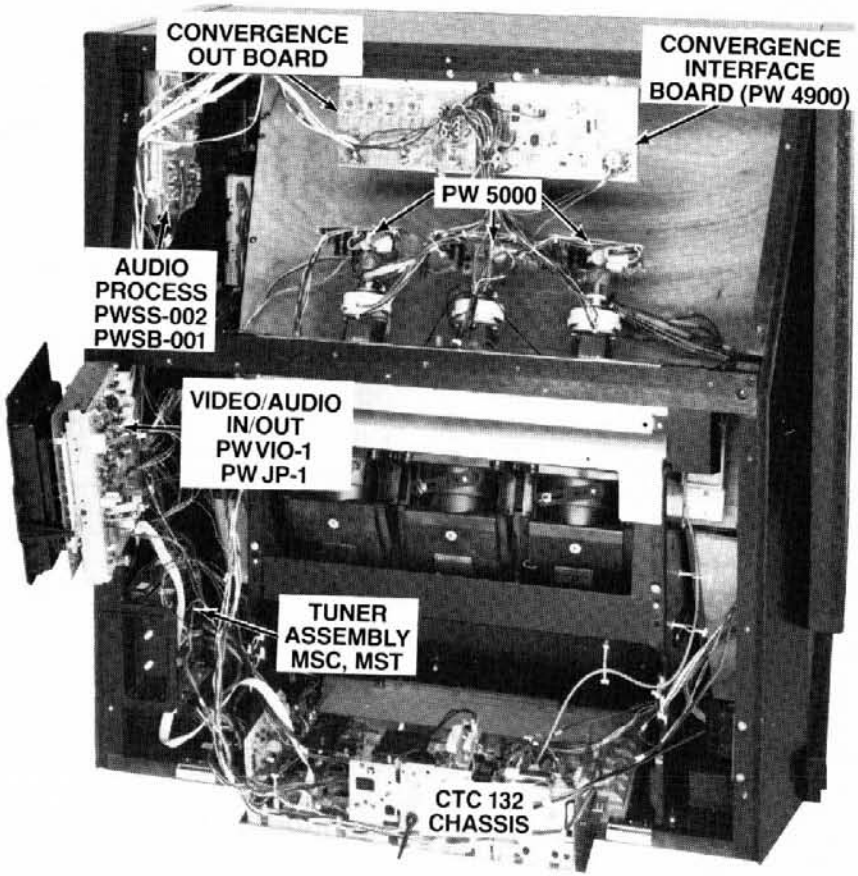
The projection television satellite assemblies are considered as modules during the warranty period and can be exchanged in lieu of component level servicing. The CTC 132 chassis **must** be serviced at component level. In most cases, the servicing flowcharts and information contained in this publication that pertain to the CTC 131 chassis also apply to servicing the circuitry in the CTC 132 Projection Television chassis.



PKC 500 Subassembly Locations



Convergence Interface Board (PW 4900) Block Diagram



PKC 500 Subassembly Locations

Convergence Interface Board (PW 4900)

The convergence interface assembly (PW 4900) contains a variety of circuits added to the projection television series that are necessary for a three picture tube system. Due to the amount of high voltage applied to the very small picture tubes, additional protection is provided for overbeam current. As a result, an overbeam current shutdown system is included on the PW 4900 board.

The IHVT return line from T401 is applied to connector J1, pin 6, of the convergence interface assembly. If excessive beam current is present, the output from the overbeam shutdown circuit applies a logic "Hi" output to pin 7 of connector J1, which is routed to PWM power supply system IC U401, pin 7. The logic "Hi" applied to U401, pin 7 causes the PWM system to turn "off" the chopper power supply on the CTC 132 chassis. As a result, scan derived B+ is lost and the television shuts down. This protection scheme protects the expensive picture tubes from damage in the event that excessive beam current may occur.

Another safety feature is provided for the small 7-inch picture tubes in the event that deflection sweep is lost. This safety feature works by applying, both vertical and horizontal scan signals to a sweep sense circuit on the convergence interface board. When scan is detected, a logic "Lo" signal is applied through connector J1, pin 5 to the kine drive circuit board assembly (red drive board). This logic "Lo" signal at the kine drive circuit board assembly turns "on" a B+ switching circuit applying B+ power to the video bias/AKB system, allowing normal operation of the video drive circuitry to the picture tubes. If loss of either horizontal or vertical deflection is sensed, the output at pin 5 of connector J1 immediately rises logic "Hi," turning "off" the B+ power to the automatic kine bias system, and as a result, turns "off" the bias of the picture tubes protecting the picture tubes from serious damage.

The third and final circuit on the PW 4900 is an amplifier for keystone correction. A vertical signal from the yoke output point of the CTC 132 chassis is routed through connector J4 to an internal amplifier on the PW 4900 circuit board assembly. The amplified vertical parabola signal is output at J1, pin 11 and routed back to the CTC 132 chassis, modulating the horizontal scan at a vertical rate for keystone correction. Keystone correction circuitry is not uncommon to projection television receivers.

Symptom(s)

Receiver Does Not Turn "On"

Service Procedure(s)

During a Dead Set symptom, confirm for a logic "Lo" at pin 7 of connector J1 of the interface circuit board assembly. If a logic "Lo" appears at the time the set is turned "on," the beam shutdown is not activated. Refer to the servicing procedure regarding the PWM chopper regulator and horizontal output servicing. If a logic "Hi" pulse appears at J1, pin 7 at turn "on," suspect a problem in the overbeam current shutdown area. During the warranty period, the technician can replace the complete convergence interface assembly or service the assembly discretely.

Symptom(s)

No Picture, Audio OK

Service Procedure(s)

Confirm the presence of a logic "Hi" at connector J1, pin 5 of the convergence interface board with horizontal and vertical pulses present at J1, pins 8 and 9, and J4. If missing, suspect a defect in the sweep sense circuitry. If pulses are **not** present, the problem lies in the vertical/horizontal chassis circuitry.

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